A Comparative Analysis of Optimized CMOS Neural Amplifier

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***Abstract*—**This paper investigates various implementation techniques of neural amplifiers with emphasis on their design performance metrics and trade-offs such as gain, noise, power consumption, and area. The proposed comparative analysis covers the recently published neural amplifiers in the literature, and proposes a basic optimization method for these amplifiers. These amplifiers are redesigned using UMC 130nm CMOS technology for fair comparison.

***Keywords*—** neural amplifiers, low noise, subthreshold OTAs, self-biased OTAs, and pseudo resistors.

I. Introduction

The Rapid growth of the electronic industry and neuroscience research led to evolutional milestones in biomedical systems. Based on this growth, scientists spare no effort in developing microsystems that are able to record and stimulate neural brain activities. This helps in treating several neurological disorders such as Epilepsy and Parkinson diseases [1].

Design of a neural recording system faces many challenges, starting from the design of the implantable electrode needed for recording the neural signal, and ended with the feature extraction from the recorded signals. A low noise pre-amplifier (LNA) is needed, because the bio-potential signals' amplitude ranges from a few microvolts to several millivolts, and covers a wide range of frequencies from few millihertz to kilohertz [2]. In order to process these signals, they should be digitized with a high resolution, and low frequency analog-to-digital converter (ADC). The most critical part of this system is the design of the LNA, as it filters the noise without reshaping the signal, adds acceptable gain, rejects the dc offset of the electrode tissue interface, and minimizes the power consumption.

This paper introduces a comparative review and analysis of the different LNA architectures recently published in the literature, and attempts to optimize the performance metrics for lower noise, lower power consumption, better dc cancellation, and lower implementation area. The rest of the paper is organized as follows. In Section II, the design and analysis of the different LNA architectures is presented, followed by the basic optimization technique in Section III, and ended by the simulation results in Section IV. Finally, a conclusion is derived in Section V.

II. LNA Architectures

In this Section, different LNA architectures are discussed. The LNA architectures are classified based on (1) differential or single ended, (2) the operational transconductance amplifier (OTA) structure, and (3) the feedback resistors to achieve the required specifications based on the application are presented.

A. Fully Differential Capacitive Feedback LNA

Using a fully differential amplifier applies a great advantage in reducing the noise whether it comes from the circuit itself, or the neighbouring circuits. In Fig. 1, the closed loop LNA circuit is shown, where the mid-band gain is set by the ratio C_{in}/C_f, and the lower cut-off frequency is calculated by $1/2\pi R_f C_f$ [5]. The low cut-off frequency should vary from 0.1 Hz to 10 Hz, and accordingly, we need to implement a very high impedance feedback resistor in range of GΩ [5]. To implement these resistors, PMOS transistors biased in the subthreshold region are used, where we can obtain any frequency in the range stated above (i.e., 0.1Hz to 10Hz) by changing V_{res} [4]. Regarding the higher cut-off frequency, it is controlled by the bias current of the OTA and the load capacitance [5].

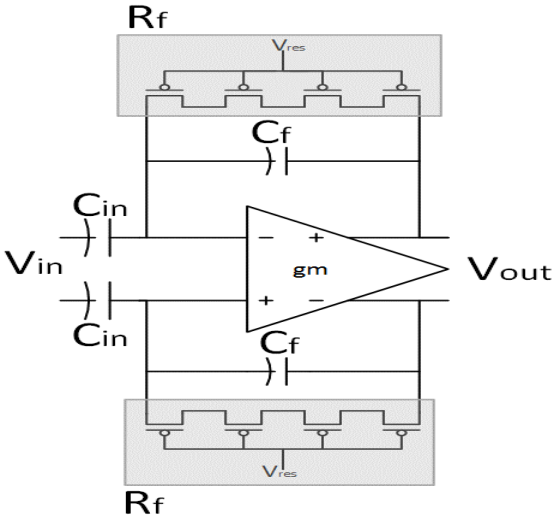

Fig. 1 Closed Loop LNA Schematic [4]

A fully differential Telescopic OTA is used to implement this LNA. This OTA provides low power consumption, good noise performance, and a sufficient output swing. The OTA circuit schematic, and its common mode feedback (CMFB) circuit are shown in Fig. 2. Due to the low operating frequency range of neural amplifiers, the impact of the flicker noise and the thermal noise is significant and must be taken into account [4].

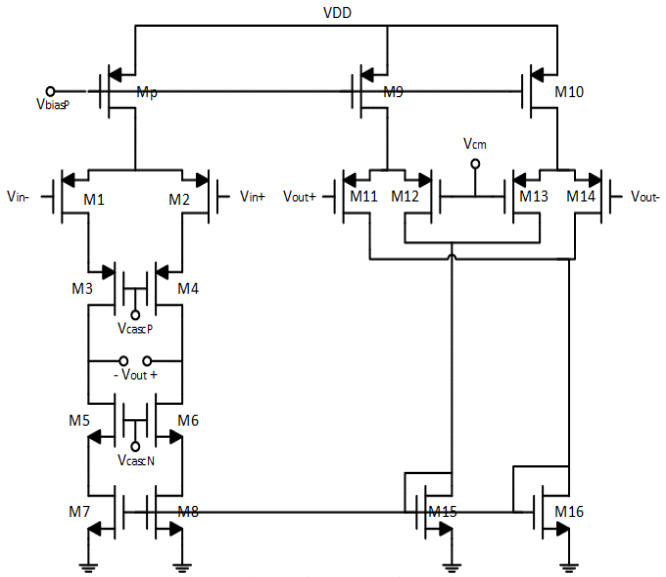

Fig. 2 Telescopic OTA Schematic [4]

B. *Single Ended Capacitive Feedback LNA*

This LNA uses a single ended OTA with a capacitive feedback topology [3], as shown in Fig. 3. Two coupling capacitors are used to reject the dc offset associated with the sensing electrodes. The high-pass cut off frequency is controlled by the biasing resistance on the positive input terminal of the OTA in parallel with the capacitor. To achieve an extremely low high-pass cut off frequency, a resistance in the range of GΩ is needed. This huge resistance is implemented by using two pseudo resistors connected as shown in Fig. 3. On the other hand, the low-pass cut off frequency is set by the gain of the OTA and the load capacitance connected at the output node. Finally, the gain of the amplifier is controlled by the ratio between the coupling capacitor divided by the feedback capacitor [3].

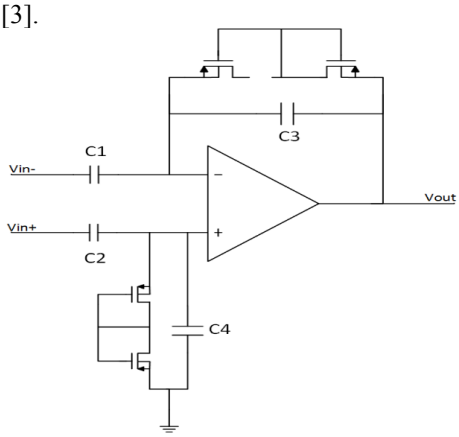

Fig. 3 Single Ended pre-amplifier Schematic [3]

A two stage amplifier with a Miller compensating capacitor C_5 is used for the OTA design as shown in Fig. 4. A cascode stage that is formed by the transistors M3, and M4 is added to the input differential pair transistors (M1, and M2) in order to increase the gain of the first stage, and to enhance the phase margin of the amplifier by cancelling the right half plane zero, which is formed by the miller capacitance, instead of using a compensation resistance [3]. The path formed from the capacitance C_6 with the transistor M10 is used to enhance the settling time of the amplifier. To minimize the flicker noise of the input pair transistors, their gate size is designed large. Thus, increasing their areas means decreasing the input referred noise of the OTA [3].

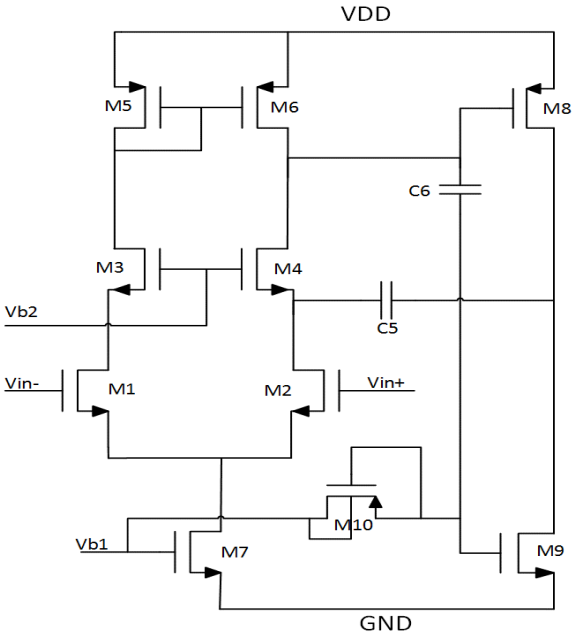

Fig. 4 OTA Schematic [3]

C. *LNA with Active Low Frequency Suppression*

This LNA with its active low frequency suppression circuit is shown in Fig. 5. This LNA presents an active dc rejection scheme that does not require any AC coupling capacitors. This makes it suitable for the massive integration in implantable neural recording amplifiers, and preserves the LNA high input impedance [6]. This configuration relies on placing an active integrator in the feedback path of the LNA that rejects any DC offset and places the high pass cut off frequency within the transfer function [6].

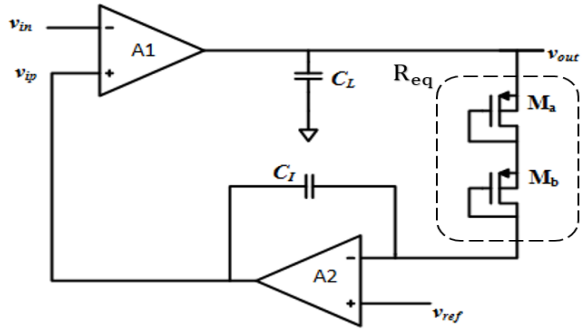

Fig. 5 LNA with the active feedback network Circuit Schematic [7]

This LNA circuit consists of a single ended low noise OTA (A1) shown in Fig. 6, where the OTA output is connected to a Miller integrator in the feedback path. The active feedback network is designed from another OTA (A2), a capacitor (C_I) and a high impedance pseudo resistor (R_{eq}) which leads to a high time constant ($\tau = R_{eq}C_I$), and sets the -3db high pass cut off frequency (f_{hp}) as shown in the following equation [7]:

$$f_{hp} = \frac{1}{2\pi}\frac{A_{01}}{R_{eq}C_I}$$

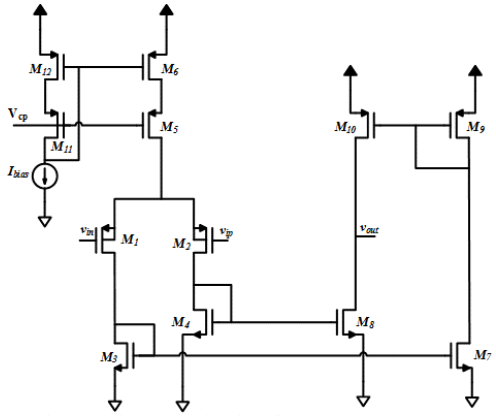

Fig. 6 Main OTA Circuit Schematic [7]

In addition, the midband gain of this LNA is the same as the DC gain of OTA1 (A_{01}), where $A_{01} = g_m/g_0$ ($g_m = g_{m1,2}$ and $g_m = g_{m8,10}$). Finally, the -3db low-pass cut off frequency (f_{1p}) is given by the following equation [7]:

$$f_{1p} = \frac{1}{2\pi}\frac{gm}{A_{01}C_L}$$

For the active feedback network, a two stage OTA topology with a lead compensation was chosen for A_2 as shown in Fig. 7. This OTA is used to provide a high dc gain, and maintain less implementation area. The integrator circuit ensures that node V_{ip} tracks the dc level seen by V_{in}, cancelling any dc offset, or any other low-frequency voltages. Moreover, it introduces a 90° phase shift to the output signal [8].

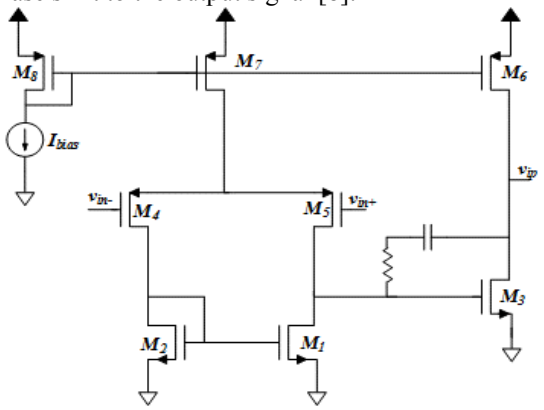

Fig. 7 Feedback OTA Circuit Schematic [7]

III. Optimization

In this section, an optimization method for lower power consumption, and better noise performance is discussed. The pre-mentioned neural amplifiers are optimized by replacing the used OTA by an optimized one.

A. Current-Reuse OTA

The circuit schematic is shown in Fig. 8, where it achieves an extremely low power consumption, and a better noise performance [11]. To minimize the flicker noise, and the thermal noise, the input transistors (P1, P2, N1, and N2) are biased in the subthreshold region. For the CMFB circuit, the transistors (N3, and N4) are used to define the DC output level, and a resistive sensing elements are used [11]. These resistive sensing elements are implemented using the two diode connected PMOS transistors. Thus, they act as a large impedance, and maintain a high gain at the output [11].

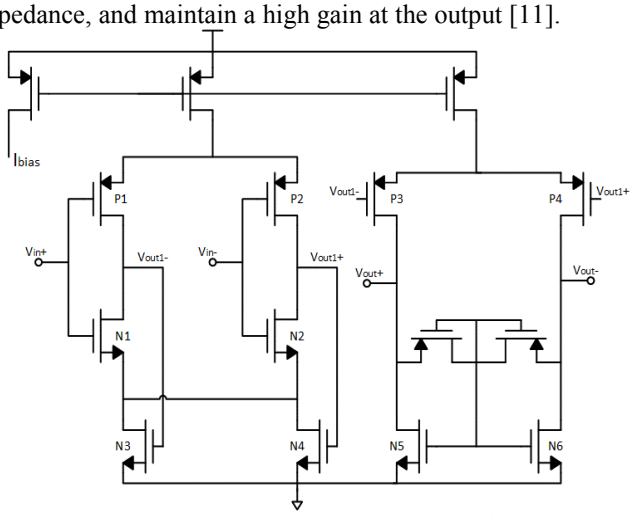

Fig. 8 Fully Differential Current-Reuse OTA Circuit Schematic [11]

B. Bulk-Driven OTA

To reduce the power consumption extensively, bulk-driven OTAs are good candidates for this purpose. The idea is to connect the input voltage to the bulk terminal which offers several advantages such as the removal of the threshold voltage constraints, wider input common mode range spanning from negative voltages to slight positive input voltage, and operation on low supply voltages [9,10]. On the other hand, the bulk driven OTAs have several disadvantages including higher input referred noise, lower transconductance, and lower bandwidth. Moreover, the bulk driven fabrication process usually has higher cost [10].

In Fig. 9, the schematic of the enhanced bulk driven OTA is shown. To increase the transconductance of the transistors, a positive feedback source degeneration is proposed and used to reach a higher gain and relatively a higher bandwidth [10]. Moreover, this enhancement is carried out without any need to increase the power consumption. The positive feedback source degeneration is the only difference from the traditional bulk driven OTAs. This OTA consists of a two stage OTA with a Miller compensation between the two stages, in order to improve the phase margin and stability of the system. The first stage is a folded cascode stage with an input bulk driven differential pair, while the second one is a normal common source OTA [10].

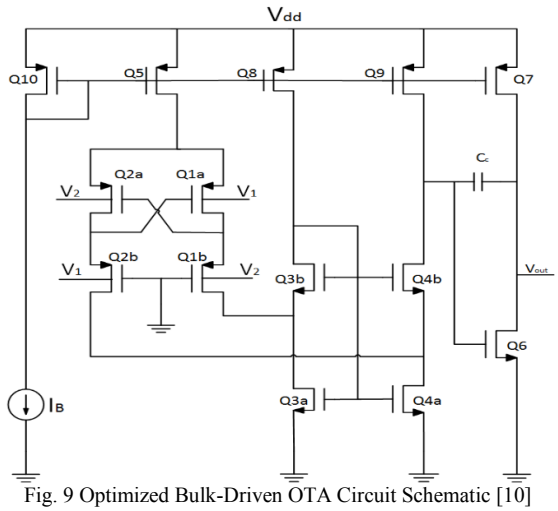

Fig. 9 Optimized Bulk-Driven OTA Circuit Schematic [10]

IV. Simulation Results

In this section, all the previous neural LNA circuits are simulated using hardware-calibrated UMC 130 nm CMOS technology under the same environment to guarantee fair comparison as listed in Table I.

Here are the proposed modifications as following:

- The neural amplifiers are re-simulated, and achieved better results due to technology scaling as shown in Table I.
- For the fully differential capacitive feedback LNA, single stage amplifier, the telescopic OTA has been replaced by current re-use OTA for lower power consumption, and better noise performance as shown is shown in Table I.
- For the single ended capacitive feedback LNA, the circuit was resized from the beginning for optimized results, so no need for further investigation, and this obvious in Table I.
- For the LNA with active low frequency suppression, both OTAs replaced by the bulk-driven OTA. This modification has improved the midband gain, the power consumption, but the input referred noise has been degraded. However, this was expected from the bulk driven OTA.

V. Conclusion

In this paper, using 1.2 V supply voltage and 130 nm technology, several types of neural amplifiers are designed and simulated using the same technology and the same environmental conditions to guarantee fair comparison. The comparison shows many topologies whether differential or single ended output, wide bands for different applications, and a several dc rejection techniques. The comparison emphasizes the effect of replacing the used OTAs by a more efficient designs reducing the power consumption in such great rate. Moreover, the noise performance, and the bandwidth improved, but not with all designs.

VI. Acknowledgment

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TABLE I
Comparison between different LNA architectures

Reference	Circuit Topology	Midband Gain (dBs)	High-pass cut off frequency (Hz)	Low-pass cut off frequency (KHz)	Input Referred Noise ($\mu V / \sqrt{Hz}$)	Power Consumption (μW)	DC Rejection Technique
[4]	Differential Ended Output	33	10	5	3.75	4.76	AC Coupling
[3]	Single Ended Output	45.88	0.05	2.1	1.195	0.1712	AC Coupling
[8]	Single Ended Output	53.78	9	11	4.42	8.1	Active Feedback Sensing
Optimized for [4]	Differential Ended Output	33	5.7	10.5	2.34	0.1953	AC Coupling
Optimized for [8]	Single Ended Output	79.2	6.1	0.143	20	1.52	Active Feedback Sensing