Design of High Frequency Three Port VCVS Structures

Entwurf von hochfrequenten Dreitor-VCVS-Anordnungen

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Abstract:

Active phase compensation methods of the three port voltage controlled voltage source structure (VCVS) employing two operational amplifiers are considered. Three theorems describing the necessary coefficient relations for the three port mode of operation as well as the phase compensation condition for the generalized VCVS structures are derived. Fourteen different phase compensated three port VCVS networks are given. The properties of each network and the design equations from the specified noninverting and inverting DC gains are summarized in tables.

Übersicht:

Es werden Methoden der aktiven Phasenkompensation bei Dreitoranordnungen mit spannungsgeregelten Spannungsquellen beschrieben, die zwei Operationsverstärker enthalten. Drei Theoreme werden entwickelt, welche die Koeffizientenbeziehungen für die Betriebsweise des Dreitores und die Bedingungen für die Phasenkompensation verallgemeinerter VCVS-Anordnungen angeben. Vierzehn verschiedene phasenkompensierte Dreitor-VCVS-Schaltungen werden gezeigt. Die Dimensionierungen und Schaltungsgleichungen der angegebenen nichtinvertierenden und invertierenden Gleichstromverstärkungen sind in Tabellen zusammengefaßt.

Für die Dokumentation:

Dreitor / Phasenkompensation / Spannungsregelung / Spannungsquelle / Operationsverstärker / Dimensionierung

1. Introduction

It is well known that the 3 port voltage controlled voltage source (VCVS) which employs a single operational amplifier (opamp) and two resistors is suitable only for applications at low frequency due to the finite gain bandwidth of the opamp. Passive and active phase [1–3] and magnitude compensation [4] methods for the 3 port VCVS structures have been reported in the literature. In all these circuits [1–4] the noninverting DC gain „P" equals to the magnitude of the inverting DC gain „N" $+1$. Adding a potential divider at the noninverting input port will provide an additional control on P within the limited range $P \leq (N+1)$, and will result in a finite input impedance at the noninverting port.

The purpose of this paper is to provide a design procedure for the active phase compensated 3 port VCVS structures employing two opamps and having a generalized output voltage expression of the form:

$$V_0 = [PV_2 - NV_1]\,\varepsilon_c \tag{1}$$

where P is the required noninverting DC gain
N is the magnitude of the required inverting DC gain, and
ε_c is the compensated error function having a negligible phase error
(Ideally ε_c must have a zero phase and a unity magnitude).

In this paper, the active phase compensated 3 port VCVS structures using two opamps are classified into two major classes. Each class includes two types. Fourteen networks are given in this paper. The properties of each network as well as the design equations are given in Tables.

2. Analysis

The generalized active phase compensated double input VCVS employing two opamps is shown in **Fig. 1,** where V_1 and V_2 are the inverting and noninverting input voltages respectively. The basic circuit equations are represented by the following matrix equation:

$$\begin{bmatrix} \frac{V_{01}}{A_1} \\ \frac{V_{02}}{A_2} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} b_{11} & b_{12} \\ b_{21} & b_{22} \end{bmatrix} \begin{bmatrix} V_{01} \\ V_{02} \end{bmatrix}. \tag{2}$$

A_i is the open loop gain of the opamp which for all practical applications is represented by the single pole model [5]

$$A_i(s) \simeq \frac{\omega_{ti}}{s} \quad (i=1, 2) \tag{3}$$

where ω_t is the unity gain bandwidth of the opamp.

The coefficients a_{ij} and b_{ij} represent transfer functions of the resistive network and thus they are real and have magnitudes ≤ 1 $(i, j=1, 2)$; [6]. The necessary coefficient relations to operate the circuit as a 3 port phase compensated VCVS are derived next.

Theorem 1. For the generalized double input VCVS shown in Fig. 1 and having the circuit equations as given by (2) with V_{01} as the output voltage, the necessary condition for the 3 port mode of operation is given by

$$\det.\,[a] = 0 \tag{4}$$

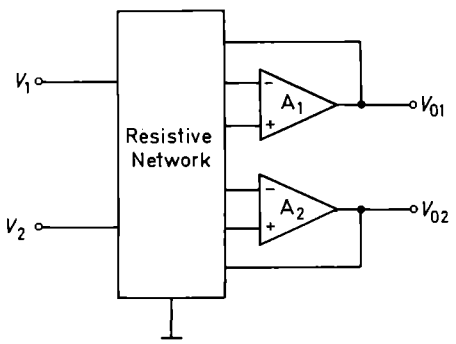


Fig. 1: The generalized double input VCVS structure employing two operational amplifiers

Proof: From (2), the generalized expression for the output voltage V_{01} is obtained as

$$V_{01}=\frac{V_1\left[-a_{11}b_{22}+a_{21}b_{12}+\frac{a_{11}}{A_2}\right]+V_2\left[a_{22}b_{12}-a_{12}b_{22}+\frac{a_{12}}{A_2}\right]}{[b_{11}b_{22}-b_{12}b_{21}]-\frac{b_{11}}{A_2}-\frac{b_{22}}{A_1}+\frac{1}{A_1A_2}}. \quad (5)$$

The numerator of the above equation can be written in the form

$$\text{Numerator}\,(V_{01})=V_1[-a_{11}b_{22}+a_{21}b_{12}]\,F_1(a,b,A)+V_2[a_{22}b_{12}-a_{12}b_{22}]\,F_2(a,b,A) \quad (6)$$

where

$$F_1(a,b,A)=1+\frac{a_{11}}{a_{21}b_{12}-a_{11}b_{22}}\,\frac{1}{A_2}, \quad (7)$$

and

$$F_2(a,b,A)=1+\frac{a_{12}}{a_{22}b_{12}-a_{12}b_{22}}\,\frac{1}{A_2}. \quad (8)$$

For the 3 port mode of operation, it is necessary that

$$F_1(a,b,A)=F_2(a,b,A),$$

From (7) and (8), thus the necessary condition for the 3 port mode of operation is given by

$$a_{11}a_{22}-a_{12}a_{21}=0 \quad \text{or} \quad \det.[a]=0 \quad \text{Q.E.D.}$$

Before considering the necessary phase compensation condition, the generalized 3 port VCVS networks will be classified into two major classes depending on whether $b_{22}=0$ or $b_{11}=0$. This condition follows from the coefficient of the s term in the denominator of (5) after using (3) (in order to limit the number of the resistors in the circuit and to reduce the sensitivity to the gain bandwidth product of the opamps). For each class, the phase compensation condition is derived next.

3. Class 1 – 3 port VCVS

Theorem 2. For a class 1, 3 port VCVS employing two opamps and having the generalized circuit equations as given by (2) with $b_{22}=0$, and with (4) being satisfied, the necessary condition for phase compensation is independent of ω_t of the opamps and is given by

$$\frac{a_{11}}{a_{21}}=\frac{b_{11}}{b_{21}}. \quad (9)$$

Proof: From (5), setting $b_{22}=0$, and using (3) and (4), thus

$$V_{01}=\left[V_1\,\frac{-a_{21}}{b_{21}}+V_2\,\frac{-a_{22}}{b_{21}}\right]\varepsilon_1(s) \quad (10)$$

where

$$\varepsilon_1(s)=\frac{1+\frac{a_{11}}{a_{21}b_{12}}\,\frac{s}{\omega_{t2}}}{1+\frac{b_{11}}{b_{12}b_{21}}\,\frac{s}{\omega_{t2}}+\frac{-1}{b_{12}b_{21}}\,\frac{s^2}{\omega_{t1}\omega_{t2}}}. \quad (11)$$

$\varepsilon_1(s)$ is the error function of the class 1 VCVS networks. In order to reduce the phase error to a negligible level it is necessary that the coefficients of the s-terms in the numerator and deonominator of $\varepsilon_1(s)$ be equal [2, 6]. Thus it follows that the phase compensation condition is independent of the unit gain bandwidth of the opamps and is given by (9) and the theorem is proved.

Thus for a class 1, 3 port VCVS networks the necessary conditions for the 3 port mode of operation and for phase compensation are given by

$$\frac{a_{11}}{a_{21}}=\frac{a_{12}}{a_{22}}=\frac{b_{11}}{b_{21}}. \quad (12)$$

Next, the coefficients a_{ij} and b_{ij} signs are obtained. From the denominator of (11) and for the stability of the network, it is necessary that the coefficient b_{11} and the produce $(b_{12}b_{21})$ must have negative signs. Two types of the VCVS structures are defined next. Type A in which b_{12} is negative and b_{21} is positive, and type B in which b_{12} is positive and b_{21} is negative. Now from (10) it follows that the coefficient a_{21} must have the same sign as b_{21}, where as a_{22} must have opposite sign to b_{21}. Finally the signs of the two remaining coefficients a_{11} and a_{12} are obtained by examining (12). The coefficients signs for both types A and B are included in **Table 1.**

Fig. 2a and b represent two networks, that are generated from the coefficient signs and both belong to the class 1 – type A. **Fig. 3** represents a class 1 – type B-3 port VCVS

Table 1: The coefficients a_{ij} and b_{ij} for classes 1 and 2 VCVS structures

The 3 port VCVS									
Class	Type	a_{11}	a_{12}	a_{21}	a_{22}	b_{11}	b_{12}	b_{21}	b_{22}
1	A	–	+	+	–	–	–	+	0
	B	–	+	–	+	–	+	–	0
2	A	–	+	0	0	0	–	+	–
	B	–	+	0	0	0	+	–	–

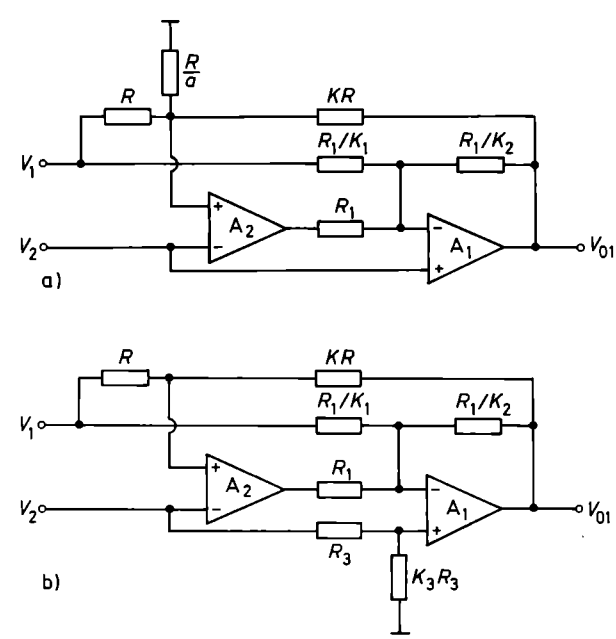


Fig. 2: Class 1 – type A, 3 port VCVS
a. Circuit 1
b. Circuit 2

Table 2: The circuit matrices $[a]$ and $[b]$ for all 3 port VCVS structures

The 3 port VCVS network				Circuit Matrices	
Class	Type	Fig.	Ref.	$[a]$	$[b]$
1	A	2a		$\begin{bmatrix} -\frac{K_1}{1+K_1+K_2} & 1 \\ \frac{K}{1+K(a+1)} & -1 \end{bmatrix}$	$\begin{bmatrix} -\frac{K_2}{1+K_1+K_2} & -\frac{1}{1+K_1+K_2} \\ \frac{1}{1+K(a+1)} & 0 \end{bmatrix}$
		2b		$\begin{bmatrix} -\frac{K_1}{1+K_1+K_2} & \frac{K_3}{1+K_3} \\ \frac{K}{1+K} & -1 \end{bmatrix}$	$\begin{bmatrix} -\frac{K_2}{1+K_1+K_2} & -\frac{1}{1+K_1+K_2} \\ \frac{1}{1+K} & 0 \end{bmatrix}$
	B	3		$\begin{bmatrix} -\frac{K}{1+K} & \frac{K_1}{1+K_1} \\ -\frac{K}{1+K} & \frac{K_2}{1+K_2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{1+K} & \frac{1}{1+K_1} \\ -\frac{1}{1+K} & 0 \end{bmatrix}$
2	A	4a 4b	[2] [3]	$\begin{bmatrix} -\frac{K_1}{1+K_1} & 1 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & -\frac{1}{1+K_1} \\ \frac{1}{1+K_2} & -\frac{1}{1+K_2} \end{bmatrix}$
		4c		$\begin{bmatrix} -\frac{K_1}{1+K_1} & 1 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & -\frac{1}{1+K_1} \\ \frac{1+K_2}{1+K_2(a+1)} & -\frac{1}{1+K_2(a+1)} \end{bmatrix}$
		4d		$\begin{bmatrix} -\frac{K_1}{1+K_1} & 1 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & -\frac{1}{1+K_1} \\ \frac{1}{1+K_2(a+1)} & -\frac{1+K_2}{1+K_2(a+1)} \end{bmatrix}$
		4e 4f		$\begin{bmatrix} -\frac{K_1}{1+K_1(a+1)} & 1 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & -\frac{1}{1+K_1(a+1)} \\ \frac{1}{1+K_2} & -\frac{1}{1+K_2} \end{bmatrix}$
		4g		$\begin{bmatrix} -\frac{K_1}{1+K_1} & 1 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & -\frac{1}{1+K_1} \\ \frac{1}{1+K_2} & -\frac{1}{1+K} \end{bmatrix}$
	B	5a		$\begin{bmatrix} -1 & \frac{K_1}{1+K_1} \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & \frac{1}{1+K_1} \\ -\frac{1}{1+K_2} & -\frac{K_2}{1+K_2} \end{bmatrix}$
		5b	[10, 11]	$\begin{bmatrix} -1 & \frac{K_1}{1+K_1} \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & \frac{1}{1+K_1} \\ -\frac{1}{1+K_2(a+1)} & -\frac{K_2}{1+K_2(a+1)} \end{bmatrix}$
		5c		$\begin{bmatrix} -1 & \frac{K_1}{1+K_1(a+1)} \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & \frac{1}{1+K_1(a+1)} \\ -\frac{1}{1+K_2} & -\frac{K_2}{1+K_2} \end{bmatrix}$
		5d		$\begin{bmatrix} -1 & \frac{K_1}{1+K_1} \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & \frac{1}{1+K_1} \\ \frac{1}{1+K_3} - \frac{1}{1+K_2} & -\frac{K_2}{1+K_2} \end{bmatrix}$

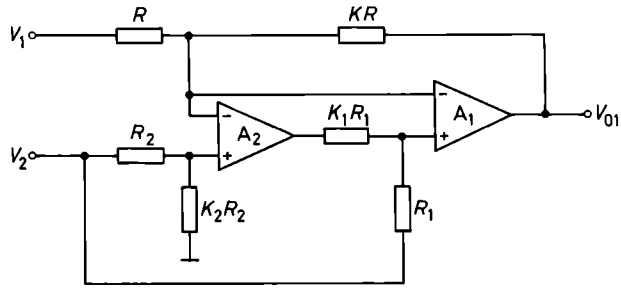


Fig. 3: Class 1 – type B, 3 port VCVS

network. The circuit matrices for these networks are included in **Table 2.** The properties of these VCVS structures and the design equations for specified P and N are given in **Table 3.** The VCVS network shown in Fig. 3 is capable of realizing equal P and N. In this case, the design equation simplifies to

$$K = K_1 = K_2 = P\,. \tag{13}$$

The error functions for these networks (assuming the 3 port mode of operation condition is satisfied) are given in **Table 4.** The compensated error functions $\varepsilon_c(s)$ in terms of P and N are also included in Table 4. The approximate remaining phase errors for the class 1 networks are given respectively by

$$\phi \simeq -\frac{P^3}{[P-(N+1)]^2}\,\frac{\omega^3}{\omega_{t1}\omega_{t2}^2} \quad \text{(Fig. 2a network)}, \tag{14a}$$

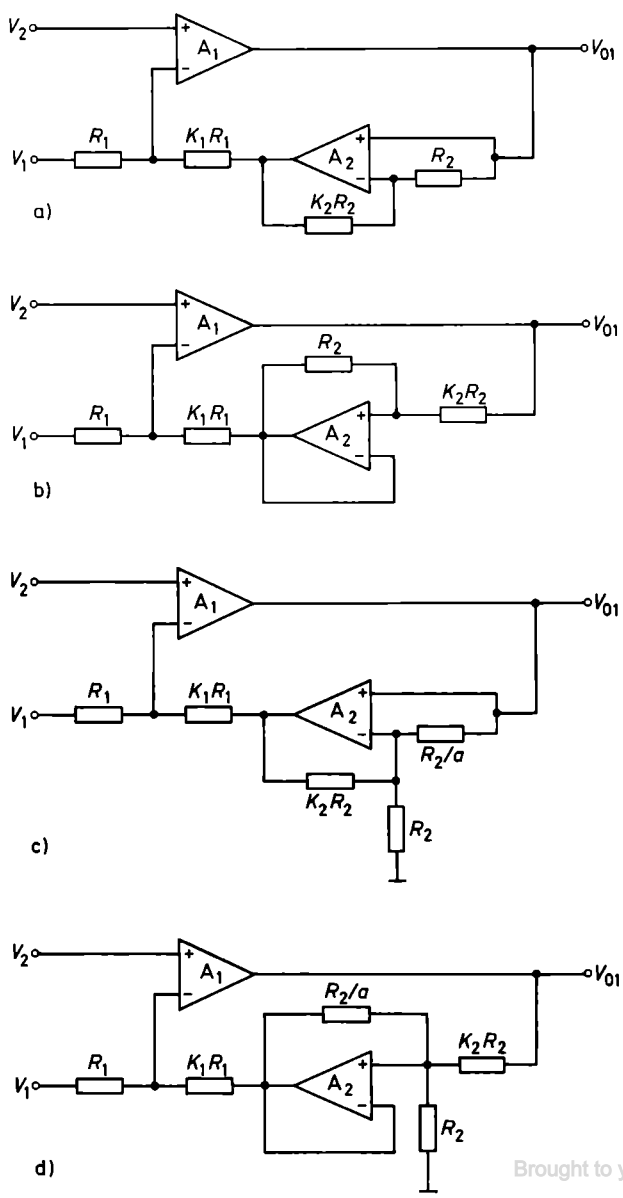
$$\phi \simeq -K_2 P[K_2 P+1]\,\frac{\omega^3}{\omega_{t1}\omega_{t2}^2} \quad \text{(Fig. 2b network)}, \tag{14b}$$

$$\phi \simeq -\frac{(N+1)^3}{[(N+1)-P]^2}\,\frac{\omega^3}{\omega_{t1}\omega_{t2}^2} \quad \text{(Fig. 3 network)}. \tag{14c}$$

It is worth noting that the 3 port VCVS networks of Fig. 2a and b include the Reddy noninverting VCVS [7] and Soliman's inverting VCVS [8] as special cases. Also the inverting VCVS reported recently in reference [9] may be generated from the circuit of Fig. 3 by setting $V_2 = 0$.

4. Class 2 – 3 port VCVS

Theorem 3: For a 3 port VCVS employing two opamps and having the generalized circuit equations as given by (2)



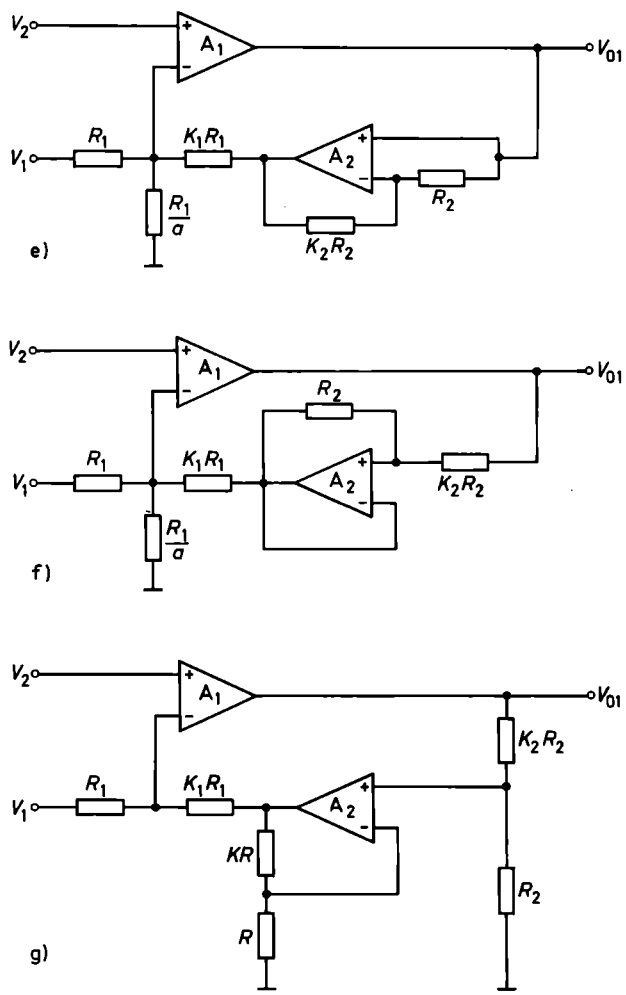


Fig. 4: Class 2 – type A, 3 port VCVS
a. Circuit 1 [2]
b. Circuit 2 [3]
c. Circuit 3
d. Circuit 4
e. Circuit 5
f. Circuit 6
g. Circuit 7

Table 3: The noninverting DC gain P, the magnitude of the inverting DC gain N, the necessary conditions for phase compensation and for 3 port mode of operation, the design equations for a specified P and N and the realizability conditions for all the 3 port VCVS structures

The 3 port VCVS				Noninverting DC Gain P	Magnitude of Inverting DC Gain N	Necessary condition for		Design Equation	Necessary realizability conditions
Class	Type	Fig.	No. of Res.			3 port mode of operation	phase* compensation		
1	A	2a	6	$K(a+1)+1$	K	$K_2+1=K_1\left(a+\frac{1}{K}\right)$	$K_2=\frac{K_1}{K}$	$K=N$ $a=\frac{P-1}{N}-1$ $K_1=\frac{N}{P-(N+1)}$ $K_2=\frac{1}{P-(N+1)}$	$P>N+1$
		2b	7	$K+1$	K	$K_3=\frac{K_1(K+1)}{K(K_2+1)-K_1}$	$K_2=\frac{K_1}{K}$	$K=N$ $K_1=NK_2$ K_2 arbitrary $K_3=K_2(K+1)$	$P=N+1$
	B	3	6	$\frac{K_2}{K_2+1}(K+1)$	K	$K_1=K_2$	—	$K=N$ $K_1=\frac{P}{(N+1)-P}$ $K_2=\frac{P}{(N+1)-P}$	$P<N+1$
2	A	4a 4b	4	K_1+1	K_1	—	$K_2=K_1$	$K_1=N$ $K_2=N$	$P=N+1$
		4c	5	$\frac{K_1+1}{K_2+1}$	$\frac{K_1}{K_2+1}$	—	$\frac{K_1+1}{K_2+1}=K_2(a+1)+1$	$K_1=\frac{N}{P-N}$ $K_2=\frac{1}{P-N}-1$ $a=\frac{(P-N)(P-1)}{1-(P-N)}-1$	$P<N+1$ $P>N+\frac{1}{P}$

		4d	5	$(K_1+1)(K_2+1)$	$K_1(K_2+1)$	—	$K_1+1=\frac{K_2(a+1)+1}{(K_2+1)^2}$	$K_1=\frac{N}{P-N}$ $K_2=P-(N+1)$ $a=\frac{(P-1)(P-N)}{P-(N+1)}$	$P>N+1$
		4e 4f	5	$K_1(a+1)+1$	K_1	—	$K_2=K_1(a+1)$	$K_1=N$ $K_2=P-1$ $a=\frac{P-1}{N}-1$	$P\geq N+1$
		4g	6	$\frac{(K_1+1)(K_2+1)}{(K+1)}$	$\frac{K_1(K_2+1)}{(K+1)}$	—	$K_1+1=\frac{(K+1)^2}{(K_2+1)}$	$K=P-1$ $K_1=\frac{N}{P-N}$ $K_2=P(P-N)-1$	$P\geq N+\frac{1}{P}$ $P>1$
	B	5a	4	K_1K_2	$(K_1+1)K_2$	—	$K_1+1=\frac{K_2+1}{K_2^2}$	$K_1=\frac{P}{N-P}$ $K_2=N-P$	$N=P+\frac{1}{N-1}$ $N\geq 1.618$
		5b	5	K_1K_2	$(K_1+1)K_2$	—	$K_1+1=\frac{K_2(a+1)+1}{K_2^2}$	$K_1=\frac{P}{N-P}$ $K_2=N-P$ $a=(N-1)-\frac{1}{(N-P)}$	$N>P$ $N\geq 1.618$
		5c	5	K_1K_2	$[K_1(a+1)+1]K_2$	—	$K_1(a+1)+1=\frac{K_2+1}{K_2^2}$	$K_1=P(N-1)$ $K_2=\frac{1}{N-1}$ $a=\frac{N}{P}-\frac{1}{P(N-1)}-1$	$N>P+\frac{1}{N-1}$ $N\geq 1.618$
		5d	6	$\frac{K_1K_2(K_3+1)}{K_3-K_2}$	$\frac{(K_1+1)K_2(K_3+1)}{K_3-K_2}$	—	$\frac{(K_1+1)(K_3+1)}{K_3-K_2}=\frac{K_2+1}{K_2^2}$	$K_1=\frac{P}{N-P}$ $K_2=\frac{1}{N-1}$ $K_3=\frac{1+N-P}{(N-P)(N-1)-1}$	$N>P+\frac{1}{N-1}$ $N\geq 1.618$

* For class 2 it is assumed that matched operational amplifiers are used.

Table 4: The error function for all the 3 port VCVS structures

The VCVS Figure	The error function*	The compensated error function in terms of P & N $\varepsilon_c(s)$
2a	$\dfrac{1+[K_1+K_2+1]\dfrac{1}{A_2}}{1+K_2[K(a+1)+1]\dfrac{1}{A_2}+[K(a+1)+1][K_1+K_2+1]\dfrac{1}{A_1A_2}}$	$\dfrac{1+\left[\dfrac{P}{P-(N+1)}\right]\dfrac{s}{\omega_{t2}}}{1+\left[\dfrac{P}{P-(N+1)}\right]\dfrac{s}{\omega_{t2}}+\left[\dfrac{P^2}{P-(N+1)}\right]\dfrac{s^2}{\omega_{t1}\omega_{t2}}}$
2b	$\dfrac{1+\dfrac{K_3(K_1+K_2+1)}{K_3+1}\dfrac{1}{A_2}}{1+K_2(K+1)\dfrac{1}{A_2}+(K+1)(K_1+K_2+1)\dfrac{1}{A_1A_2}}$	$\dfrac{1+K_2P\dfrac{s}{\omega_{t2}}}{1+K_2P\dfrac{s}{\omega_{t2}}+[K_2P+1]\dfrac{s^2}{\omega_{t1}\omega_{t2}}}$
3	$\dfrac{1+\dfrac{K_1(K_2+1)}{K_2}\dfrac{1}{A_2}}{1+(K_1+1)\dfrac{1}{A_2}+(K_1+1)(K+1)\dfrac{1}{A_1A_2}}$	$\dfrac{1+\left[\dfrac{N+1}{(N+1)-P}\right]\dfrac{s}{\omega_{t2}}}{1+\left[\dfrac{N+1}{(N+1)-P}\right]\dfrac{s}{\omega_{t2}}+\left[\dfrac{(N+1)^2}{(N+1)-P}\right]\dfrac{s^2}{\omega_{t1}\omega_{t2}}}$
4a 4b	$\dfrac{1+(K_2+1)\dfrac{1}{A_2}}{1+(K_1+1)\dfrac{1}{A_1}+(K_1+1)(K_2+1)\dfrac{1}{A_1A_2}}$	$\dfrac{1+P\dfrac{s}{\omega_{t1}}}{1+P\dfrac{s}{\omega_{t1}}+P^2\left(\dfrac{s}{\omega_{t1}}\right)^2}$
4c	$\dfrac{1+[K_2(a+1)+1]\dfrac{1}{A_2}}{1+\left[\dfrac{K_1+1}{K_2+1}\right]\dfrac{1}{A_1}+\dfrac{(K_1+1)[K_2(a+1)+1]}{(K_2+1)}\dfrac{1}{A_1A_2}}$	
4d	$\dfrac{1+\dfrac{[K_2(a+1)+1]}{(K_2+1)}\dfrac{1}{A_2}}{1+(K_1+1)(K_2+1)\dfrac{1}{A_1}+(K_1+1)[K_2(a+1)+1]\dfrac{1}{A_1A_2}}$	
4e 4f	$\dfrac{1+(K_2+1)\dfrac{1}{A_2}}{1+[K_1(a+1)+1]\dfrac{1}{A_1}+[K_1(a+1)+1][K_2+1]\dfrac{1}{A_1A_2}}$	
4g	$\dfrac{1+(K+1)\dfrac{1}{A_2}}{1+\left[\dfrac{(K_1+1)(K_2+1)}{(K+1)}\right]\dfrac{1}{A_1}+(K_1+1)(K_2+1)\dfrac{1}{A_1A_2}}$	
5a	$\dfrac{1+\dfrac{K_2+1}{K_2}\dfrac{1}{A_2}}{1+K_2(K_1+1)\dfrac{1}{A_1}+(K_1+1)(K_2+1)\dfrac{1}{A_1A_2}}$	$\dfrac{1+N\dfrac{s}{\omega_{t1}}}{1+N\dfrac{s}{\omega_{t1}}+N^2\left(\dfrac{s}{\omega_{t1}}\right)^2}$
5b	$\dfrac{1+\left[\dfrac{K_2(a+1)+1}{K_2}\right]\dfrac{1}{A_2}}{1+K_2(K_1+1)\dfrac{1}{A_1}+(K_1+1)[K_2(a+1)+1]\dfrac{1}{A_1A_2}}$	
5c	$\dfrac{1+\dfrac{K_2+1}{K_2}\dfrac{1}{A_2}}{1+K_2[K_1(a+1)+1]\dfrac{1}{A_1}+[K_1(a+1)+1](K_2+1)\dfrac{1}{A_1A_2}}$	
5d	$\dfrac{1+\dfrac{K_2+1}{K_2}\dfrac{1}{A_2}}{1+\dfrac{K_2(K_1+1)(K_3+1)}{K_3-K_2}\dfrac{1}{A_1}+\dfrac{(K_1+1)(K_2+1)(K_3+1)}{K_3-K_2}\dfrac{1}{A_1A_2}}$	

* For class 1 it is assumed that the 3 port mode of operation condition is satisfied.

with $b_{11}=0$ and with (4) being satisfied, the necessary condition for phase compensation is given by

$$\frac{a_{21}}{a_{11}}=\frac{b_{22}}{b_{12}}+\frac{b_{21}}{b_{22}}\frac{\omega_{t1}}{\omega_{t2}}. \tag{15}$$

Proof: From (5), setting $b_{11}=0$ and using (3) and (4) thus

$$V_{01}=\left[V_1\frac{a_{11}b_{22}-a_{21}b_{12}}{b_{12}b_{21}}+V_2\frac{a_{12}b_{22}-a_{22}b_{12}}{b_{12}b_{21}}\right]\varepsilon(s) \tag{16}$$

where

$$\varepsilon(s)=\frac{1+\dfrac{a_{11}}{a_{21}b_{12}-a_{11}b_{22}}\dfrac{s}{\omega_{t2}}}{1+\dfrac{b_{22}}{b_{12}b_{21}}\dfrac{s}{\omega_{t1}}+\dfrac{-1}{b_{12}b_{21}}\dfrac{s^2}{\omega_{t1}\omega_{t2}}}. \tag{17}$$

From the above equation, it is seen that the necessary condition for phase compensation is given by (15), and the theorem is proved.

The phase compensation condition in this case depends on the unity gain bandwidth of both opamps. Thus it is recommended to use matched opamps with this group of amplifiers.

Examining (4), (16) and (17), it is seen that by taking the coefficients a_{21} and a_{22} to be zero the VCVS networks obtained will always satisfy the necessary condition for the 3 port mode of operation. In this special case (defined here as a class 2), the generalized expression for the output voltage is given by

$$V_{01}=\left[V_1\frac{a_{11}b_{22}}{b_{12}b_{21}}+V_2\frac{a_{12}b_{22}}{b_{12}b_{21}}\right]\varepsilon_2(s) \tag{18}$$

where

$$\varepsilon_2(s)=\frac{1+\dfrac{-1}{b_{22}}\dfrac{s}{\omega_{t2}}}{1+\dfrac{b_{22}}{b_{12}b_{21}}\dfrac{s}{\omega_{t1}}+\dfrac{-1}{b_{12}b_{21}}\dfrac{s^2}{\omega_{t1}\omega_{t2}}}. \tag{19}$$

From the above equations, the coefficient signs are obtained and it is found that two types of networks may be defined, and the results are given in Table 1.

For the class 2 VCVS structures and assuming matched opamps are used, the phase compensation condition reduces to

$$b_{22}{}^2+b_{12}b_{21}=0. \tag{20}$$

Fig. 4 represents seven circuits which belong to the class 2 – type A. The two equivalent circuits of Fig. 4a and b have been reported in [2–3]. From Table 4 it is clear that the approximate phase and magnitude errors for any of the class 2 – type A networks is given by

$$\left.\begin{aligned}\phi&\simeq -P^3\left(\frac{\omega}{\omega_{t1}}\right)^3\\ \gamma&\simeq P^2\left(\frac{\omega}{\omega_{t1}}\right)^2\end{aligned}\right\}\ \omega\ll\frac{\omega_{t1}}{P}. \tag{21}$$

The bandwidth can be easily obtained from the phase compensated error function and is given by

$$BW=1.817\frac{\omega_{t1}}{P}. \tag{22}$$

Fig. 5 includes four of the class 2 – type B VCVS networks. The circuit of Fig. 5b is the three port generalization of the inverting VCVS network reported in [10]. From the compensated error function given in Table 4, the approximate

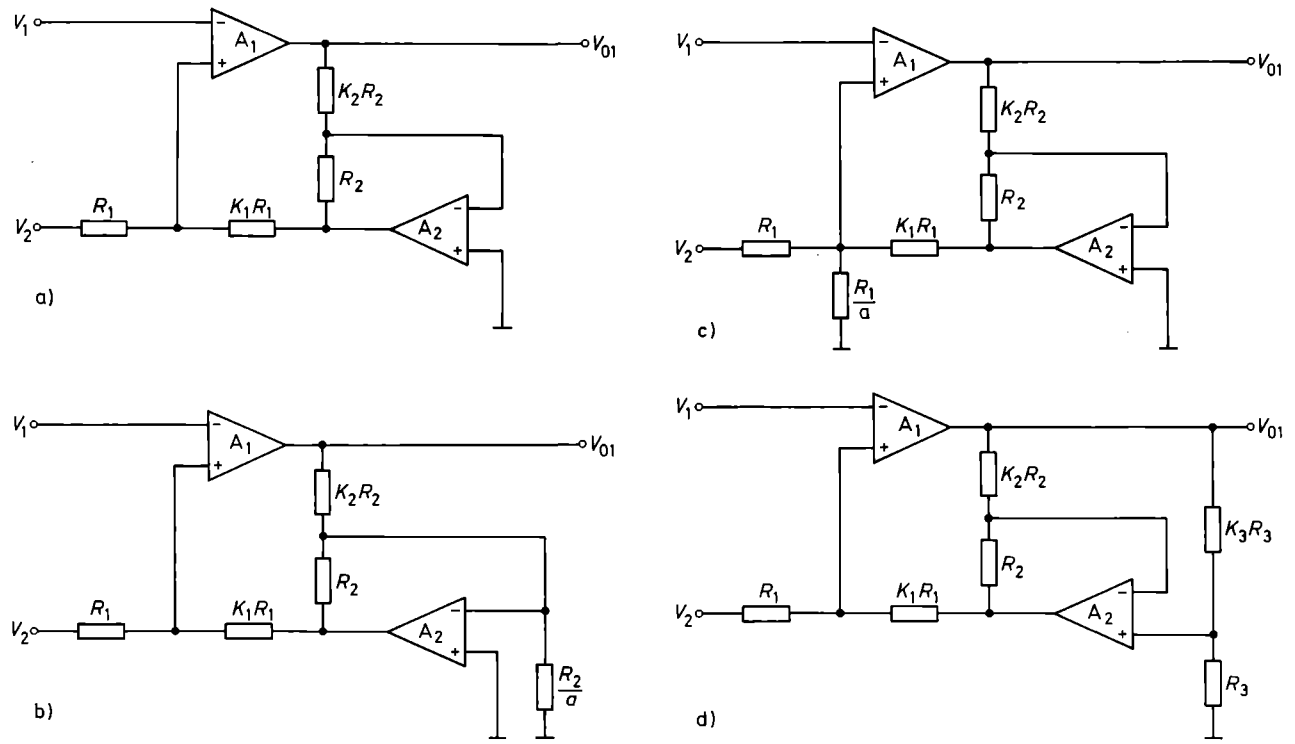


Fig. 5: Class 2 – type B, 3 port VCVS

a. Circuit 1
b. Circuit 2 [10–11]
c. Circuit 3
d. Circuit 4

phase and magnitude errors and the realizable bandwidth for any of the class 2 – type B networks are given by

$$\left.\begin{aligned}\phi &\simeq -N^3\left(\frac{\omega}{\omega_{t1}}\right)^3\\ \gamma &\simeq N^2\left(\frac{\omega}{\omega_{t1}}\right)^2\end{aligned}\right\}\ \omega \ll \frac{\omega_{t1}}{N} \qquad (23)$$

$$BW = 1.817\,\frac{\omega_{t1}}{N}\,. \qquad (24)$$

It should be noted that the class 2 – type B networks are restricted to an inverting gain of magnitude ≥ 1.618.

From (22) and (24) it is clear that, in realizing a noninverting (inverting) VCVS, the class 2 – type A (type B) networks provide a larger gain bandwidth product than the class 2 – type B (type A) networks.

5. Conclusions

A design procedure for realizing a phase compensated 3 port VCVS with specified noninverting and inverting DC gains is given. Two classes are defined in this paper. In the class 1 VCVS networks, the phase compensation condition is independent of the gain bandwidth of the two opamps employed in the circuit. For the class 1–3 port VCVS, three circuits are given, the first is suitable for realizing $P>(N+1)$, the second is restricted to $P=(N+1)$ and the third realizes $P<(N+1)$. The properties of each circuit and the design equations for specified P and N are summarized in Tables. The class 2–3 port VCVS networks defined in this paper meets the necessary condition for the 3 port mode of operation without any further restriction on the circuit components as in the class 1 case. In the class 2 however the phase compensation condition depends on the gain bandwidth of both opamps employed in the circuit. Eleven 3 port VCVS networks which belong to class 2 are given in this paper. The circuits of Fig. 4a, b and 5a include 4 resistors only, thus they have only two design parameters K_1 and K_2. To fulfill the necessary phase compensation condition together with the DC gain requirements, a definite relation between P and N exists in both cases. For the circuits of Fig. 4a and b, $P=N+1$, whereas for the circuit of Fig. 5a; $P=N-\frac{1}{N-1}$, $(N\geq 1.618)$. Of course it is possible to realize $P=N$ using these circuits by adding a potential divider at the noninverting (inverting) input port for the circuits of Fig. 4a and b (for the circuit of Fig. 5a). Note however that the circuit of Fig. 3 is the only VCVS network having $P=N$ (using only 2 opamps + 6 resistors) and with a phase compensation condition independent of the gain bandwidth of both opamps. Another 3 port VCVS network having $P=N$ and with a phase compensation condition independent of the gain bandwidth of the opamps may be obtained from the circuit of Fig. 2a by adding a potential divider at the noninverting input; in this case however the circuit uses 8 resistors. It is worth noting that all the circuits reported in this paper with exception of those in Fig. 2b and 3 have infinite input impedance at one of the two input ports.

Generalization of the class 2 VCVS networks to noninverting and inverting weighted summers is possible [3]. For the class 1 circuits however the VCVS of Fig. 2a may be generalized to noninverting weighted summers and that of Fig. 3 may be generalized to inverting weighted summers [9] only.

The networks reported in this paper include several noninverting [6, 7] and inverting VCVS structures as special cases [12]. More circuits may be generated and are not included here to limit the length of the paper (especially for the case $b_{11}=0$, and nonzero a_{21} and a_{22}). In some of the circuits reported here, the second opamp output V_{02} may provide some useful response.

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Neues aus Forschung, Industrie und Wirtschaft

Optische Nachrichtenübertragung im Wellenlängenmultiplex

Für künftige zusätzliche Dienste in der Telekommunikation ist die Technik mit dem Lichtwellenleiter und seiner immensen Übertragungskapazität bestens gerüstet. Dennoch macht man sich in den Siemens-Forschungslabors schon heute eifrig Gedanken über die Mehrfachausnutzung solcher Leitungen – angeregt auch durch die Förderung des Bundesministeriums für Forschung und Technologie. Die Ingenieure entwickeln derzeit beispielsweise optische Komponenten für ein vielversprechendes Wellenlängenmultiplexverfahren. Es basiert auf neuartigen Bausteinen, die es ermöglichen, modulierte Strahlung mehrerer Lichtquellen verschiedener Wellenlängen gleichzeitig über eine einzige Glasfaser zu senden. Und das auch im bidirektionalen Betrieb.

Die Funktion der linsenlosen Multiplex-Bausteine beruht auf einem aus mehreren Schichten bestehenden, selektiven Interferenzfilter, das im Hochvakuum auf eine schräg polierte Glasfaserstirnfläche aufgedampft wird. Die Fasern sind im Baustein zur Fixierung und Justierung in V-förmigen Furchen von Silizium-Substraten geführt, die zwischen Glaskörpern eingekittet sind. Als Sender dienen Lumineszenzdioden im infrarotnahen Bereich, wobei mit einem Kanalabstand von 70 nm die ersten Experimente gemacht wurden. Im 2-Kanal-Betrieb mit zwei Multiplex-Bausteinen ergab sich dabei ein gesamter Einfügeverlust von 4 dB und eine Fern-Nebensprechdämpfung von 30 dB bei unidirektionaler Übertragung. Im bidirektionalen Einsatz betrug die Nah-Nebensprechdämpfung 60 dB.