Faculty of Engineering – Cairo University
Electronics and Electrical Engineering Department
EECE2020 – Electronics II
Problem Set # 1

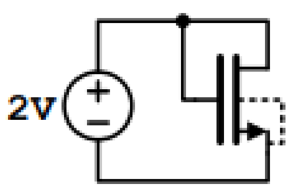
Unless otherwise specified, use the parameters from the following table for all problems.

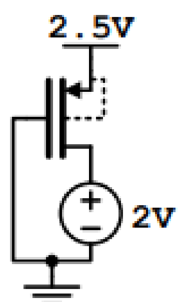
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \; and \; \epsilon_{ox} = 3.9\epsilon_o$$

Parameter	NMOS	PMOS	Units
$\lvert V_{th} \rvert$	0.7	0.8	V
λ	0.1	0.2	V^{-1}
μ_o	350	100	$\frac{cm^2}{V.sec}$
t_{ox}	9	9	nm

Problem 1.1: Determine what region of operation (cutoff, linear, or saturation) each of the following circuits is operating in.

a)

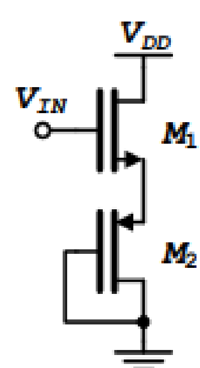




b) For an NMOS with VDS = 0.5V, what are the ranges of VGS voltages in which the device operates in the cutoff, linear, and saturation regions?

c) For an NMOS with VGS = 1V, what are the ranges of VDS voltages in which the device operates in the cutoff, linear, and saturation regions?

Problem 1.2: For the circuit on the right, answer the following questions. Ignore channel length modulation. $(W/L)_1 = (W/L)_2 = 1.0/0.5$.

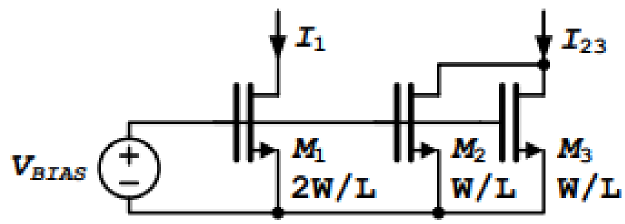


a) What is the maximum value of VIN that biases M1 in the saturation region with VDD = 5V?

b) What is the region of operation of each device when VDD = 5V and VIN = 3V?

c) What is the current through each device when VDD = 5V and VIN = 3V?

Problem 1.3: Using parallel transistors is better from a device matching perspective than varying the width of a transistor. This isn't always apparent when using simplified models of the devices. Ignore channel length modulation for all parts.



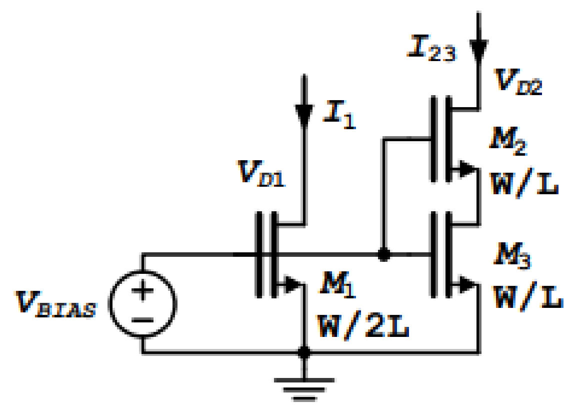
NOTE: The body terminals are not shown on these devices. This style is commonly used to show gate terminals connected across devices.

a) Calculate the currents I_1 and I_{23} for the circuit on the right. Assume VBIAS = 1V, VDS = 2V for all devices, $(W/L)_1 = 2.0/0.5$, and $(W/L)_2 = (W/L)_3 = 1.0/0.5$.

b) Are the 2 currents in part a) the same or different? Briefly explain why.

c) Suppose you needed to generate a third current I_{OUT} that is $2.5 \cdot I_{23}$ using any number of NMOS devices, but with the size of each NMOS restricted to W/L = 1.0/0.5. VGS and VDS are the same as in part a). Draw a schematic of how you could implement this?

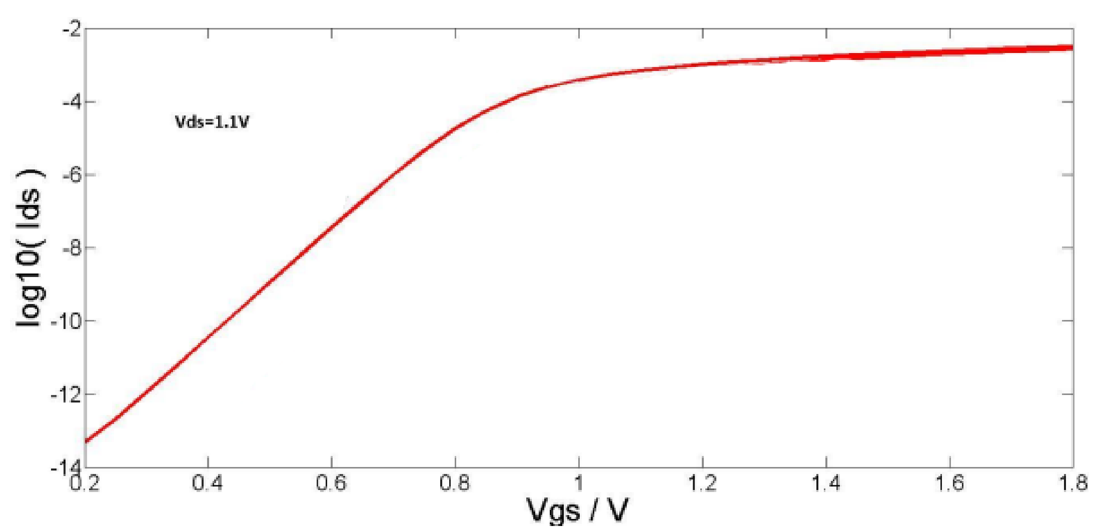
Problem 1.4: Stacking transistors and increasing length are techniques used to increase the output impedance and reduce leakage current through devices. You may ignore channel length modulation.



a) Calculate the currents I_1 and I_{23} for the circuit on the right. Assume VBIAS = 1V, VD1 = VD2 = 2V, $(W/L)_1 = 1.0/1.0$, and $(W/L)_2 = (W/L)_3 = 1.0/0.5$. Body terminals on all devices are connected to the ground. (Hint: assume an operating region for M2 and M3, calculate the current and voltages, then check your operating region assumption)

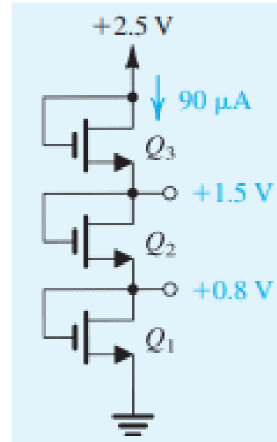
b) Are the 2 currents in part a) the same or different?

Problem 1.5: The figure below shows the measured log (I_D) vs V_{GS} curve of an NMOS transistor. Assume the sub-threshold current can be approximated with $I_D = I_0 \exp \frac{VGS-VTH}{nV_T}$ where thermal voltage VT = 26mV. Estimate the value of "n" for this transistor.



Problem 1.6: The NMOS transistors in the circuit on the right have Vt = 0.5 V, μnCox = 250 μA/V2 , λ = 0, and $L_1 = L_2 = L_3 = 0.5$ μm.

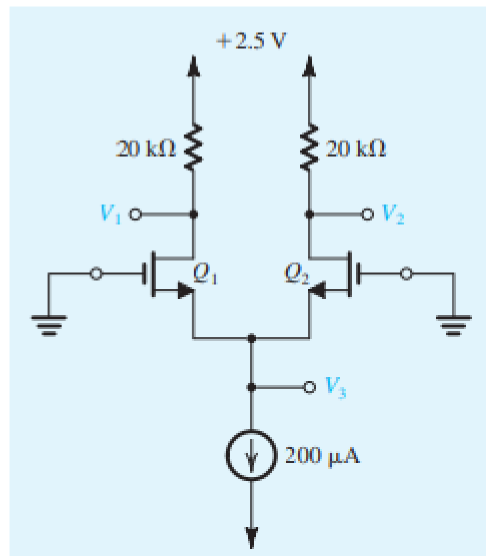
Find the required values of gate width for each all transistors to obtain the voltage and current values indicated.



Problem 1.7: 1 In the circuit shown on the right, transistors Q1 and Q2 have Vt = 0.7 V, and the process transconductance parameter μnCox =125 μA/V2. Find V1, V2, and V3 for each of the following cases:

(a) $(W/L)_1 = (W/L)_2 = 20$

(b) $(W/L)_1 = 1.5(W/L)_2 = 20$



Problem 1.8: For the circuits shown below, assume μnCox = 3μpCox = 270 μA/V2, |Vt|=0.5V, λ = 0, L = 1 μm, and W = 3 μm, unless otherwise specified. Find the labeled currents and voltages.