ELC2020

Electronics I

MOSFET Devices

Lecture (2)

Dr. Omar Bakry

omar.bakry.eece@gmail.com

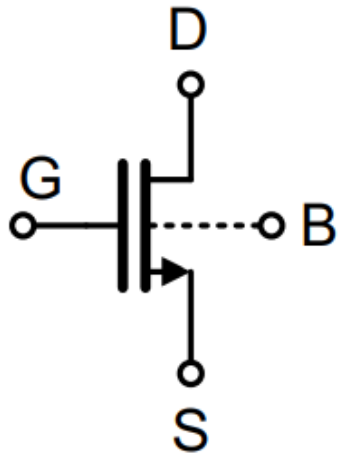
Department of Electronics and Electrical Communications

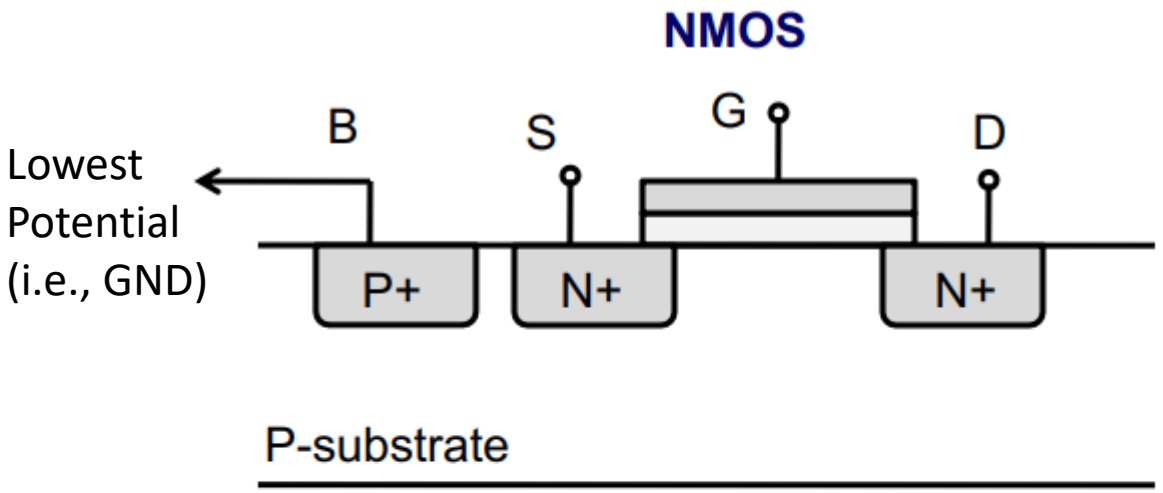
Faculty of Engineering

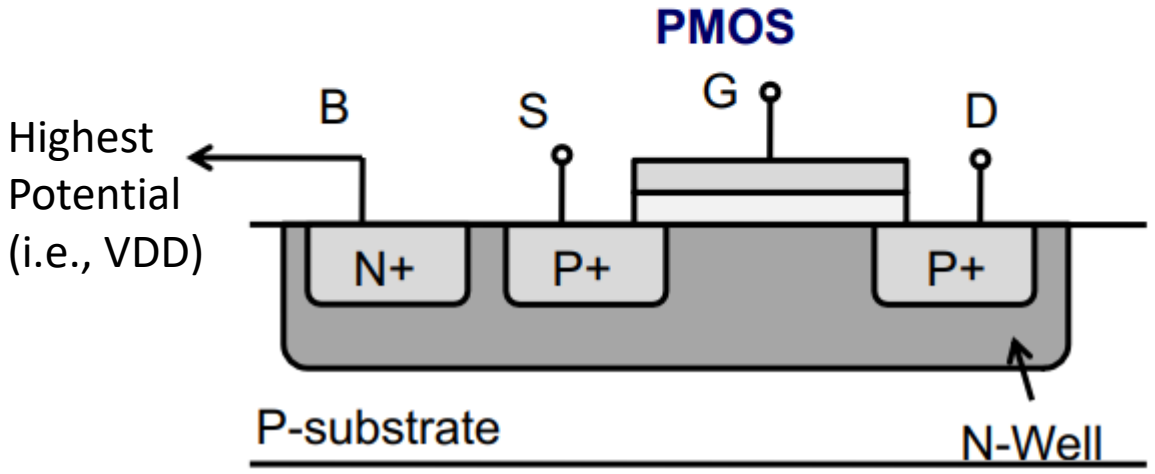
Cairo University

Fall 2023

NMOS vs PMOS





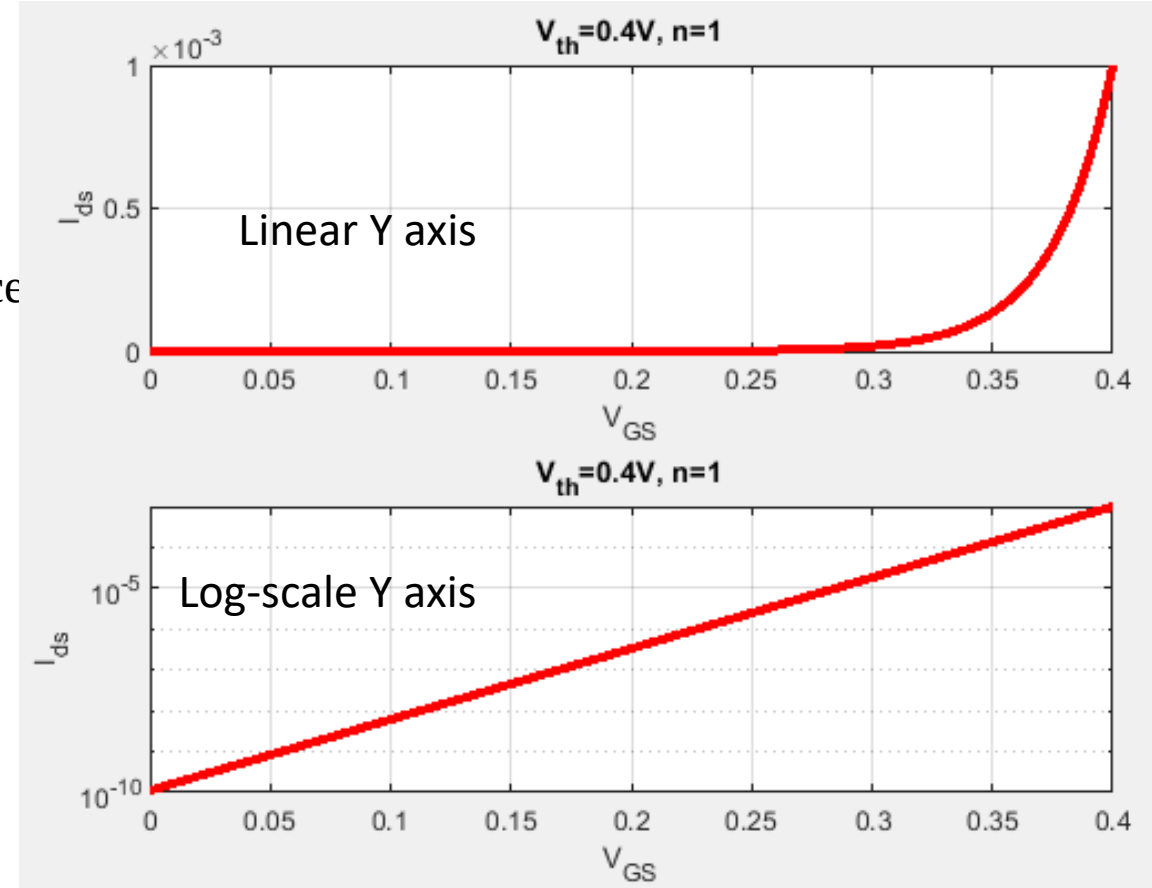


- Two polarities of FETs: NMOS and PMOS
- Body potentials (p-substrate and N-Well) should reverse-bias all P-N junctions
  - We don't want current to flow through the substrate (BULK)

The Threshold Voltage V_{th}

- Threshold voltage (V_{th}) is the value of V_{GS} at which a sufficient number of electrons accumulate in the channel → strong inversion
  - V_{th} is +ve for NMOS and -ve for PMOS.
- V_{th} range is 0.2V – 0.7V in modern technologies (typically ~0.4V).
  - **High V_{TH} (HVT), Regular V_{TH} (RVT), and Low V_{TH} (LVT), Ultra-low V_{TH} (ULVT)**

- When $V_{GS} < V_{th}$
  - This region is called sub-threshold region
  - Channel weak inversion
  - Small exponential current flows from drain to source
  - $I_{ds} = I_{ds0} \times \exp\left(\frac{V_{GS}-V_{th}}{nV_T}\right)$
  - $I_{ds0} = I_{ds}|_{V_{GS}=V_{th}}$
  - $V_T = \frac{kt}{q} \sim 25mV \ @ \ room \ tempreture$



The Capacitor Charge

- The gate and the channel region forms a parallel plate capacitor with the oxide layer acting as capacitor dielectric.

- The voltage across the parallel plate capacitor must exceed V_{th} for a channel to form and be in strong inversion.

- The excess voltage of V_{GS} over V_{th} is termed the effective voltage or overdrive voltage that determines the charge in the channel $(VGS - V_{th}) = V_{ov}$

- When $V_{DS} = 0$, the voltage at every point along the channel is zero, and the voltage across the oxide is uniform and equal to V_{GS}.

The Capacitor Charge

- The charge across the parallel plate capacitor is defined as

$$Q = C \times V = C_{ox}\,(W.L) \times (V_{GS} - V_{th})$$

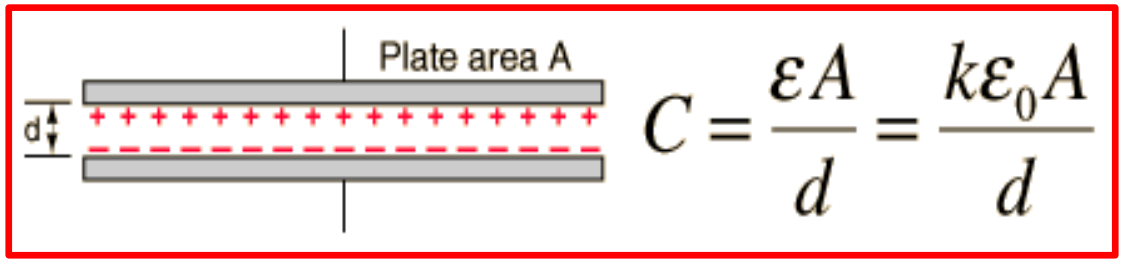
C_{ox} is the oxide capacitance per unit area

Channel width and length

$Q \propto V_{ov}$

As the over drive voltage $(V_{GS} - V_{th})$ increases, the magnitude of the charge increases.

$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} =$, where t_{ox} is the oxide thickness, $\epsilon_{ox} \sim 3.9\epsilon_o$ is the permittivity constant of silicon dioxide, and ϵ_o is the permittivity of air

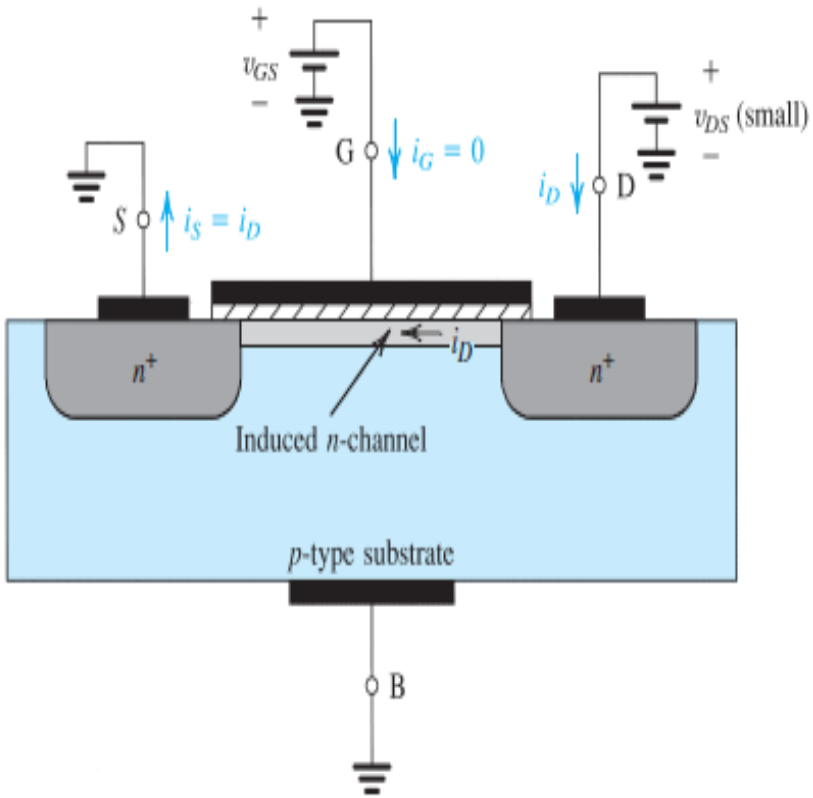


Applying a Small V_{DS} – **Uniform Channel**

- When a small +ve voltage V_{DS} between drain and source (+50mv or so) is applied, the voltage causes current to flow from drain to source opposite to electron flow.

- Since V_{DS} is small, we can assume that the voltage between the gate and various points along the channel is approximately constant and equal to ~V_{GS}.

- Therefore, we assume the channel is uniform between drain and source.



Applying a Small V_{DS} – **The Electric Field**

- The total charge of the parallel plate capacitor $Q = C_{ox}WL(V_{GS} - V_{th})$.
  - Q is proportional to $(V_{GS} - V_{th})$.
- The voltage V_{DS} establishes an electric field $|E| = \frac{V_{DS}}{L}$.
- This electric field causes electrons to move from source to drain with drift velocity v_d.
- As we know from physics $v_d = \mu_n|E| = \mu_n \frac{V_{DS}}{L}$.
- The current is defined as the total charge/unit time:

$$I_{ds} = \frac{Q}{t} = \frac{C_{ox}WL(V_{GS} - V_{th})}{t}$$

- But $\frac{L}{t} = v_d = \mu_n \frac{V_{DS}}{L}$.

Applying a Small V_{DS} – The I_{ds} Current

- $I_{ds} = \frac{C_{ox} W (V_{GS} - V_{th}) \mu_n V_{DS}}{L}$
- Rearranging,

$$I_{ds} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) V_{DS}$$

- We can write $I_{ds} = g V_{DS}$ where g is the conductance of the channel .
- $g = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})$.
- We call the term $\mu_n C_{ox} = K_n'$ which depends on fabrication process.
- The term $\frac{W}{L}$ is called the aspect ratio of the transistor.
- Let $K_n = \mathrm{K_n'} \frac{W}{L}$

Applying a Small V_{DS} – **Voltage Controlled Resistance**

- Then,

$$g = K_n(V_{GS} - V_{th}) = \frac{1}{r_{ds}}$$

where r_{ds} is the resistance between source and drain for small V_{DS}.

$$r_{ds} = \frac{1}{g} = \frac{1}{K_n(V_{GS} - V_{th})} = \frac{1}{\mu_n C_{ox} \frac{W}{L} V_{ov}}$$

- This resistance can be controlled by changing the value of $V_{ov} = V_{GS} - V_{th}$
- As we can see for small values of V_{DS}, the MOSFET can be considered as a voltage-controlled resistor .
- This region of operation is called ***linear or triode region.***

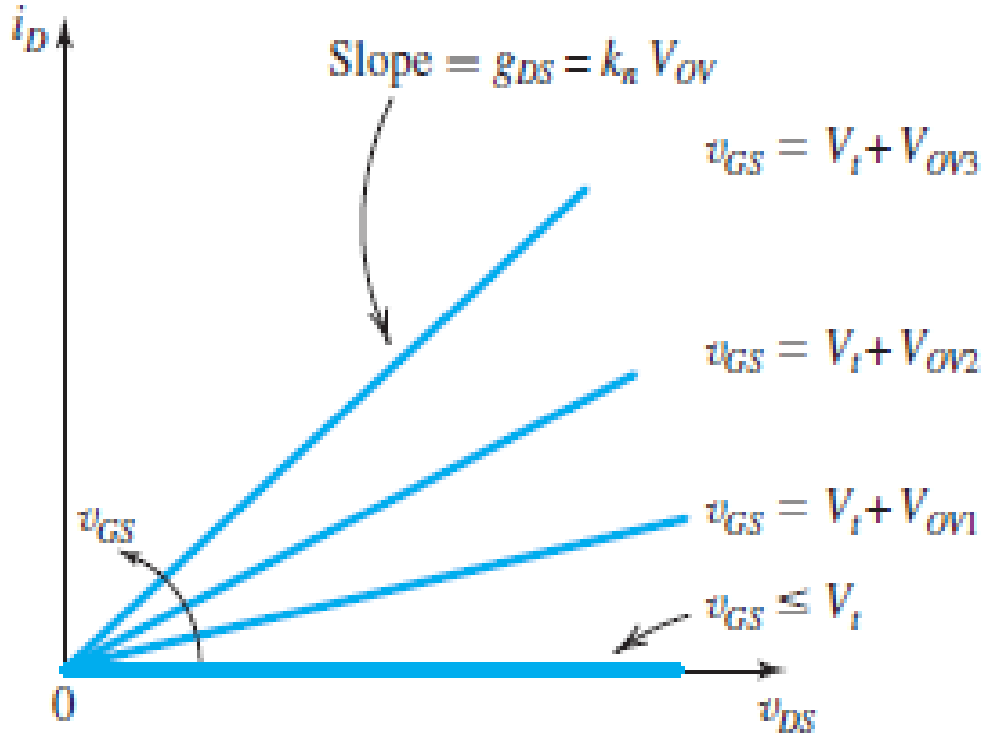
Linear/Triode Region of Operation

- This figure shows linear or triode region of operation.

- In this region the relation between the current and the voltage is linear i.e the transistor can be modeled by a linear resistance:

$$I_{ds} = \frac{V_{DS}}{r_{ds}} = K_n(V_{GS} - V_{th})V_{DS}$$

$$r_{ds} = \frac{1}{K_n(V_{GS} - V_{th})}$$



- This resistance decreases by increasing V_{GS}.

Operation as V_{DS} is increased

- For the MOSFET to conduct a current, a channel must be induced by increasing V_{GS} above the threshold voltage V_{th} (enhancement mode of operation)
- Let $V_{GS} > V_{th}$ be ***constant*** and increase V_{DS}
- V_{DS} appears as the voltage drop across the channel length.
- The voltage measured relative to the source increases from zero at the source to V_{DS} at the drain.

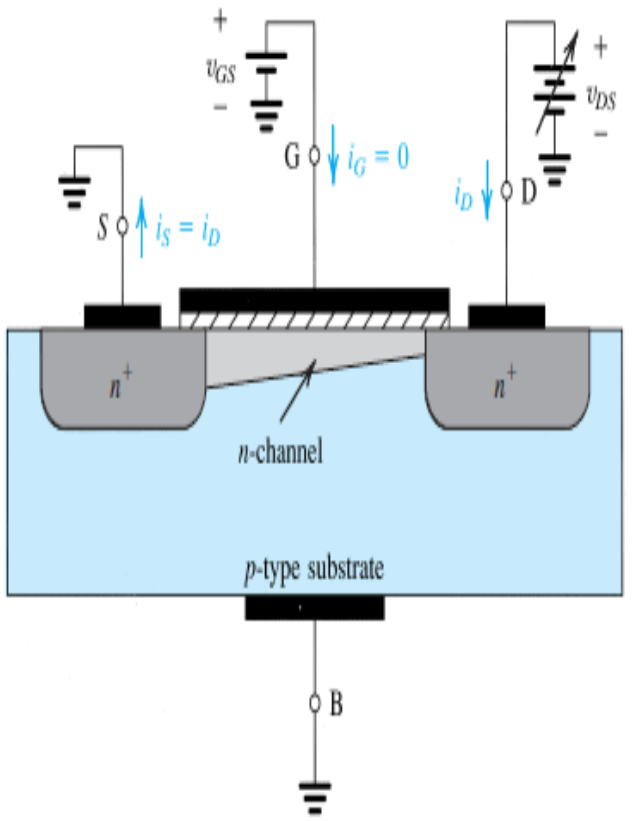


Figure 5.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value $> V_t$; $v_{GS} = V_t + V_{OV}$.

Operation as V_{DS} is increased

- The voltage between the gate and points along the channel increases from V_{GS} at the source to $V_{GD} = V_{GS} - V_{DS}$ at the drain.
- The channel is no longer uniform, it will be tapered being deepest at the source and shallowest at the drain.
- The channel depth at the source is proportional to $(V_{GS} - V_{th})$
- The channel depth at the drain is proportional to $(V_{GS} - V_{th} - V_{DS})$

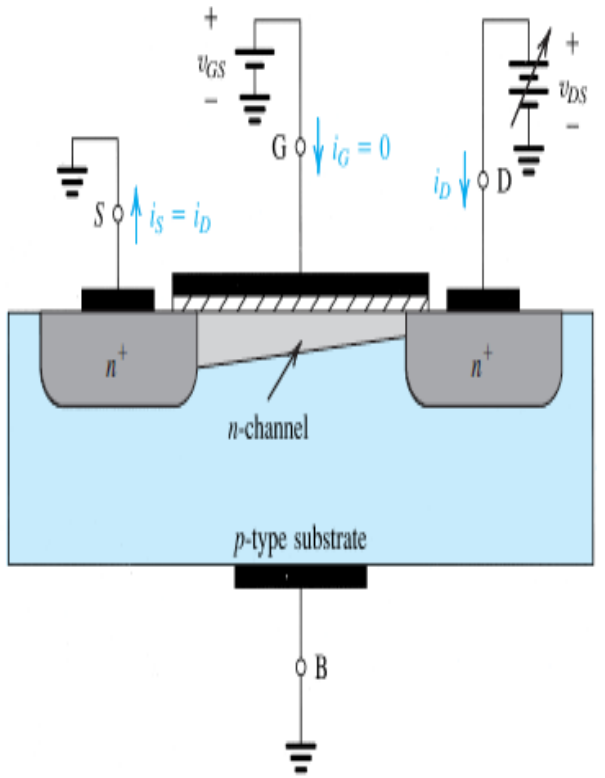


Figure 5.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value $> V_t$; $v_{GS} = V_t + V_{OV}$.

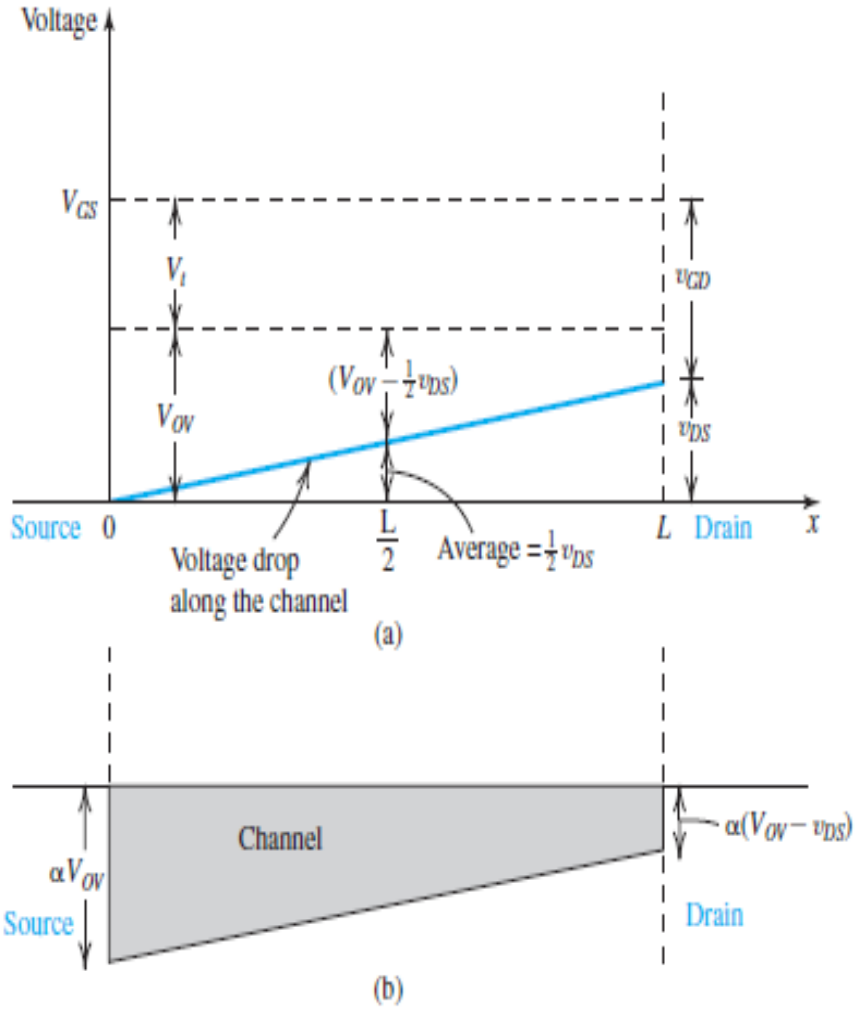
Operation as V_{DS} is increased

- Therefore, charge in this case is proportional to $(V_{GS} - V_{th} - V_{DS}/2)$

- And the current now can be written as
  $I_{ds} = K_n(V_{GS} - V_{th} - V_{DS}/2)VDS$

$$I_{ds} = K_n\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- Relationship between I_{ds} and V_{DS} is quadratic.
  - We are still in the triode region.



The Saturation Region

- As V_{DS} is increased to $V_{DS} = V_{GS} - V_{th}$, the channel depth at the drain end reduces to almost zero.

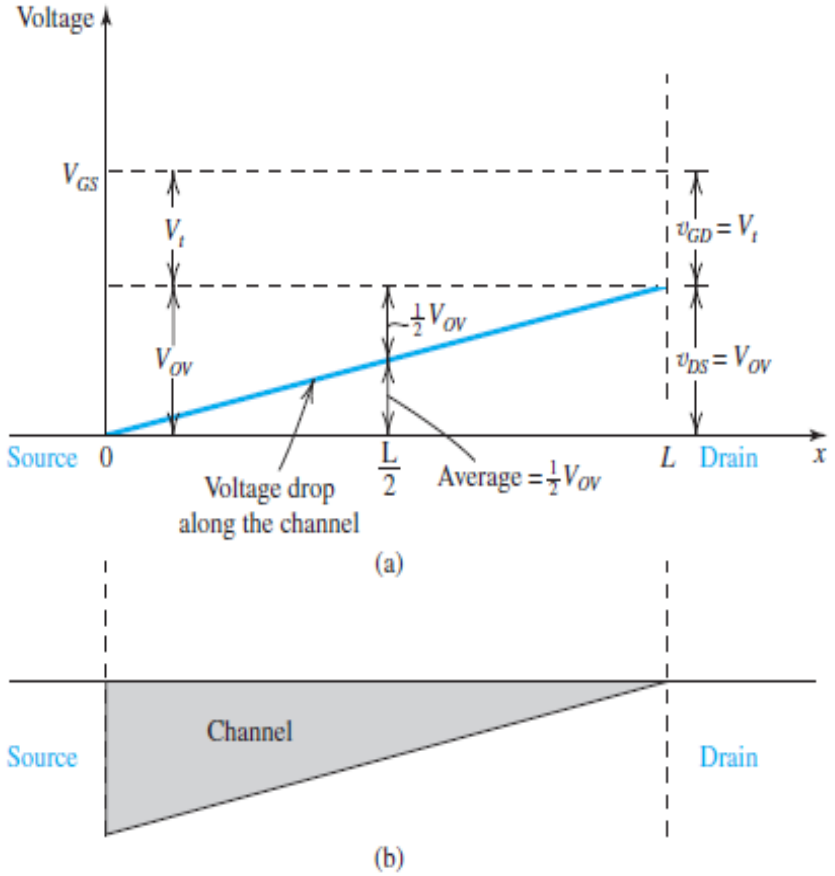


Figure 5.8 Operation of MOSFET with $v_{GS} = V_t + V_{OV}$, as v_{DS} is increased to V_{OV}. At the drain end, v_{GD} decreases to V_t and the channel depth at the drain end reduces to zero (pinch off). At this point, the MOSFET enters the saturation mode of operation. Further increasing v_{DS} (beyond $V_{Dsat} = V_{OV}$) has no effect on the channel shape and i_D remains constant.

Pinch Off – The Saturation Region Current

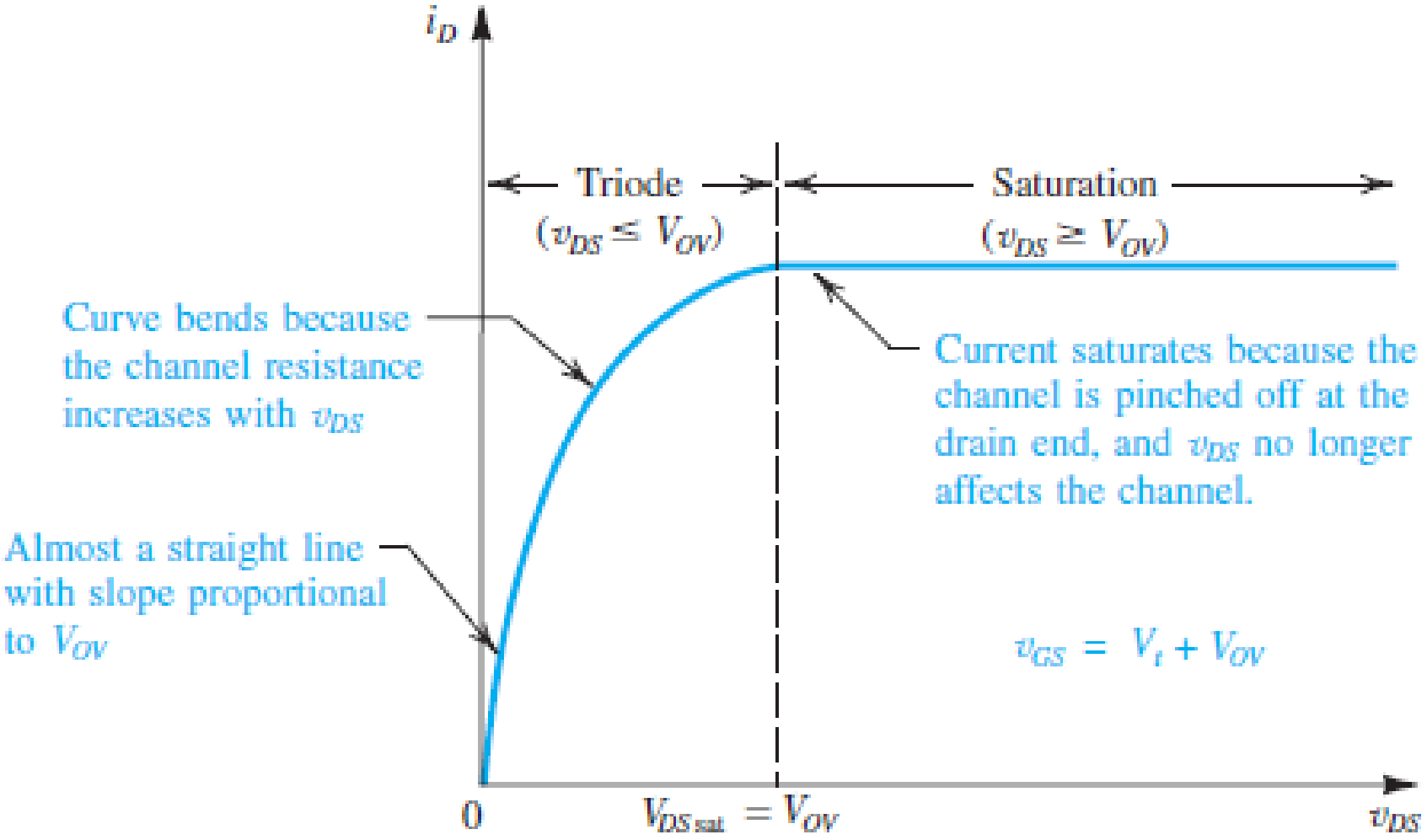
- When $V_{DS} = V_{GS} - V_{th}$, the channel is said to be pinched off at the drain.
- Increasing $V_{DS} > V_{GS} - V_{th}$ has no effect on the channel shape and the current remains constant.
- Substituting $V_{DS} = V_{GS} - V_{th}$ in the current equation results in

$$I_{ds} = \frac{K_n}{2}(V_{GS} - V_{th})^2$$

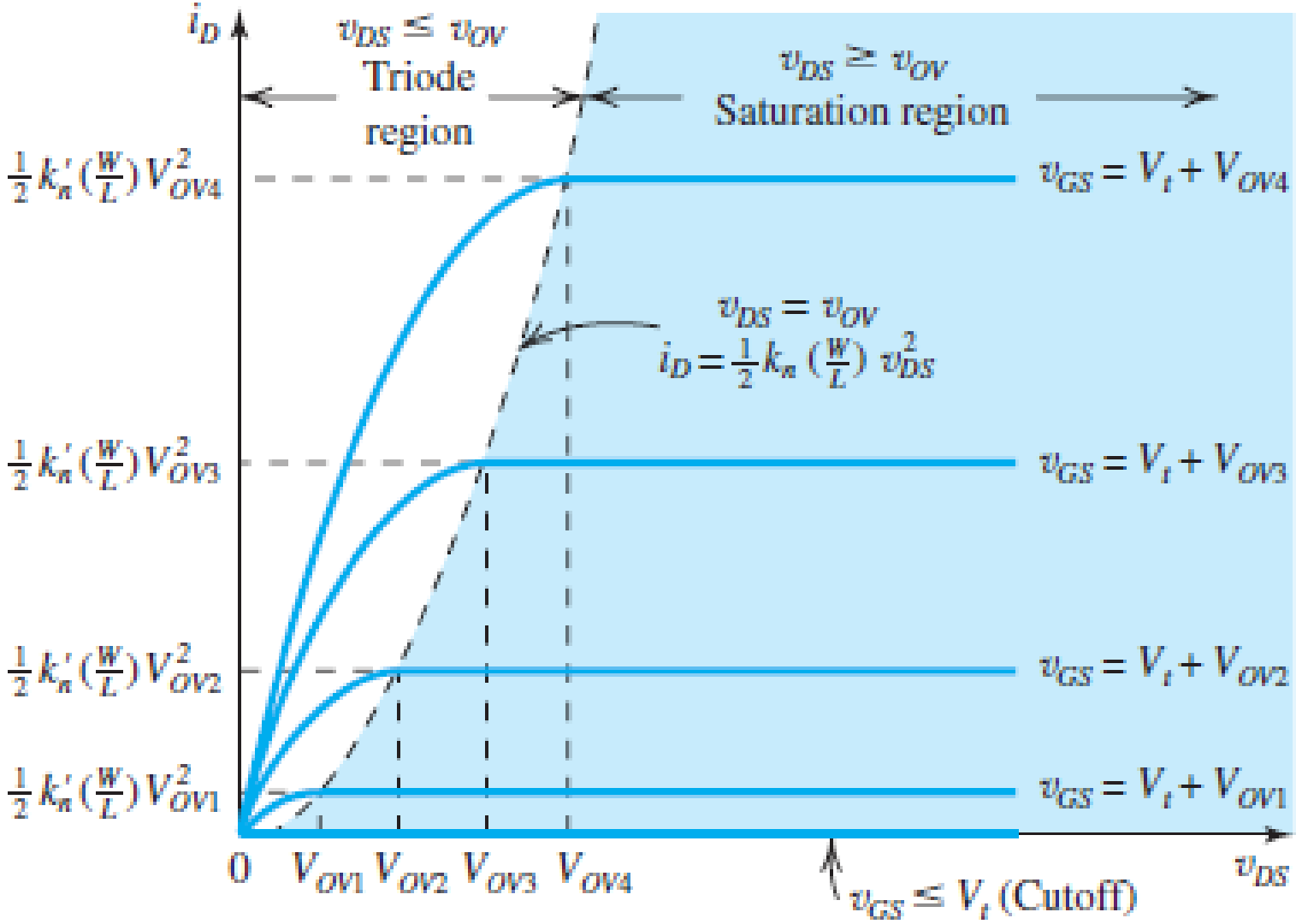
- Pinch off doesn't mean block of current it continues to flow through the channel from source to drain.

I/V Characteristics of an N Channel Enhancement MOSFET

The I_{DS} vs V_{DS} Characteristics



The I_{DS} vs V_{DS} Characteristics



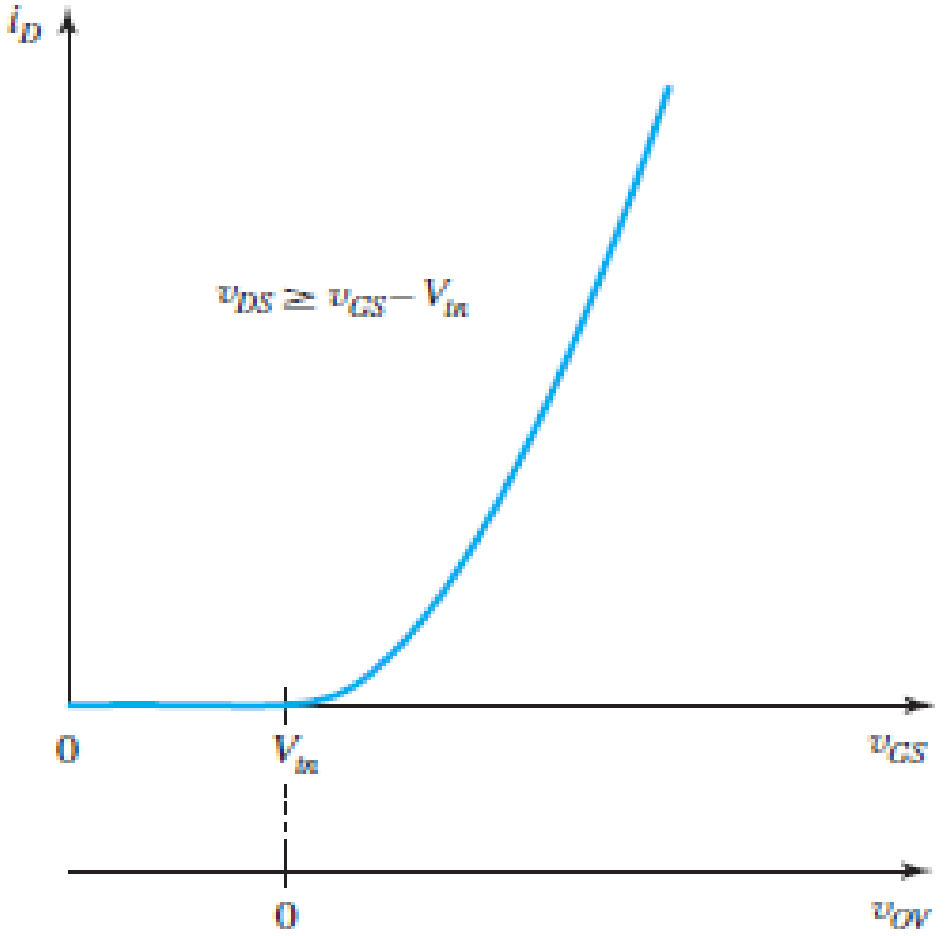
The I_{DS} vs V_{GS} Characteristics

- V_{GS} must exceed V_{th} for the channel to be created and current to flow.

- In saturation region $V_{DS} \geq V_{GS} - V_{th}$, we have quadratic current

$$I_{ds} = \frac{K_n}{2}(V_{GS} - V_{th})^2$$

- The figure shown indicates this fact.



Summary: NMOS Regions of Operation

- Large signal terminal equations

Region	V_{GS}	V_{DS}	I_{DS}
Subthreshold	$V_{GS} \leq V_{th}$	N/A	$I_{ds} = I_{ds0} \times \exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right)$
Triode	$V_{GS} > V_{th}$	$V_{DS} < V_{GS} - V_{th}$	$I_{ds} = K_n\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$
		$V_{DS} \ll V_{GS} - V_{th}$	$I_{ds} = K_n(V_{GS} - V_{th})V_{DS}$
Saturation	$V_{GS} > V_{th}$	$V_{DS} \geq V_{GS} - V_{th}$	$I_{ds} = \frac{1}{2}K_n(V_{GS} - V_{th})^2$

Example

- Consider a process technology for which $L_{min} = 0.4\mu m$, $t_{ox} = 8nm$, $\mu_n = 450cm^2/vsec$ and $V_{th} = 0.7V$

a) Find C_{ox} and K_n'.

b) For a MOSFET with $W/L = 8\mu m/0.8\mu m$, calculate the values of V_{ov}, V_{GS} and $V_{DS,min}$ needed to operate the transistor in the saturation region with a DC current $I_{DS} = 100\mu A$.

c) For the device in b find the values of V_{ov} and V_{GS} to cause the device to operate as a 1000Ω resistor for very small V_{DS}.

Solution

- $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.45\times10^{-11}}{8\times10^{-9}} = 4.32 \times 10^{-3}\ F/m^2.$

$$K_n' = \mu_n C_{ox} = 450\left(\frac{cm^2}{vsec}\right) \times 4.32 \times 10^{-3}\left(\frac{F}{m^2}\right) = 450 \times 10^{-4}\left(\frac{m^2}{vsec}\right) \times 4.32 \times 10^{-3}\left(\frac{F}{m^2}\right)$$

$$= 1.944 \times 10^{-4}\frac{A}{V^2}$$

- To operate in saturation region with $I_{DS} = 100\mu A$

$$I_{DS} = \frac{K_n'}{2}\frac{W}{L}V_{ov}^2 = 100 \times 10^{-6} = \frac{1.944 \times 10^{-4}}{2} \times \frac{8}{0.8} \times V_{ov}^2$$

$$V_{ov} = 0.32V = V_{GS} - V_{th}$$

$$V_{GS} = 0.32 + 0.7 = 1.02V.$$

$$V_{DS,min} = V_{ov} = 0.32V.$$

- $r_{ds} = V_{DS}/I_{DS} = 1/(K_n'(W/L)(V_{GS} - V_{th}))$

$$1000 = 1/(1.944 \times 10^{-4} \times 10)(V_{GS} - V_{th})$$

$$V_{ov} = V_{GS} - V_{th} = 0.51V \longrightarrow V_{GS} = 1.21V$$

Exercise

- A circuit designer intending to operate a MOSFET in SATURATION is considering the effect of changing the device dimensions and operating voltages on the drain current I_{DS}. By what factor does I_{DS} change in each of the following cases

a) The channel length is doubled.

b) The channel width is doubled.

c) The overdrive voltage is doubled.

d) The drain to source voltage is doubled.

e) Changes a,b,c,d are made simultaneously.

which of these cases might cause the MOSFET to leave saturation region?