Model Answer

Cairo University
Faculty of Engineering
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Midterm Exam – 23/11/2023
Electronics II – ELC2020
Fall Semester
Time Allowed: 1.5 hour.
Number of Pages: 9 Pages

Midterm Exam (25 points)

Name: ..... B.N.: ..... Section: .....

"I have neither given nor received unauthorized aid on this examination, nor have I concealed any violations of the Honor Code."

Signature: .....

Unless otherwise stated, in the following problems, use the device data shown in the following table and assume that ***VDD = 3V*** where necessary. All device dimensions are in microns.

Parameter	NMOS	PMOS	Units
$\|V_{th}\|$	0.7	0.8	V
λ	0.1	0.2	V^{-1}
$K' = \mu C_{ox}$	139	38	$\mu A/V^2$

Each Point +0.5

Question #1: (5 points)

Chose the correct answer for each of the following questions:

1. To reduce the channel length modulation effect (λ) of a MOS transistor,
   a) Reduce L
   b) Reduce W
   c) Increase L
   d) Increase W

2. For a MOSFET in SAT region, to keep the drain current constant while increasing the transistor's aspect ratio (W/L),
   a) Increase V_{GS}
   b) Reduce V_{ov}
   c) Reduce V_{GS}
   d) b and c

3. For a PMOS transistor in SAT region, the drain current is proportional to
   a) $V_{GS} - V_{THp}$
   b) $V_{SG} - V_{THp}$
   c) $V_{SG} + V_{THP}$
   d) $V_{SG} + |V_{THP}|$

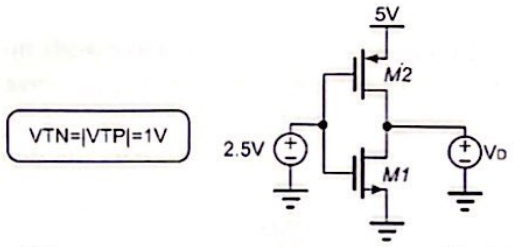
4. For a PMOS as an ON switch, the lowest R_{on} is achieved when the gate is connected to
   a) GND
   b) VDD/2
   c) VDD
   d) It depends

5. Which V_A corresponds to higher r_o?
   a) $-50V$
   b) $+50V$
   c) $-100V$
   d) $+100V$

6. For two identical transistors having a size of (W/L) and are connected in series, the effective size of the combined two transistors is:
   a) W/L
   b) $W/2L$
   c) $2W/L$
   d) $2W/2L$

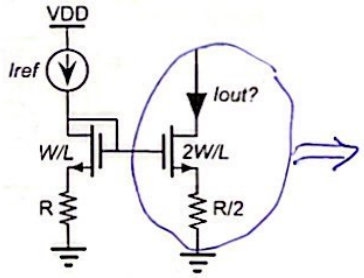
7. For the circuit shown below, the FULL range of V_D that will simultaneously bias the NMOS and PMOS in the saturation region is:

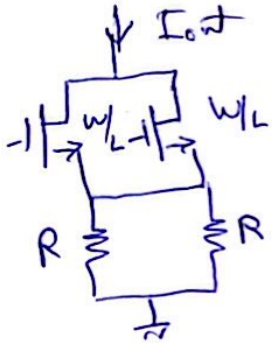
$V_{OV1} = V_{GS1} - V_{th}$
$= 2.5 - 1 = 1.5V$
$V_{OV2} = V_{SG2} - |V_{th}|$
$= (5 - 2.5) - 1 = 1.5V$
$V_{OV1} \leq V_D \leq V_{DD} - V_{OV2}$



a) $0.0 \leq V_D \leq 5.0$
b) $1.0 \leq V_D \leq 4.0$
c) $1.5 \leq V_D \leq 3.5$
d) $2.0 \leq V_D \leq 3.0$

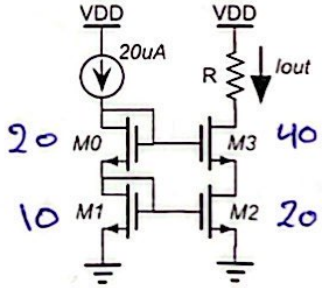
8. For the circuit shown below, assume $\lambda = 0$, I_{out} is equal to:





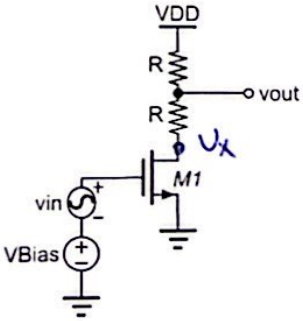
a) $0.5I_{ref}$
b) I_{ref}
c) $2I_{ref}$
d) $4I_{ref}$

9. For the cascode current mirror shown below, assume all transistors are operating in saturation. If $(W/L)_0 = (W/L)_2 = 20$ and $(W/L)_1 = 10$. What should $(W/L)_3$ be for a proper operation?



a) 10
b) 30
c) 20
d) 40

10. For the common source amplifier shown below, assume M1 is in saturation and $\lambda = 0$. The small signal gain is:

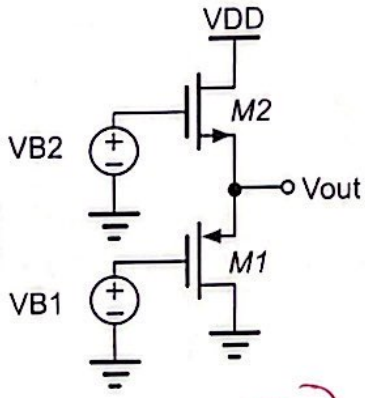


$\frac{V_x}{V_{in}} = -2g_m R$
$\frac{V_{out}}{V_x} = 1/2$
$\frac{V_{out}}{V_{in}} = -g_m R$

a) $A_v = -0.5g_m R$
b) $A_v = -g_m R$
c) $A_v = -2g_m R$
d) $A_v = -4g_m R$

Question #2: (6 points)

a) (2 Points) For the circuit shown below, derive an expression for the DC value of the V_{out} as a function of bias voltages V_{B1} and V_{B2}. Assume both transistors are in SAT, $K_p = K_n$ and $V_{THN} = |V_{THP}|$.
Ignore the channel length modulation ($\lambda = 0$).



$I_{D1} = I_{D2}$ (1)

$\frac{1}{2}K_p(V_{SG1} - |V_{thp}|)^2 = \frac{1}{2}K_n(V_{GS} - V_{th})^2$

$V_{out} - V_{B1} - |V_{thp}| = V_{B2} - V_{out} - V_{th}$

$2V_{out} = V_{B1} + V_{B2}$

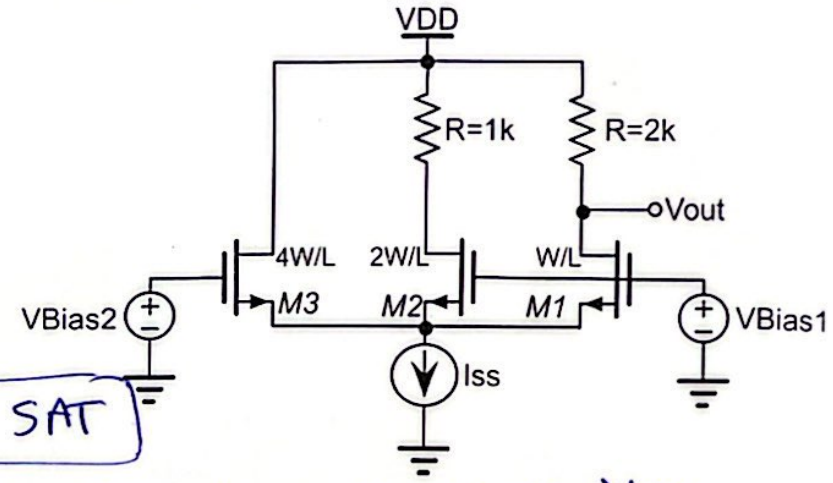
$$V_{out} = \frac{V_{B1} + V_{B2}}{2}$$ (1)

b) (4 Points) For the circuit shown below, $V_{Bias1} = V_{Bias2} = 1.6V$, $W/L = 10/0.1$ and $I_{SS} = 7mA$.

I. Calculate the DC value of V_{out}.

II. What is the voltage across I_{SS}?

Ignore the channel length modulation ($\lambda = 0$).



Assume All SAT

M_1, M_2, M_3 have the same V_{GS}

$I_D \propto (\frac{W}{L}) \Rightarrow I_{D_3} = 2I_{D_2} = 4I_{D_1} \rightarrow (I)$ (1)

$I_{D_1} + I_{D_2} + I_{D_3} = 7mA \Rightarrow (II)$

from (I) and (II) $\Rightarrow I_{D_1} = 1mA,\ I_{D_2} = 2mA,\ I_{D_3} = 4mA$

$V_{out} = V_{DD} - I_{D_1} R_1 = 3 - 1mA * 2k\Omega = 1V$ (1)

$V_{GS_1} = V_{th} + \sqrt{\frac{2I_{D1}}{K_{n1}}}$ $\quad K_{n_1} = \mu_n C_{ox} (\frac{W}{L})_1 = 13.9\ mA/V^2$

$= V_{th} + \sqrt{\frac{2}{13.9}} = 0.7 + 0.38 = 1.08V$

$V_{S_1} = V_{S_2} = V_{S_3} = V_S = V_{I_{SS}} = 1.6 - 1.08 = 0.52V$ (1)

Check Assumption of M1

$V_{DS_1} = V_{DD} - I_{D_1} R_1 - V_S$

$= 1 - 0.52 = 0.48V$

$V_{OV_1} = V_{GS_1} - V_{th} = 0.38V$

$V_{DS_1} \geq V_{OV_1}$

$\therefore$ SAT ✓

Check Assumption of M2

$V_{DS_2} = V_{DD} - I_{D_2} R_2 - V_S$

$= 3 - 2 - 0.52$

$= 0.48V$

$V_{OV_2} = 0.38V$

$V_{DS_2} \geq V_{OV_2}$

$\therefore$ SAT ✓

Check Assumption of M_3

$V_{DS_3} = V_{DD} - V_S$

$= 3 - 0.52 = 2.48$

$V_{OV_3} = 0.38V$

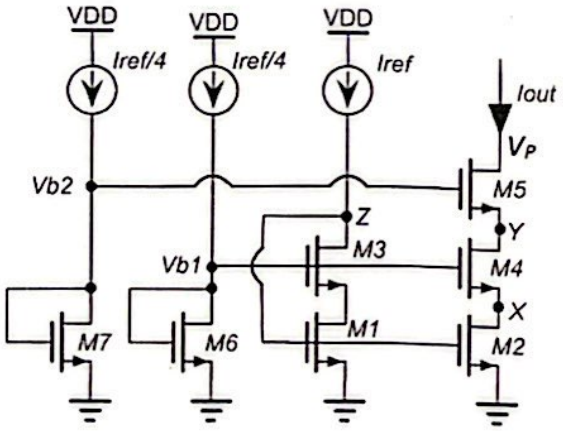
$V_{DS_3} \geq V_{OV_3}$

$\therefore$ SAT ✓ (1)

Question #3: (7 points)

For the current mirror circuit shown below, $I_{ref} = 100\mu A$. M4 and M5 double cascode the current source M2. Transistors M1 – M5 are identical having size of $W/L = 10/0.1$.
Both M6 and M7 are used to bias cascode devices.
Assume all transistors are in saturation. Consider channel length modulation.

a) What is I_{out}?
b) What is the minimum value of V_p that ensures M2, M4 and M5 are in SAT?
c) What is the optimal value of V_p that ensures there is no current mismatch between I_{out} and I_{ref}?
d) What is the optimal bias voltage V_{b1} for M3/M4?
e) What is the optimal bias voltage V_{b2} for M5?
f) What is the size of M7 $(W/L)_7$ required to generate the bias voltage V_{b2} obtained in (e)? Ignore λ in your calculations. Assume $V_{th} = 0.3V$.



a) $I_{out} = I_{ref} = 100\,\mu A$ (1)

b) $V_{p,min} = V_{ov2} + V_{ov4} + V_{ov5}$ (1.5)

c) $V_{p,opt} = V_Y + V_{ov5} = V_{GS1} + V_{ov5}$ (1)

d) $V_{b1,opt} = V_{GS3,4} + V_{ov1,2}$ (1.5)

e) $V_{b2,opt} = V_{GS5} + V_{GS7}$ (1)

f) $V_{G7} = V_{GS5} + V_{GS1} = 2V_{GS1}$

$$V_{th} + \sqrt{\frac{2 * \frac{I_{ref}}{4}}{K_{n7}}} = 2\left[V_{th} + \sqrt{\frac{2 I_{ref}}{K_{n1}}}\right]$$

$$\sqrt{\frac{I_{ref}}{2\mu_n C_{ox}\left(\frac{W}{L}\right)_7}} = V_{th} + 2\sqrt{\frac{2 I_{ref}}{K_{n1}}}$$

$\mu_n C_{ox} = 0.139\ mA/V^2$

$K_{n1} = 0.139 \times \frac{10}{0.1} = 13.9\ mA/V^2$

Continue solution of (f)

$$\sqrt{\frac{0.1}{2 * 0.139 * \left(\frac{W}{L}\right)_7}} = 0.3 + \sqrt{\frac{0.2}{13.9}}$$

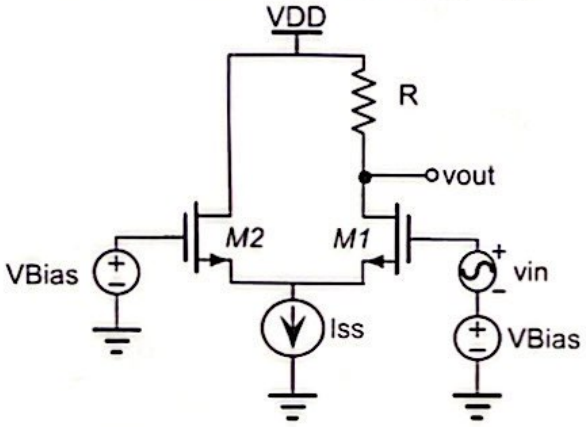
$$\left(\frac{W}{L}\right)_7 = 1.234 = \frac{0.1234}{0.1}$$

(1) #

Question #4: (7 points)

For the amplifier shown below, assume M1 and M2 are identical and in saturation.

a) What is the DC current in M1 and M2? (Ignore λ here only).
b) What is the DC voltage of V_{out}?
c) What is the configuration of this amplifier?
d) Draw the small signal model.
e) Derive an expression for the amplifier transconductance (G_m)
f) Derive an expression for the amplifier output impedance (R_{out})
g) Derive an expression for the small signal gain ($A_v = v_{out}/v_{in}$)



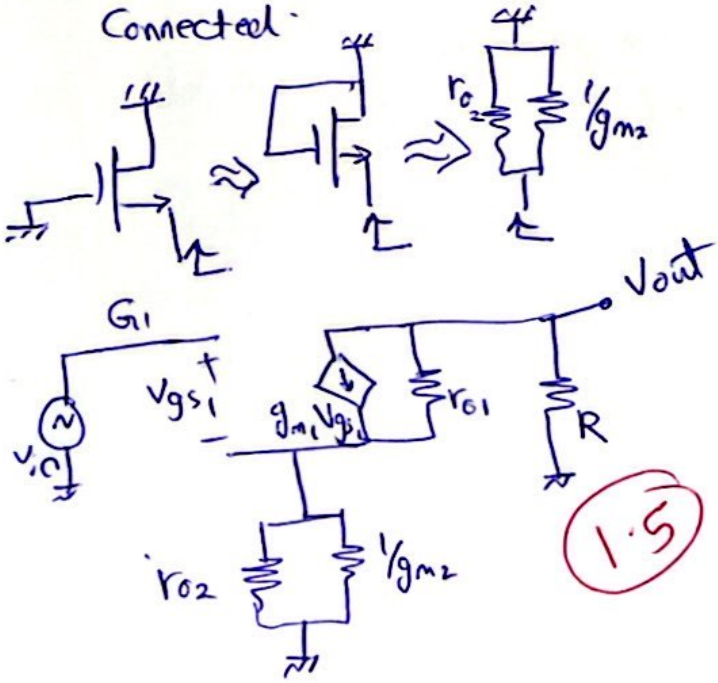
a) $I_{D_1} = I_{D_2} = \frac{I_{ss}}{2} \Rightarrow g_{m_1} = g_{m_2} = g_m$ (0.5)

(because $V_{GS_1} = V_{GS_2}$, $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$)

b) $V_{out} = V_{DD} - \frac{I_{ss}}{2} R$ (0.5)

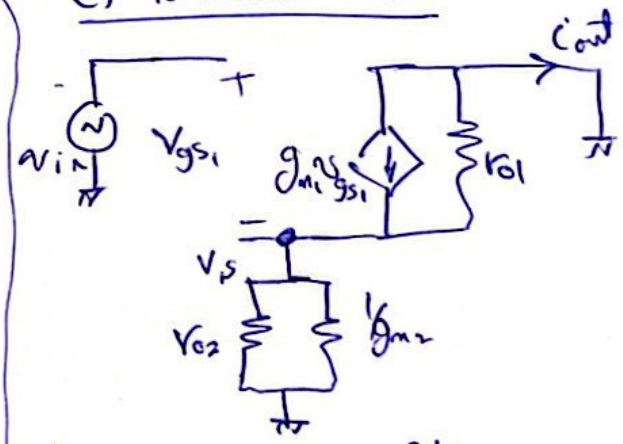
c) Common Source with degeneration and Resistive load (0.5)

d) M_2 in small signal is diode Connected.



(1.5)

e) To Calculate G_m: (1.5)



$i_{out} = -g_{m_1}V_{gs_1} + \frac{V_S}{r_{o1}}$

$V_g = v_{in}$

$V_S = -i_{out} * (r_{o2} \,||\, 1/g_{m_2})$

$i_{out}\left[1 + g_{m_1}(r_{o2} \,||\, 1/g_{m_2}) + \frac{r_{o2} \,||\, 1/g_{m_2}}{r_{o1}}\right] = -g_{m_1}$

$G_m = \frac{i_{out}}{v_{in}} = \frac{-g_{m_1}}{1 + g_{m_1}\left(r_{o_2} \,||\, \frac{1}{g_m}\right) + \frac{r_{o2} \,||\, 1/g}{r_{o1}}}$

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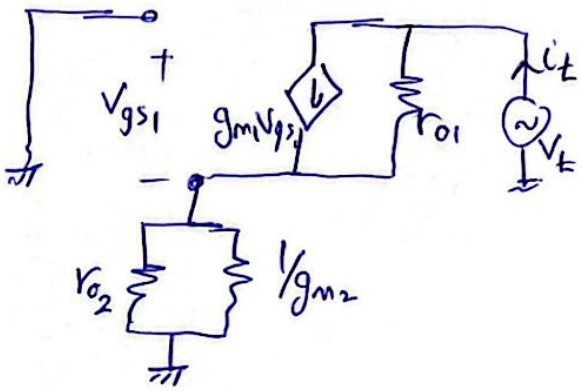
(f) To Calculate Zout: (1.5)



$$i_{t1} = g_{m1} v_{gs1} + \frac{V_t - V_s}{r_{o1}}$$

$$V_{gs1} = V_g - V_s = 0 - V_s = -V_s$$

$$V_s = i_t * (r_{o2} \,//\, 1/g_{m2})$$

$$i_{t2} = -g_{m1} V_s + \frac{v_t}{r_{o1}} - \frac{V_s}{r_{o1}}$$

$$= -g_{m1}(r_{o2} \,//\, 1/g_{m2})\, i_t - \frac{(r_{o2} \,//\, 1/g_{m2})}{r_{o1}} i_t + \frac{v_t}{r_{o1}}$$

$$i_t\left(r_{o1} + g_{m1} r_{o1} (r_{o2} \,//\, 1/g_{m2}) + (r_{o2} \,//\, \frac{1}{g_{m2}}) \right) = v_t$$

$$Z_{down} = \frac{v_t}{i_t} = r_{o1} + (r_{o2} \,//\, 1/g_{m2}) + g_{m1} r_{o1} (r_{o2} \,//\, 1/g_{m2})$$

$$Z_{out} = R \,//\, Z_{down}$$ ✓

(g) $A_V = G_m * R_{out}$ (1)

$$A_V = \frac{-g_{m1}\left[r_{o1} + (r_{o2} \,//\, \frac{1}{g_{m2}}) + g_{m1} r_{o1} (r_{o2} \,//\, 1/g_{m2}) \right]}{1 + g_{m1}(r_{o2} \,//\, 1/g_{m2}) + \frac{r_{o2} \,//\, 1/g_{m2}}{r_{o1}}}$$ #