ELC2020

Electronics II

Differential Amplifiers – Lecture 2

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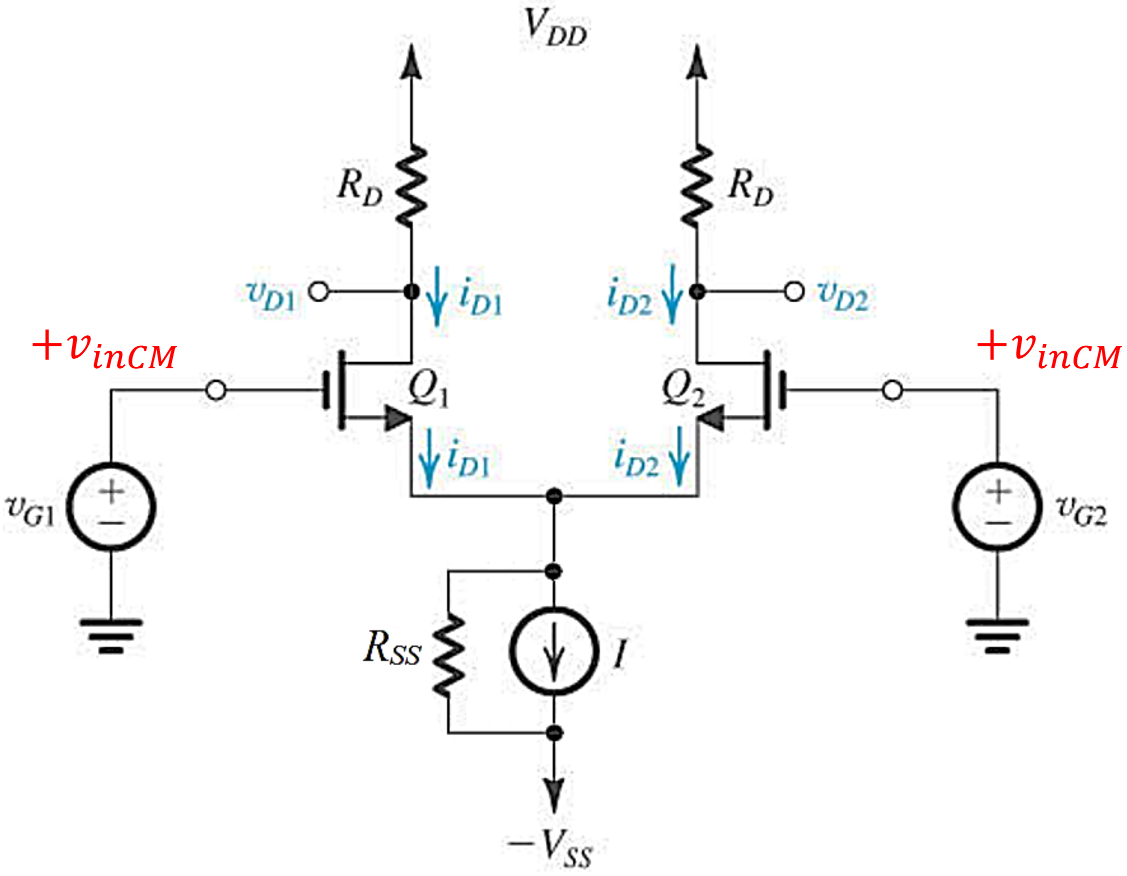
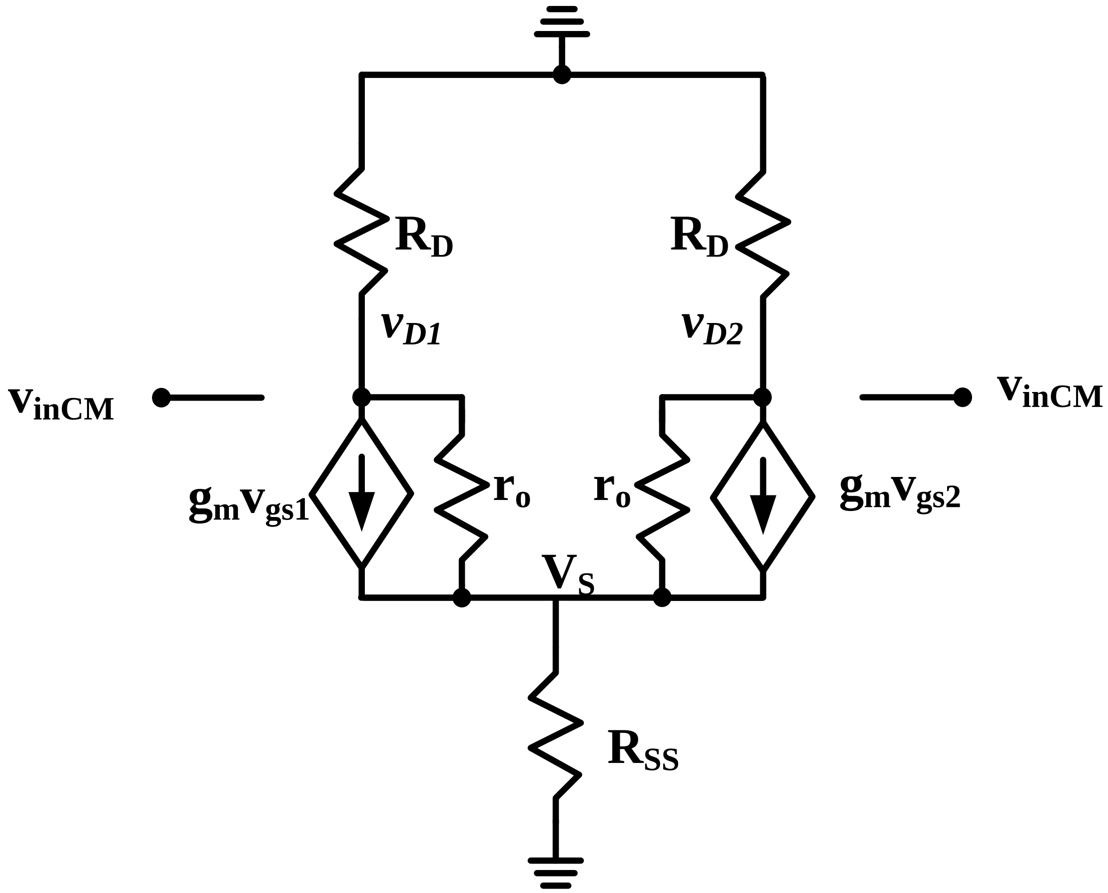
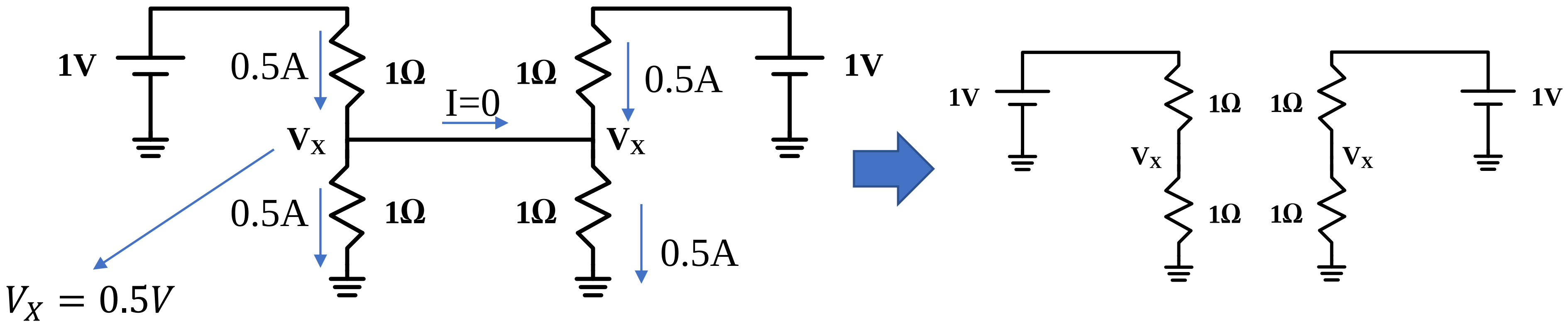
Response to AC Common Mode Signal

- Can this circuit be simplified into two half circuits



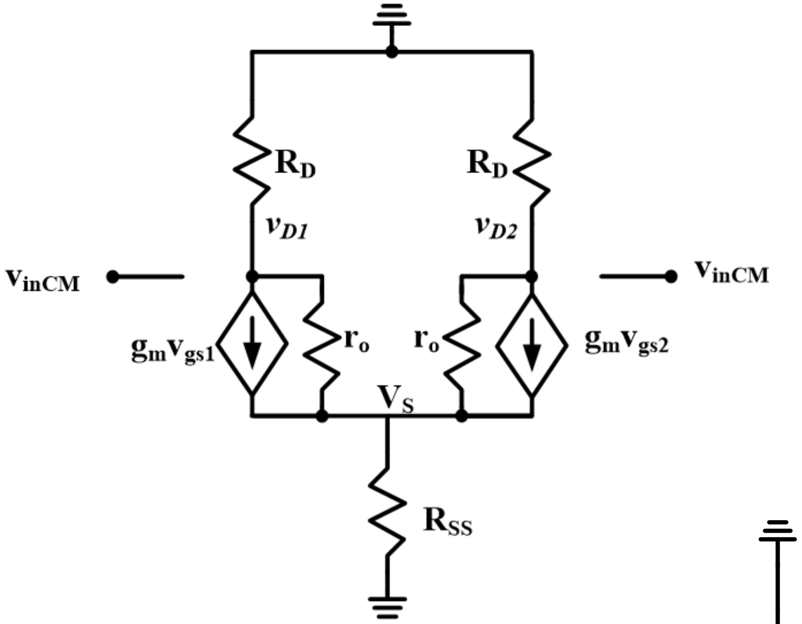


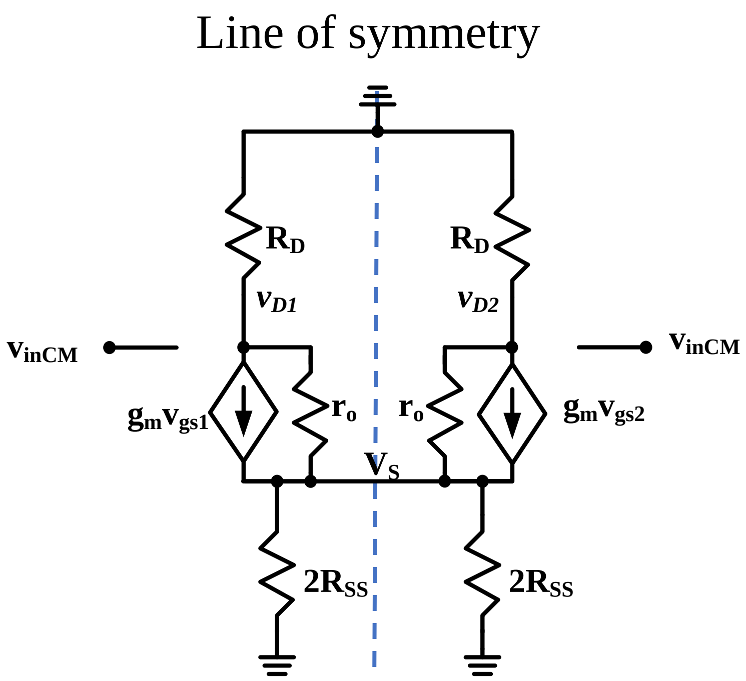
Response to AC Common Mode Signal

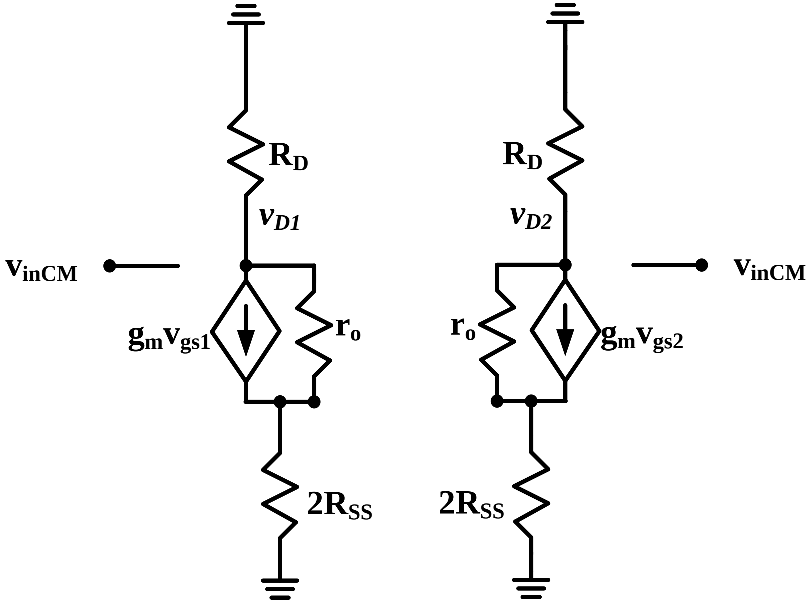


- What is the value of V_X

Response to AC Common Mode Signal







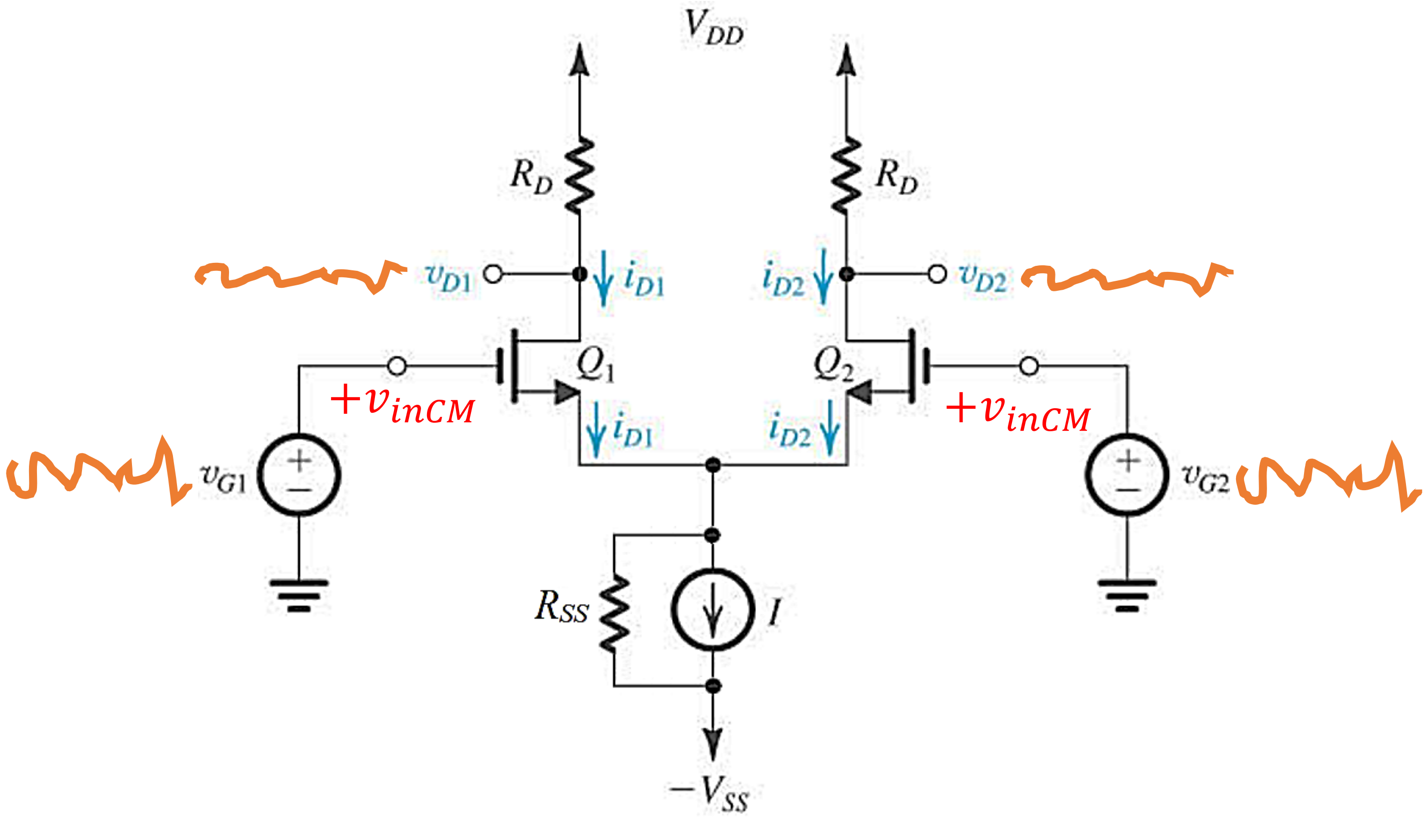
The circuit is similar to common source with source resistance

Neglecting r_o

$$v_{D1} = v_{D2} = -\frac{g_m R_D}{1 + 2 g_m R_{SS}} v_{inCM}$$

Common mode gain is typically<<1

Response to AC Common Mode Signal

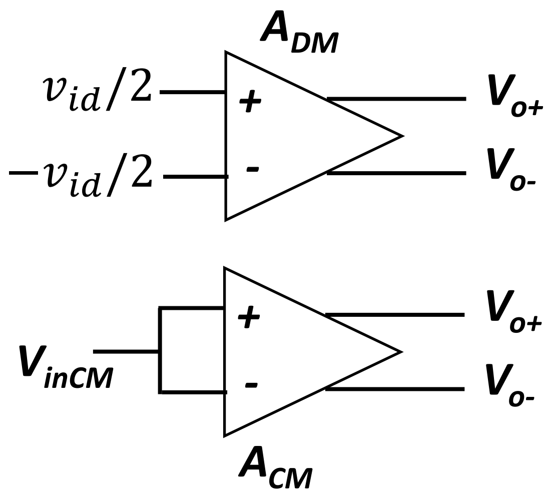


$$v_{D1} = v_{D2} = -\frac{g_m R_D v_{inCM}}{1 + 2g_m R_{SS}} \approx -\frac{R_D}{2R_{SS}} v_{inCM} \ (if\ 2g_m R_{SS} \gg 1)$$

Common Mode Rejection Ratio (CMRR)

- Being insensitive to common mode signals is one of the main advantages of the differential pair.
- CMRR is a measure of how ideal the differential pair is:

$$CMRR = \frac{|A_{DM}|}{|A_{CM}|}$$



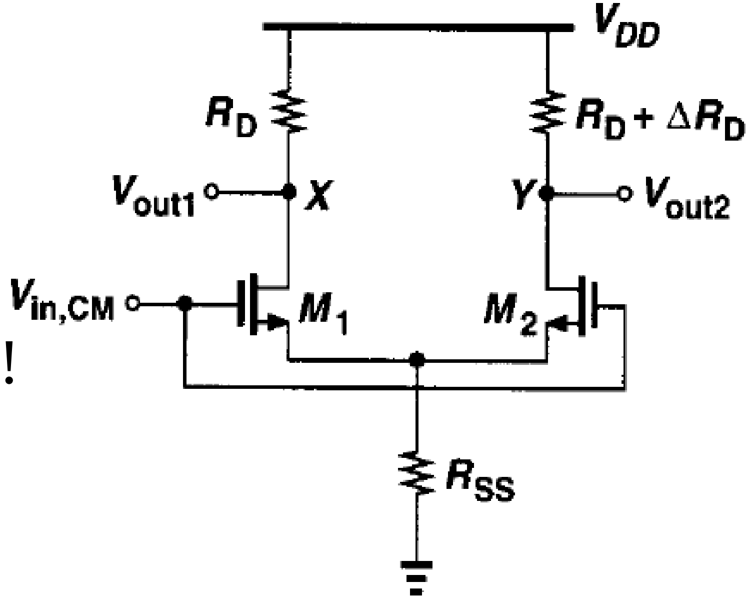
- Ideally, CMRR goes to infinity.
- Factors degrading CMRR:
  - Mismatches between MOS, Resistors, current sources, ….
  - Tail current output resistance.

CMRR: Common Mode Rejection Ratio

- As long as the circuit is symmetric CM variations remains CM
- What is the impact of common mode variations in the presence of circuit asymmetry?
- In case the resistors are mismatched due to fabrication, and neglecting the channel length modulation:

$$\frac{V_{out1}}{V_{in,CM}} = -\frac{R_D}{1/g_m + 2R_{SS}}, \frac{V_{out2}}{V_{in,CM}} = -\frac{R_D + \Delta R_D}{1/g_m + 2R_{SS}}$$

$$V_{out,DM} = V_{out1} - V_{out2} = -\frac{\Delta R_D}{1/g_m + 2R_{SS}} V_{in,CM}$$

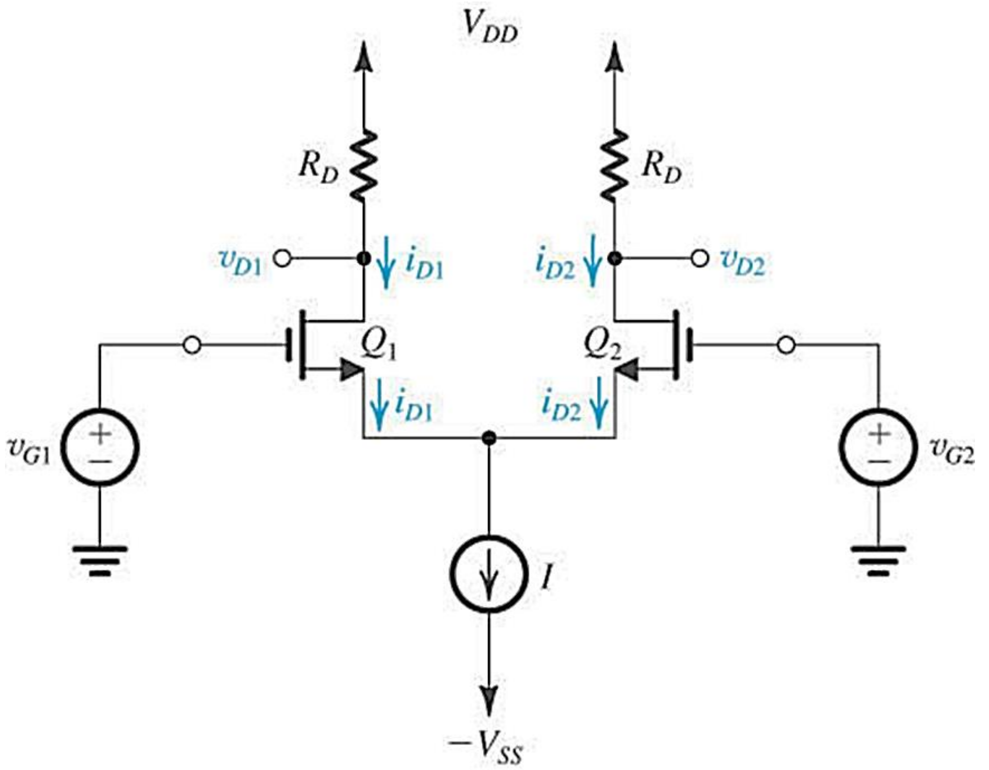


- In the presence of mismatches, input common mode variations introduce a differential component at the output!
- Could lead to input common mode noise appearing at the differential output

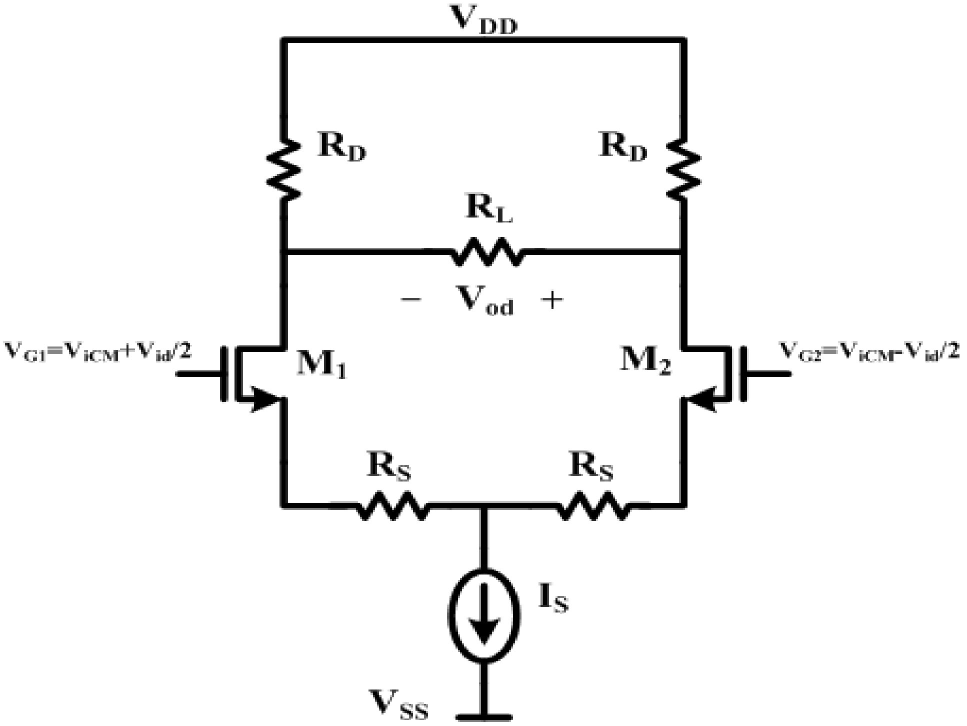
$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| = \frac{g_m R_D}{\Delta R_D/(1/g_m + 2R_{SS})} = \frac{R_D + 2g_m R_{SS} R_D}{\Delta R_D} \approx \frac{2g_m R_{SS} R_D}{\Delta R_D}$$

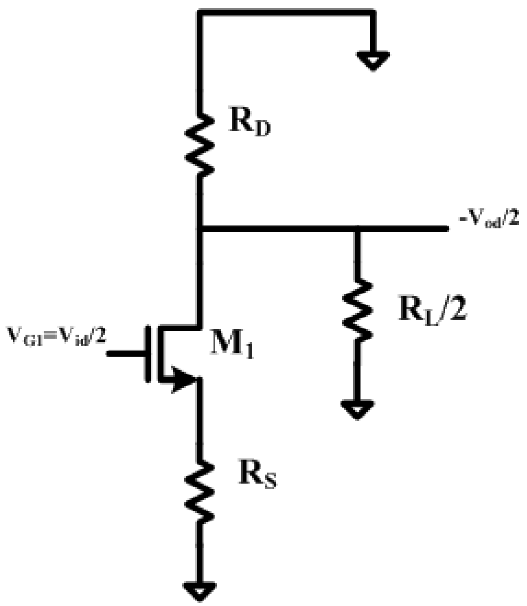
Differential Pair Summary

- Differential pair rejects common mode noise
- DC voltage is the same on both sides
- Small signal input can be written as common mode component and differential mode component (superposition can be used)
- For differential mode, source node voltage = 0V due to symmetry
- For common mode, circuit can be split into two half circuits due to symmetry (no current from left half to right half)



Half-Circuit Analysis – Example

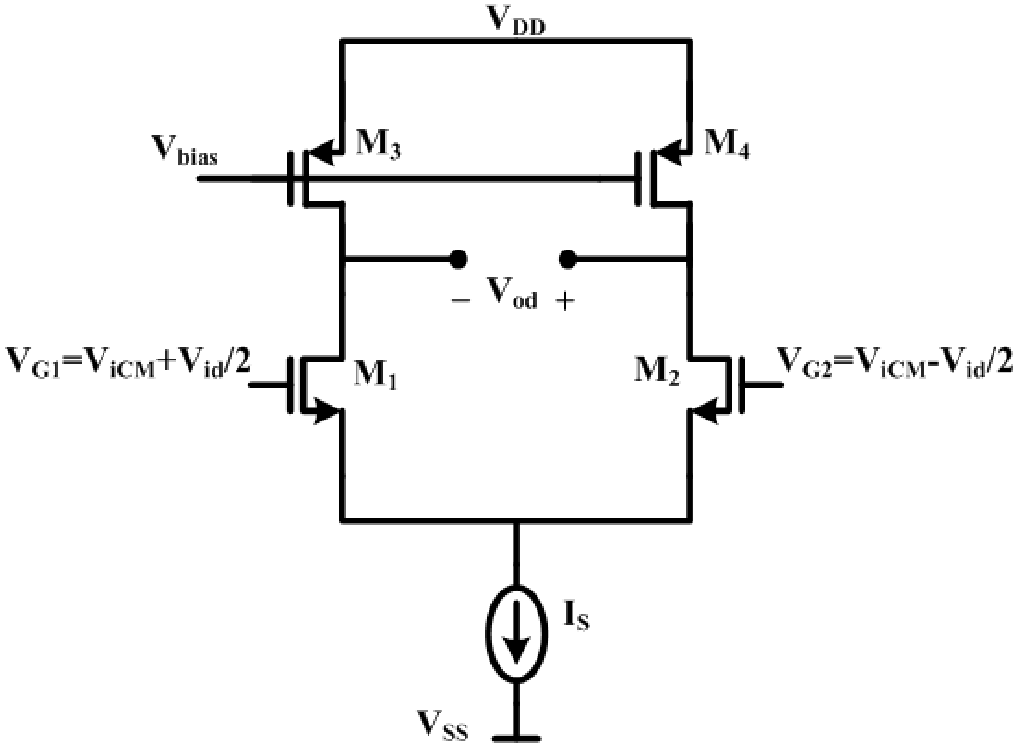


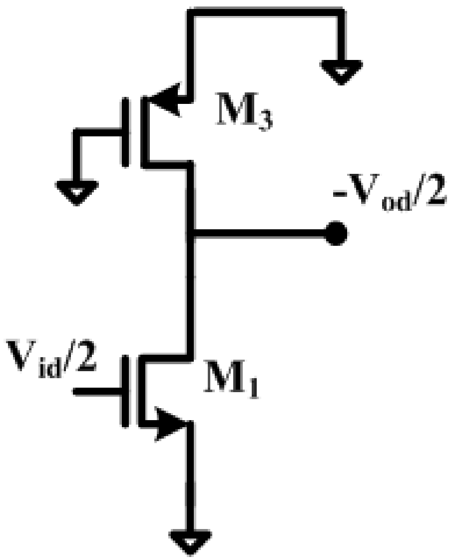


$$\frac{V_{od}}{2} = -G_m \frac{V_{id}}{2}(R_D // \frac{R_L}{2}) = -\frac{g_{m1}}{1+g_{m1}R_S}\frac{V_{id}}{2}(R_D // \frac{R_L}{2})$$

$$A_d = \frac{V_{od2} - V_{od1}}{V_{id}} = \frac{-V_{od}}{V_{id}} = \frac{g_{m1}}{1+g_{m1}R_S}(R_D // \frac{R_L}{2})$$

Current Source Load





Taking r_o into account, and assuming $r_{o1} = r_{o2}$, and $r_{o3} = r_{o4}$:

$$A_d = g_{m1}(r_{o1} // r_{o3})$$

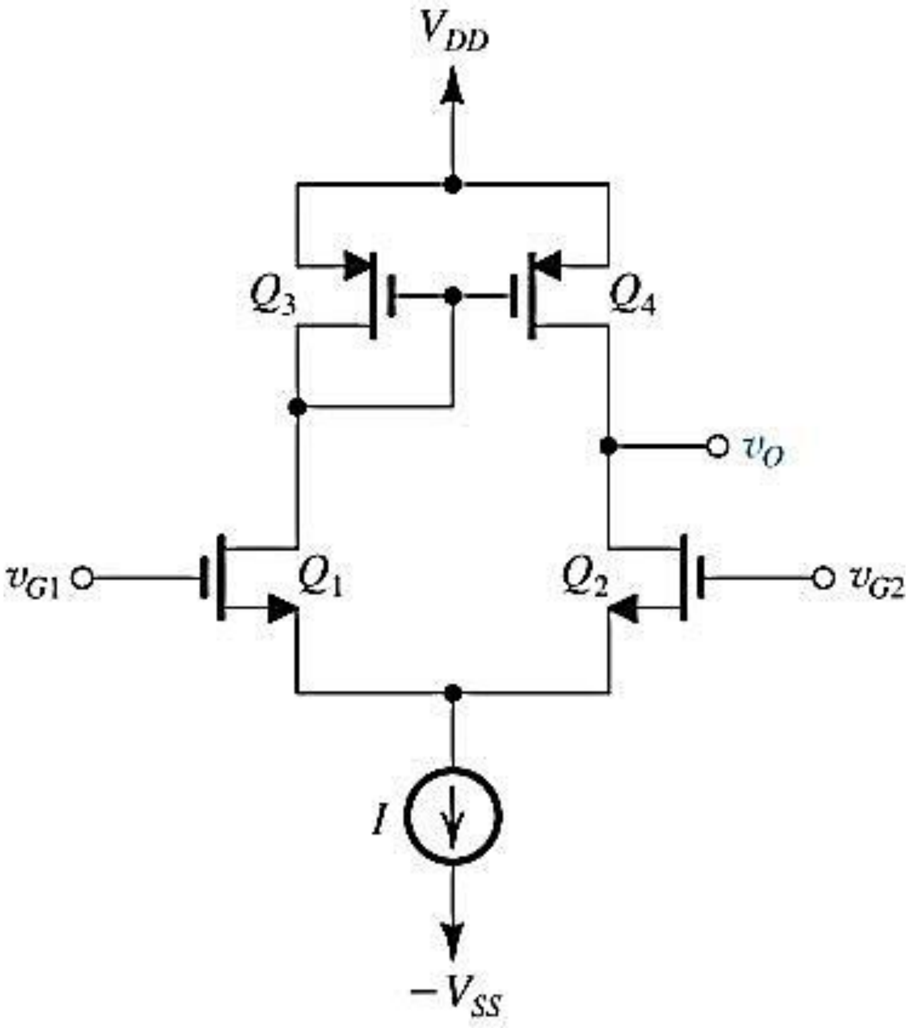
MOS Differential Pair with Active Load

- High output impedance
- Single ended output
- Assume Q1 and Q2 has same g_m and r_o

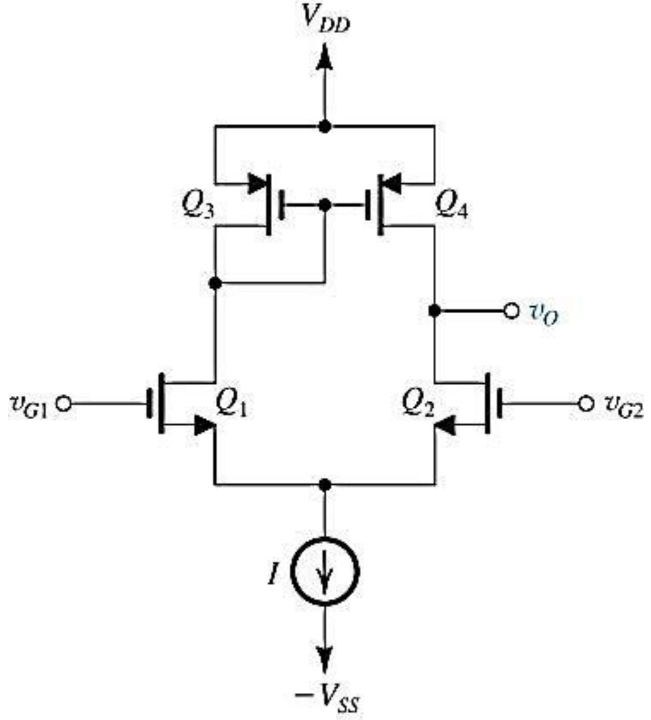
  $$g_{m1} = g_{m2} = g_{mn}, r_{o1} = r_{o2} = r_{on}$$

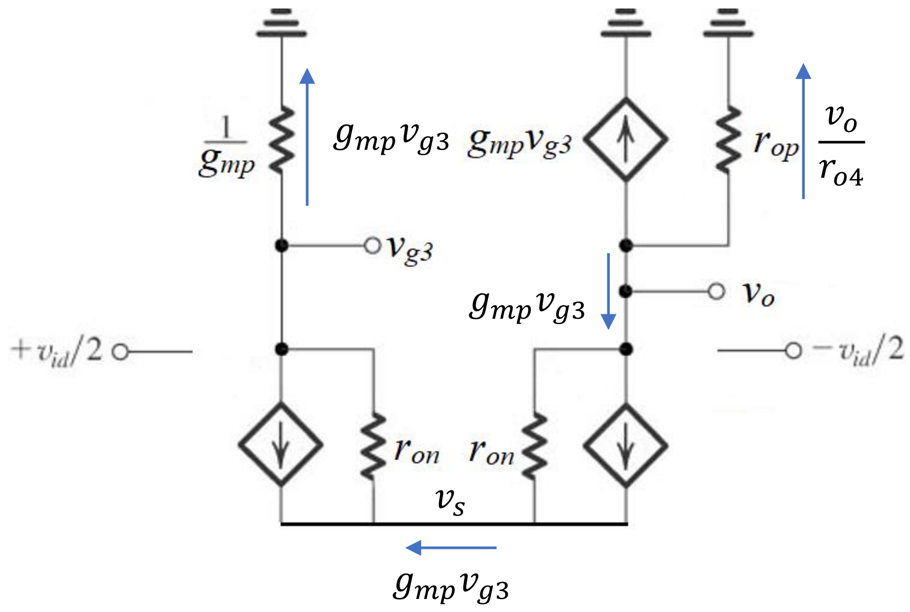
- Assume Q3 and Q4 has same g_m and r_o

  $$g_{m3} = g_{m4} = g_{mp}, r_{o3} = r_{o4} = r_{op}$$



MOS Differential Pair with Active Load

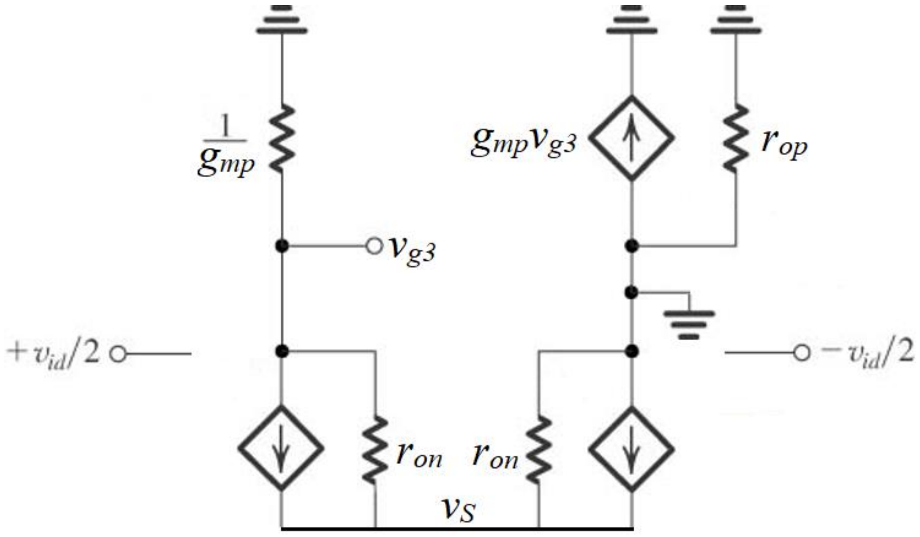




- KCL at output node→$g_{mp}v_{g3} + g_{mp}v_{g3} + \frac{v_o}{r_{op}} = 0 \rightarrow v_{g3} = -\frac{v_o}{2g_{mp}r_{op}}$
- KCL at output node→$g_{mp}v_{g3} = \frac{v_o - v_s}{r_{on}} + g_{mn}\left(-\frac{v_{id}}{2} - v_s\right)$ … (1)
- KCL at v_{g3} node→ $-g_{mp}v_{g3} = \frac{v_{g3} - v_s}{r_{on}} + g_{mn}\left(\frac{v_{id}}{2} - v_s\right)$ … (2)
- Subtract (1)-(2)→$2g_{mp}v_{g3} = \frac{v_o - v_{g3}}{r_{on}} - g_{mn}v_{id}$, use $v_{g3} = -\frac{v_o}{2g_{mp}r_{op}} \rightarrow v_o \approx g_{mn}(r_{on} \parallel r_{op})$
- Note that v_s is not 0V (you can prove $v_s \sim v_{id}/4$)

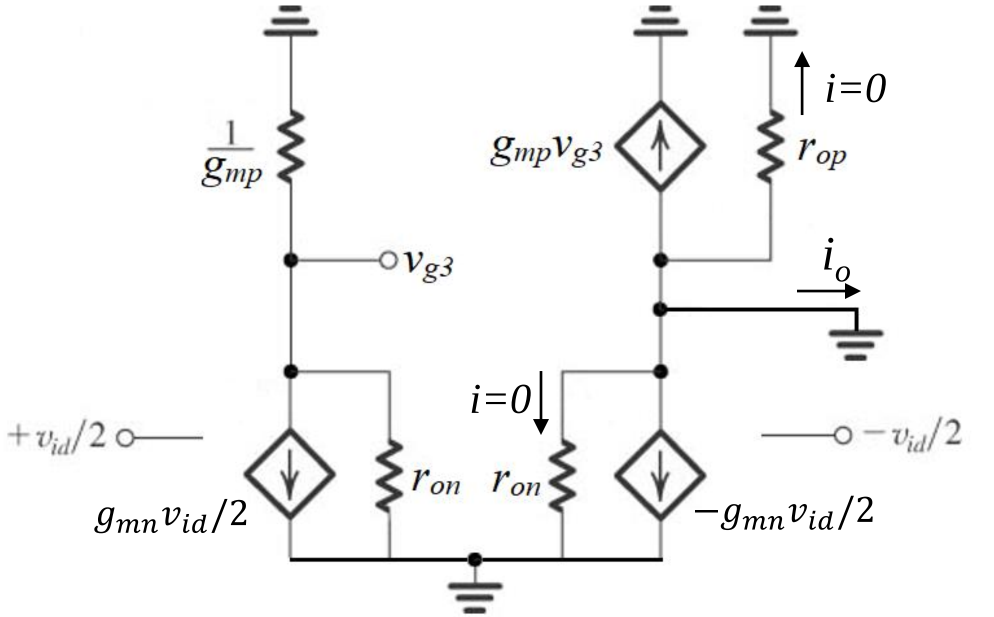
MOS Differential Pair with Active Load

- To get differential gain
  - Calculate transconductance G_m
  - Calculate R_{out}
  - $Gain = G_m R_{out}$
- Circuit is not symmetrical, half circuit concept cannot be used
  - When calculating Gm, output is short circuit to ground, v_S will be close to 0V (Need to prove it first, write KCL at v_{g3} and v_S nodes and get v_S as a function of v_{id})



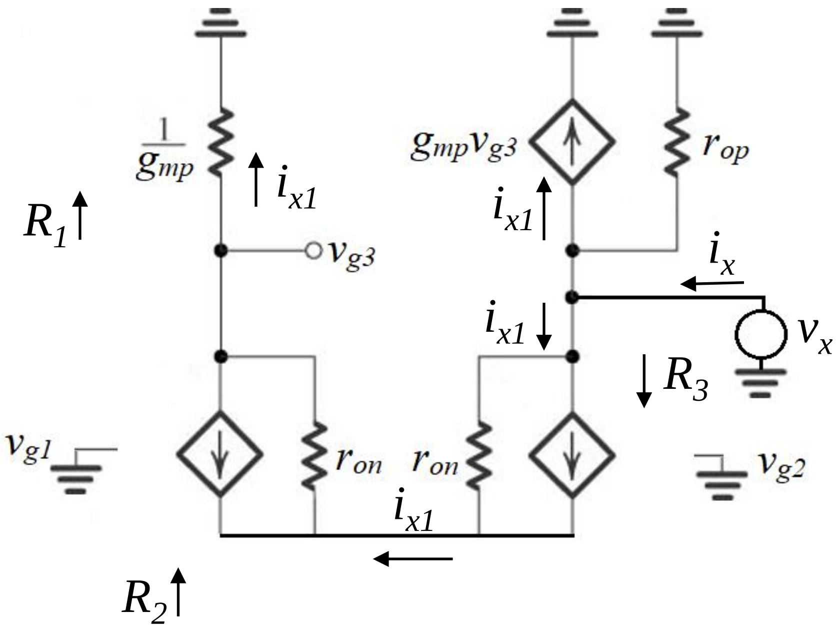
MOS Differential Pair with Active Load

- $v_{g3} \approx -\frac{g_{mn}}{g_{mP}}\frac{v_{id}}{2}, i_o = \frac{g_{mn}v_{id}}{2} - g_{mp}v_{g3} = g_{mn}v_{id}$
- $Hence\ G_m = g_{mn}$

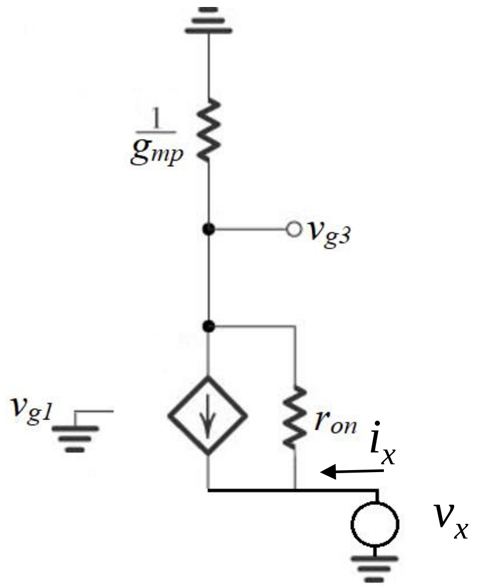


MOS Differential Pair with Active Load

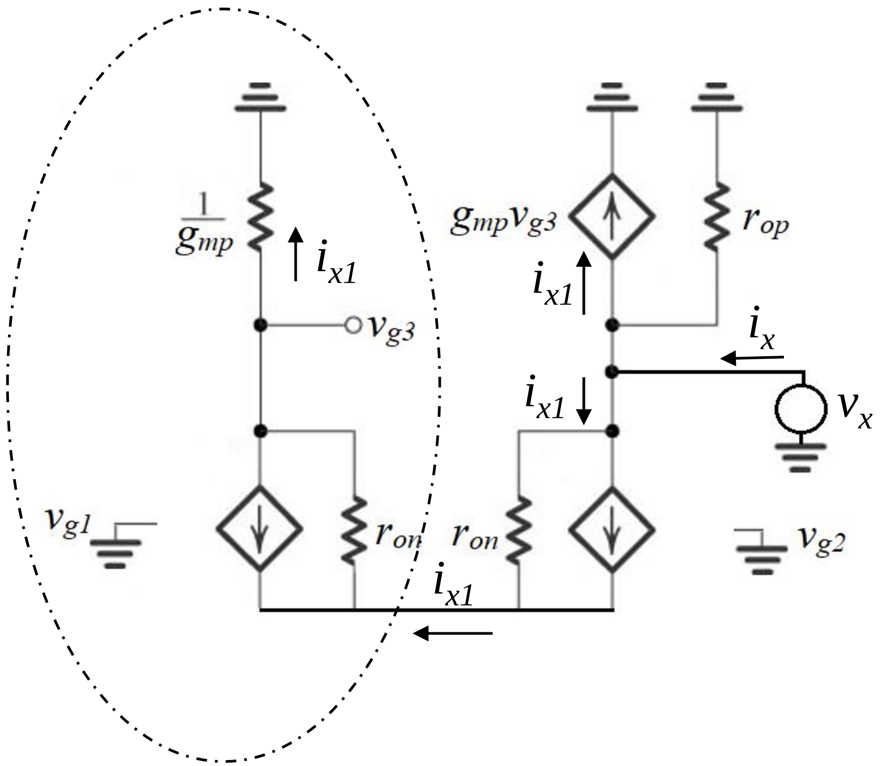
- $v_{g3} = \dfrac{i_{x1}}{g_{mp}}$
- $i_x = 2i_{x1} + \dfrac{V_x}{r_{op}}$



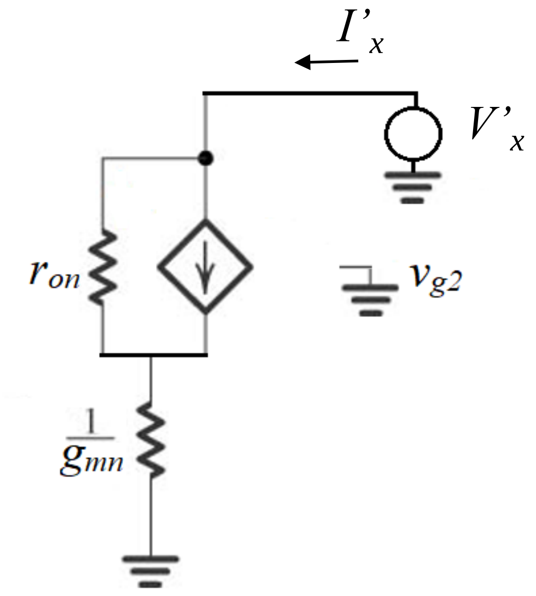
MOS Differential Pair with Active Load



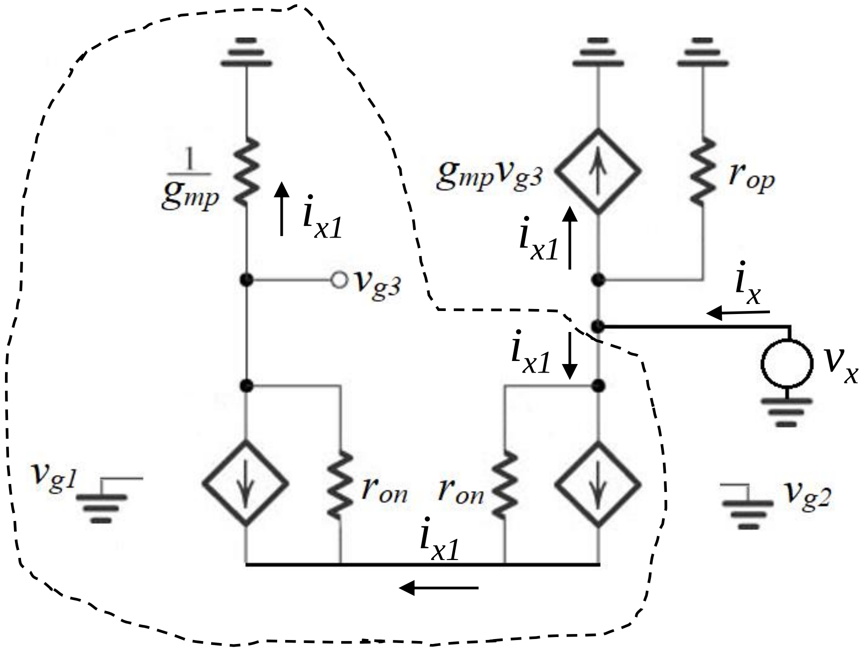
$$R_2 = \frac{r_{on} + 1/g_{mp}}{g_{mn} r_{on}} \approx \frac{1}{g_{mn}}$$



MOS Differential Pair with Active Load

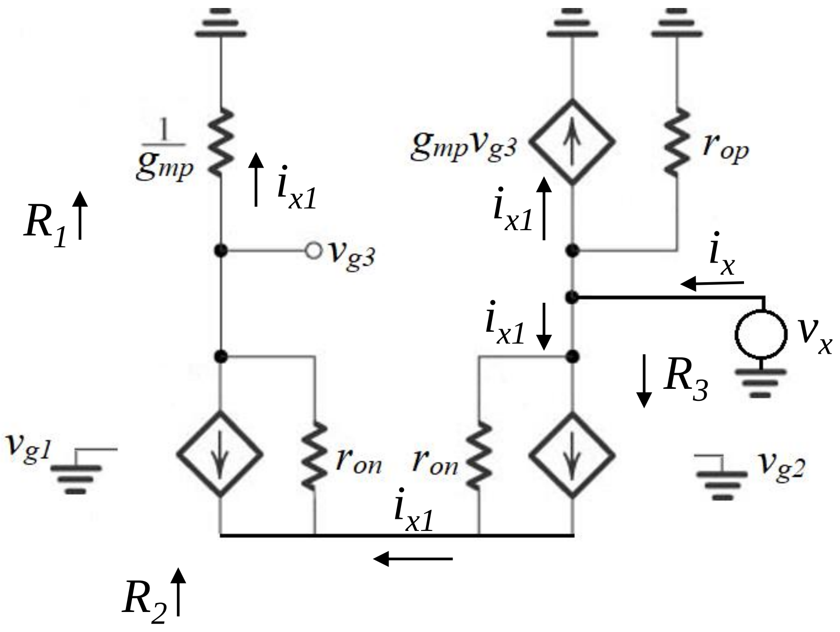


$$R_3 = r_{on} + R_2 + g_{mn} r_{on} R_2 \approx 2r_{on}$$



MOS Differential Pair with Active Load

- $R_1 = \frac{1}{g_{mp}}$
- $R_2 = \frac{r_{on} + 1/g_{mp}}{g_{mn} r_{on}} \approx \frac{1}{g_{mn}}$
- $R_3 = r_{on} + R_2 + g_{mn} r_{on} R_2 \approx 2r_{on}$
- $i_{x1} = \frac{V_x}{R_3}$
- $i_x = 2i_{x1} + \frac{V_x}{r_{op}} = 2\frac{V_x}{R_3} + \frac{V_x}{r_{op}} = \frac{V_x}{r_{on} \| r_{op}}$
- $R_{out} = r_{on} \parallel r_{op}$
- $A_{dm} = G_m R_{out} = g_{mn} r_{on} \parallel r_{op}$



Common Mode Gain Analysis

- Neglecting r_{on}, KCL at source node

$$v_S = 2g_{mn}(v_{iCM} - v_S)R_{SS}$$

$$v_s = \frac{2g_{mn}R_{SS}v_{iCM}}{1 + 2g_{mn}R_{SS}}$$

$$v_{gs} = \frac{v_{iCM}}{1 + 2g_{mn}R_{SS}}$$

- $v_{g3} = -\frac{g_{mn}v_{iCM}}{1+2g_{mn}R_{SS}}\left(\frac{1}{g_{mp}} \parallel r_{op}\right)$
- KCL at output node

$$\frac{g_{mn}v_{iCM}}{1 + 2g_{mn}R_{SS}} + g_{mp}v_{g3} + \frac{v_o}{r_{op}} = 0$$

$$v_o = -\frac{g_{mn}v_{iCM}}{1 + 2g_{mn}R_{SS}}\frac{r_{op}}{1 + g_{mp}r_{op}} \approx -\frac{1}{2g_{mp}R_{ss}}v_{icm}$$

$$A_{cm} = \frac{v_o}{v_{icm}} = -\frac{1}{2g_{mp}R_{ss}}$$