ELC2020

Electronics II

Active Current Mirrors

Acknowledgement: *"**Design of Analog CMOS Integrated Circuits**",* Chapter 5, 2nd Edition, Behzad Razavi

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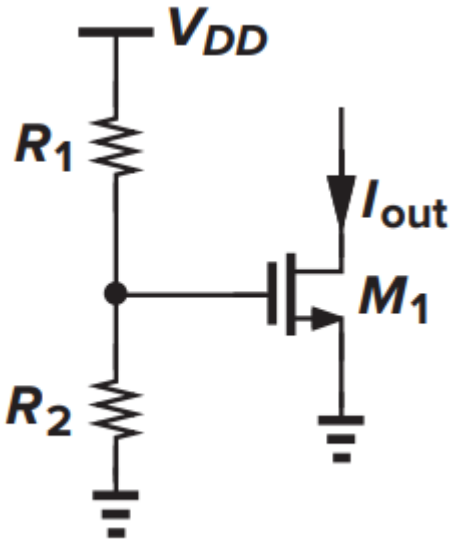
Simple Current Source

- The goal is to obtain a current that is insensitive to process, supply, and temperature (PVT) variations.
- Biasing with this simply divider from the supply makes the current sensitive to PVT variations.
- Assuming M1 is in saturation, we can write
- $I_{out} = \frac{1}{2} K_n (V_{GS} - V_{th})^2$
- $I_{out} = \frac{1}{2} K_n \left(VDD \frac{R_2}{R_1 + R_2} - V_{th} \right)^2 \rightarrow$

T,P V T,P



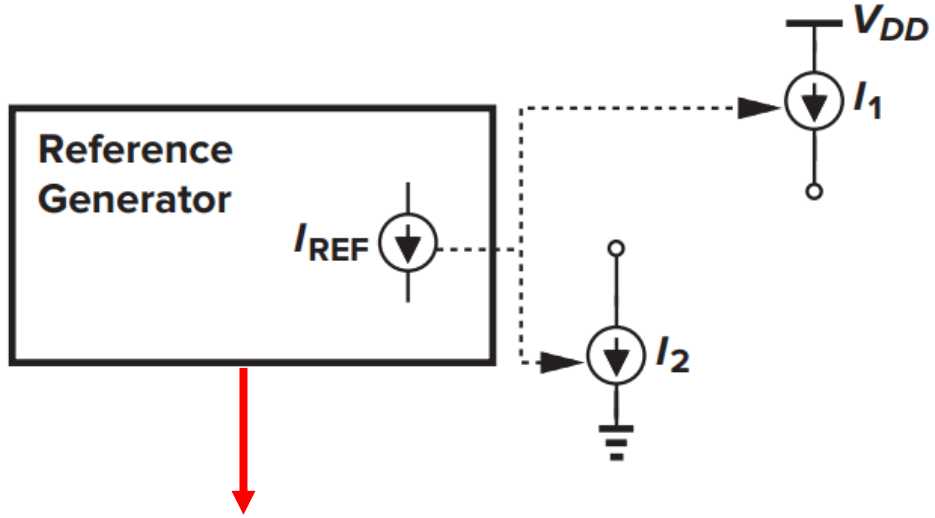
This expression reveals various PVT dependencies of I_{out}

- The overdrive voltage is a function of V_{DD} and V_{th}
- The threshold voltage may vary by 50 to 100 mV from wafer to wafer.
- Both μ_n and V_{th} exhibit temperature dependence.

Thus, I_{out} is poorly defined.

Current Mirrors

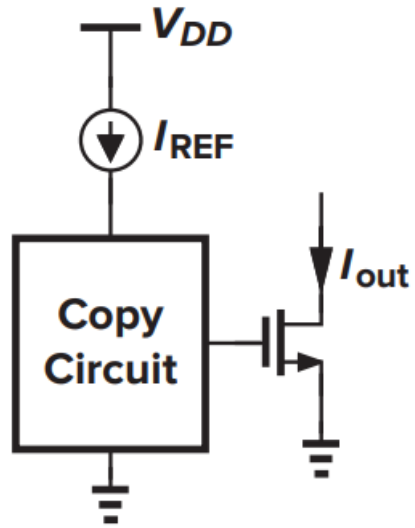
- The design of current sources is based on "copying" currents from a reference, with the assumption that one precisely-defined current source is already available.
- A relatively complex circuit is used to generate a stable reference current, I_{REF}, which is then "replicated" to create many current sources in the system using current mirrors.
- The design of the reference current generator itself (I_{REF}) is outside the scope of this course.

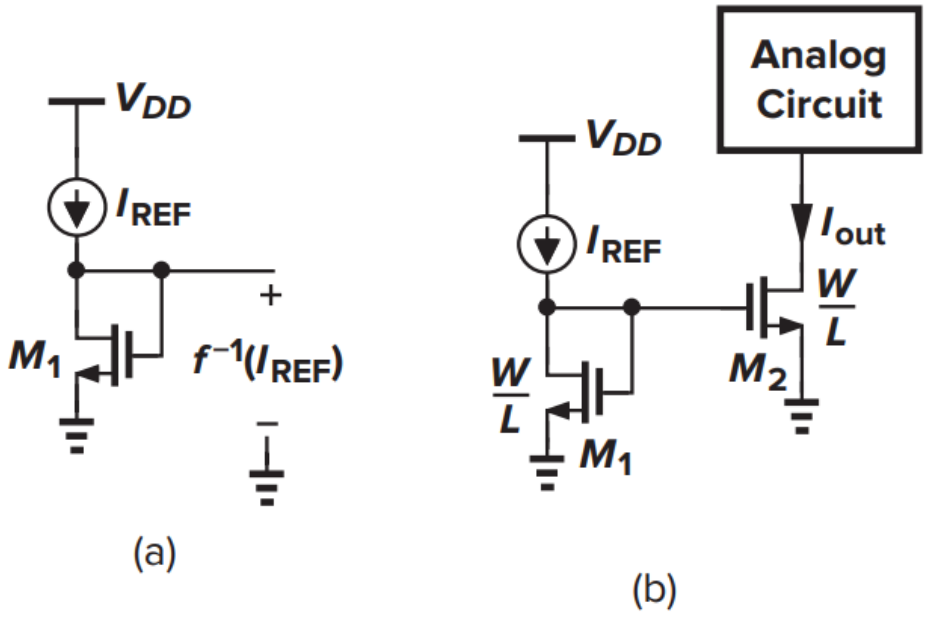


Sometimes requires external adjustments (calibration)

Current Mirrors (Cont'd)

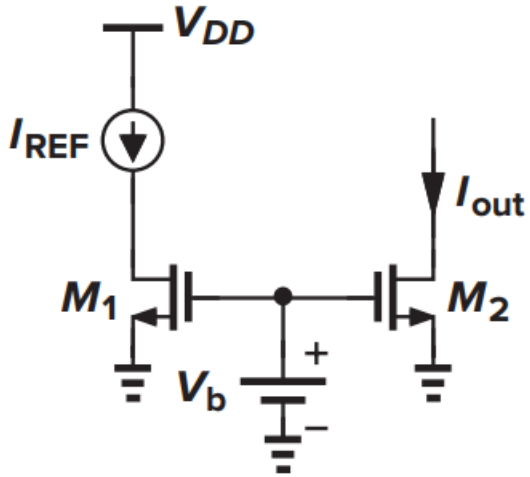
- How to generate $I_{out} = I_{REF}$?
- For a MOSFET, if $I_D = f(V_{GS})$, then $V_{GS} = f^{-1}(I_D)$.
- If this voltage (V_{GS}) is applied to the gate and source terminals of a second MOSFET, the resulting current is $I_{out} = f[f^{-1}(I_{REF})] = I_{REF}$
- Assume M_2 is in saturation and neglecting channel-length modulation (r_o), we can write:
  - $I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{th})^2$
  - $I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{th})^2$
  - $I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$
- I_{out} is independent of PVT ☺



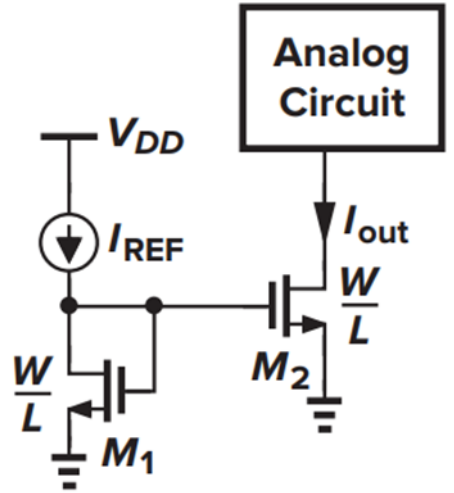


Current Mirrors (Cont'd)

- Is this circuit capable of copying currents?
  - No, V_b is not caused by I_{REF}, and hence I_{out} does not track I_{REF}.

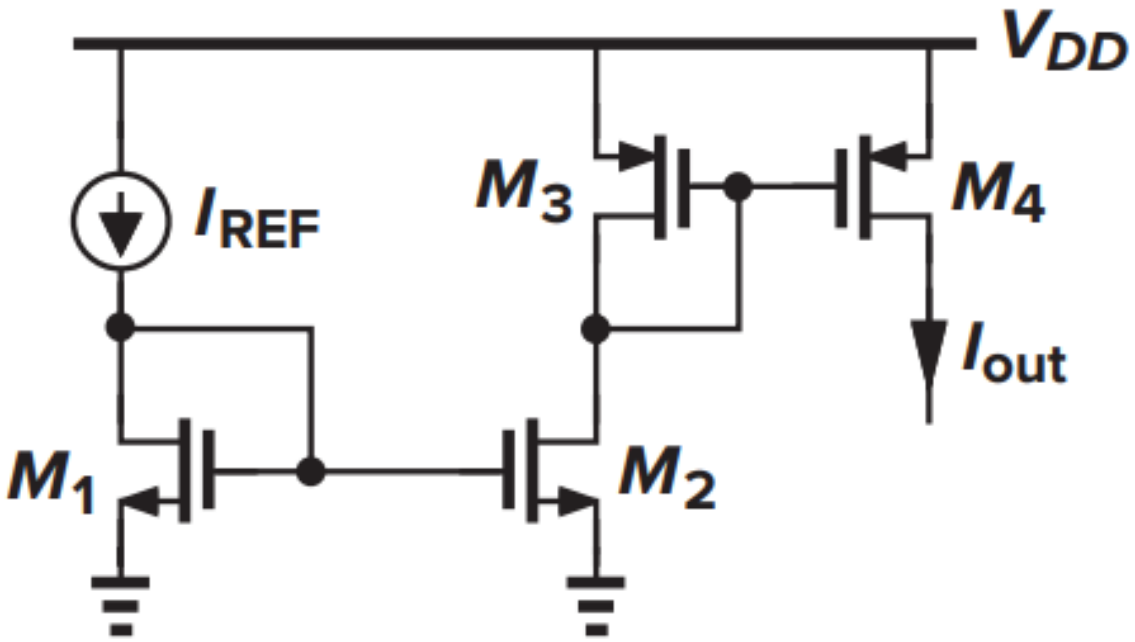


- So, for a current mirror circuit to work properly, we need to use a diode-connected device such that V_{GS} is generated by I_{REF}.



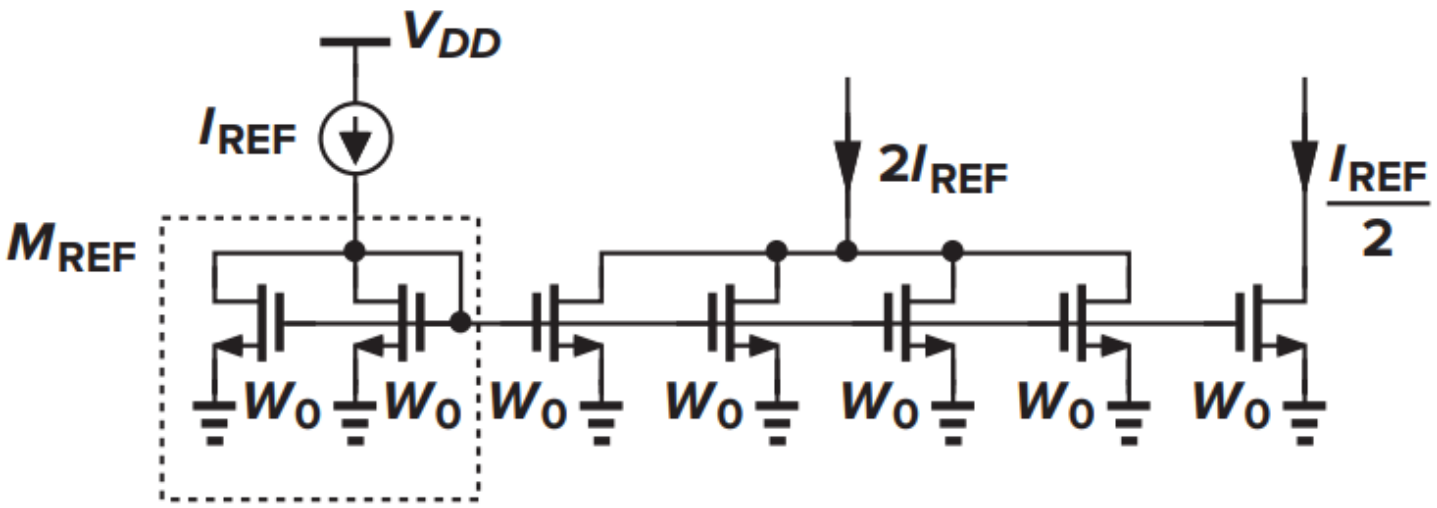
Example

- Find the drain current of M4 if all the transistors are in saturation.
- Solution:
  - $I_{D2} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$
  - $|I_{D3}| = |I_{D2}|$
  - $I_{D4} = \frac{(W/L)_4}{(W/L)_3} I_{D_3}$
  - $I_{out} = \frac{(W/L)_2}{(W/L)_1} \frac{(W/L)_4}{(W/L)_3} I_{REF} = \alpha\beta I_{REF}$
- $\alpha = \beta = 5 \rightarrow I_{out} = 25 I_{REF}$
- $\alpha = \beta = 0.2 \rightarrow I_{out} = 0.04 I_{REF}$
- Two current mirrors in “Cascade”|

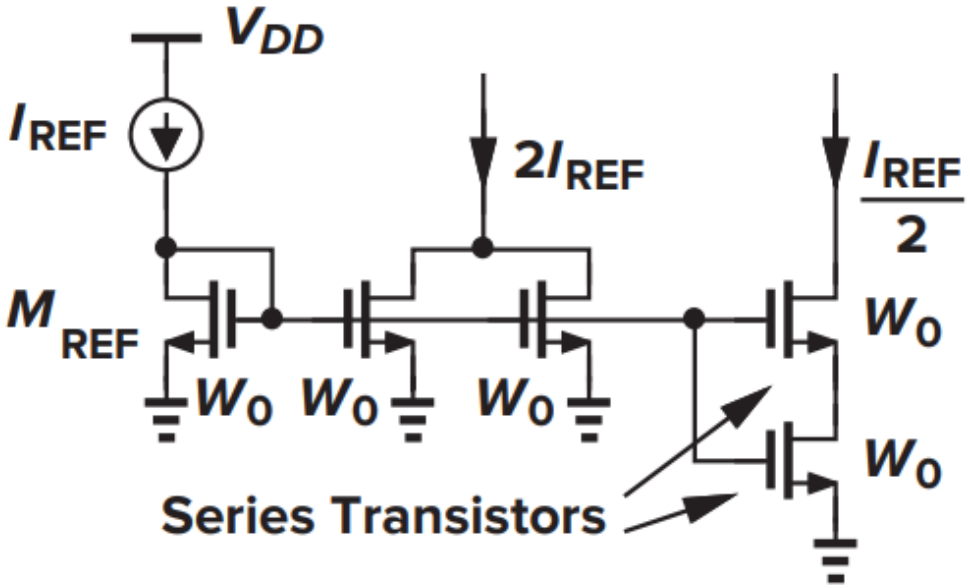


Sizing Issue

- We prefer to employ a "unit" transistor and create copies by repeating such a device to reduce mismatches between devices.
- How to generate $2I_{REF}$ and $0.5I_{REF}$ from I_{REF} current?



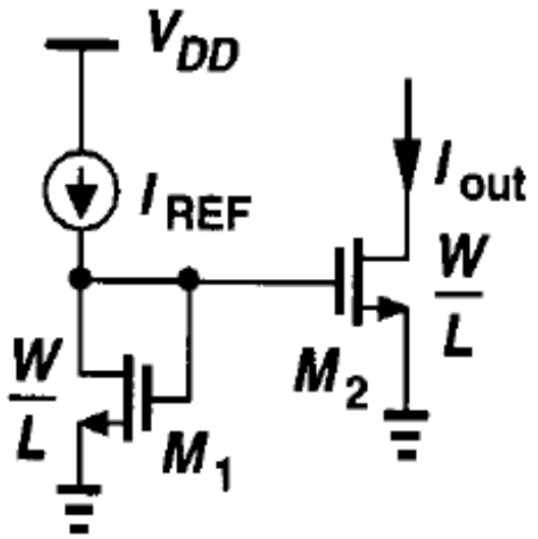
Solution 1

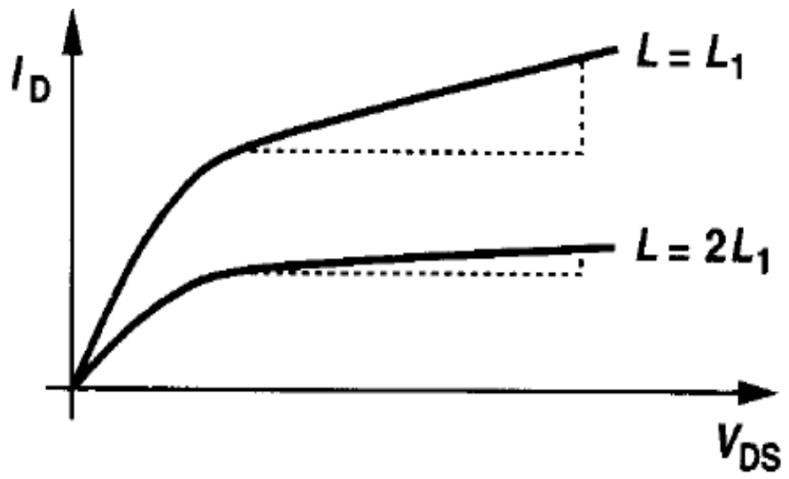


Solution 2

Channel Length Modulation Effect

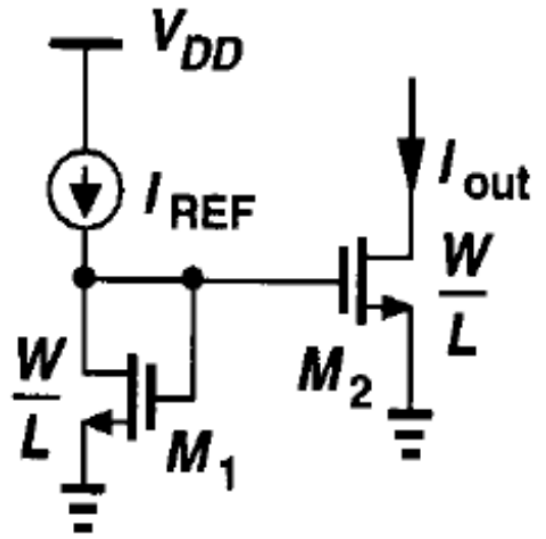
- Channel length modulation effect produces significant error in copying currents, especially if minimum-length transistors are used.
- Considering the channel length modulation effect (r_o):
  - $I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{th})^2(1 + \lambda V_{DS1})$
  - $I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{th})^2\ (1 + \lambda V_{DS2})$
  - $I_{out} = \frac{(W/L)_2}{(W/L)_1}\frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})} I_{REF} = \frac{(W/L)_2}{(W/L)_1}\frac{(1+\lambda V_{DS2})}{(1+\lambda V_{GS})} I_{REF}$
- While $V_{DS1} = V_{GS1} = V_{GS2}$, V_{DS2} may not equal V_{DS1} because of the circuitry fed by M_2.
- It is not desired to have the mirroring ratio dependent on V_{DS2}
- **Since $\lambda \propto 1/L$, we typically increase "L" to reduce the channel length modulation effect.**





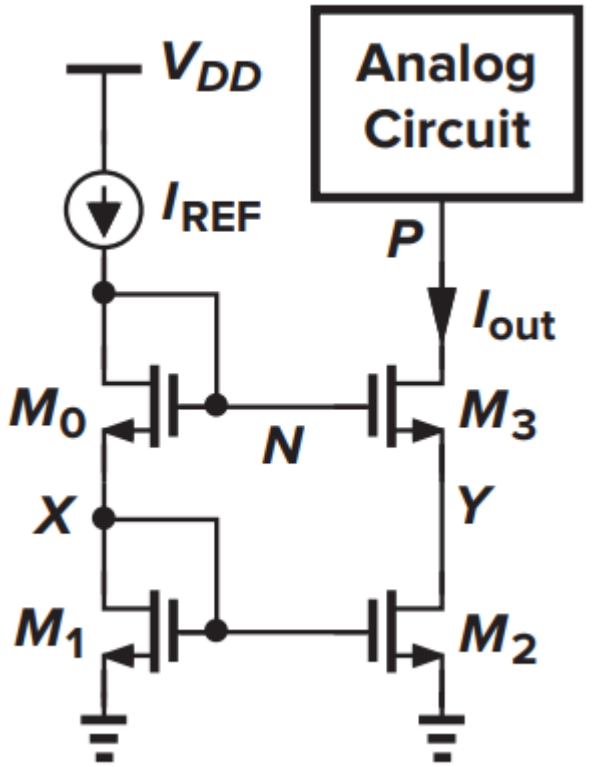
Channel Length Modulation Effect

- To have M_1 and M_2 operating at the edge of SAT region:
  - $V_{DS1} = V_{GS1}$ "diode connected"
  - $V_{DS2} = V_{ov2} = V_{GS2} - V_{TH2}$
  - $V_{DS1} \neq V_{DS2}$ → inaccuracy in current mirror ratio ☹
  - V_{DS1} is larger than V_{DS2} by V_{TH} → less headroom ☹
- To suppress the effect of channel-length modulation, we can either:
  1. Force V_{DS2} to be equal to V_{DS1}, or
     - $\boldsymbol{V_{DS2} = V_{DS1} = V_{GS1,2}}$
  2. Force V_{DS1} to be equal to V_{DS2}.
     - $\boldsymbol{V_{DS1} = V_{DS2} = V_{GS1,2} - V_{TH1,2}}$
- These two principles lead to two different topologies



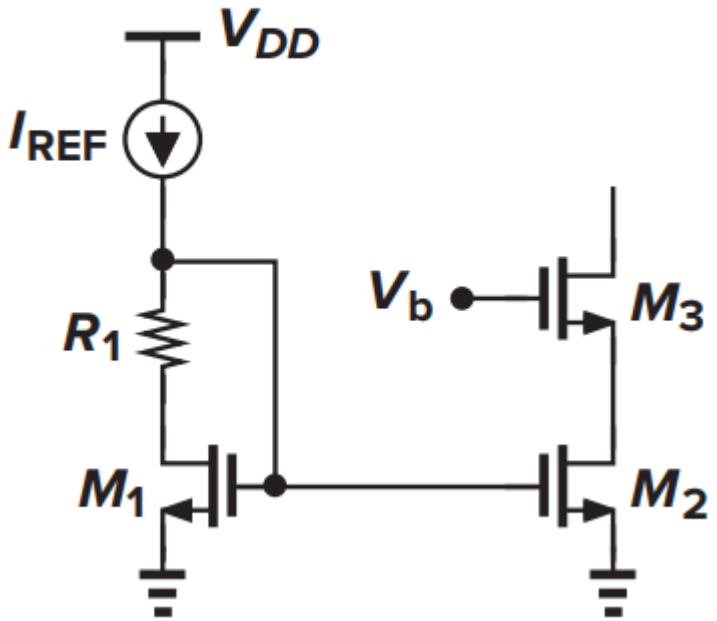
Cascode Current Mirrors – 1st Approach

- For the shown cascode current mirror:
  - $V_N = V_X + V_{GS0}$
  - $V_N = V_Y + V_{GS3}$
  - If $V_{GS0} = V_{GS3} \rightarrow V_Y = V_X$ "eliminate channel length modulation"
- In order for this to take place:
  - $V_{GS0} = V_{TH0} + \sqrt{\frac{2I_{REF}}{K_0}}$
  - $V_{GS3} = V_{TH3} + \sqrt{\frac{2I_{out}}{K_3}}$
  - $\frac{I_{out}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} = \frac{(W/L)_3}{(W/L)_0}$
- $V_{P,min} = V_{GS2} + (V_{GS3} - V_{TH3})$
- M2 is biased with a $V_{DS2} = V_{GS2}$, which is V_{TH2} away from the triode region edge.
- Accuracy is obtained at the expenses of the extra headroom
  - $(V_{GS} + V_{ov})$ instead of $(2V_{ov})$ → **VTH Penalty.**



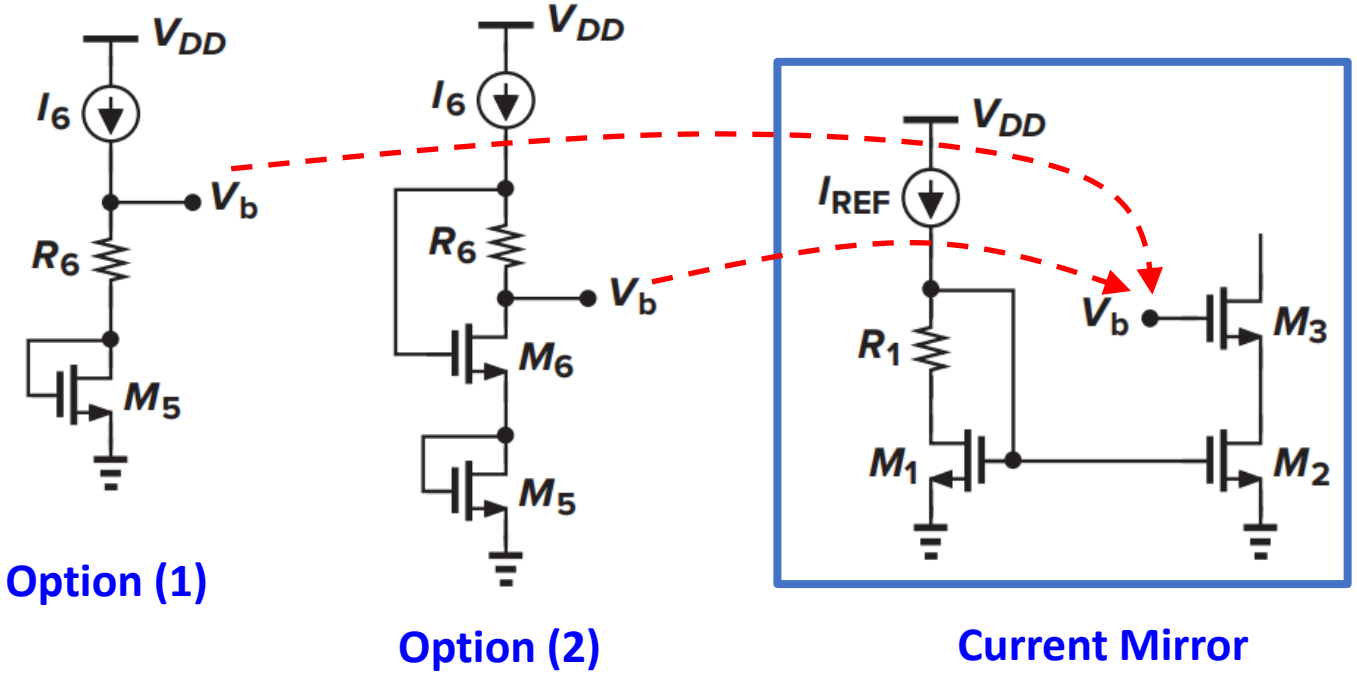
Low Voltage Cascode Current Mirrors – 2nd Approach (I)

- Force V_{DS1} to be equal to V_{DS2} to avoid the VTH penalty.
- Choose $V_b = V_{GS3} + (V_{GS2} - V_{TH2})$ so that
  - V_{DS2} is around one overdrive voltage.
  - Hence, $V_{out,min} = 2V_{ov}$ (Low Voltage Cascode)
- To ensure that $V_{DS1} = V_{DS2} = V_{GS2} - V_{TH2}$
  - Since M1 is a diode-connected device, it appears impossible to expect a V_{DS1} less than one threshold.
  - A simple solution is to create a deliberate voltage difference between the gate and drain of M1 by a means of a resistor.
- By choosing $I_{REF}R_1 \approx V_{TH1}$ and $V_b = V_{GS3} + (V_{GS1} - V_{TH1})$
  - $V_{DS1} = V_{GS1} - I_{REF}R_1 \approx V_{GS1} - V_{TH1}$, which is equal to $V_b - V_{GS3}$ and hence to V_{DS2}.



Low Voltage Cascode Current Mirrors – 2nd Approach (I)

- Design challenges:
  - In the presence of PVT variations, it is difficult to guarantee that $I_{REF}R_1 \approx V_{TH1}$ as R_1 and V_{TH} may vary differently.
  - The generation of $V_b = V_{GS3} + V_{ov2}$ is not straightforward.

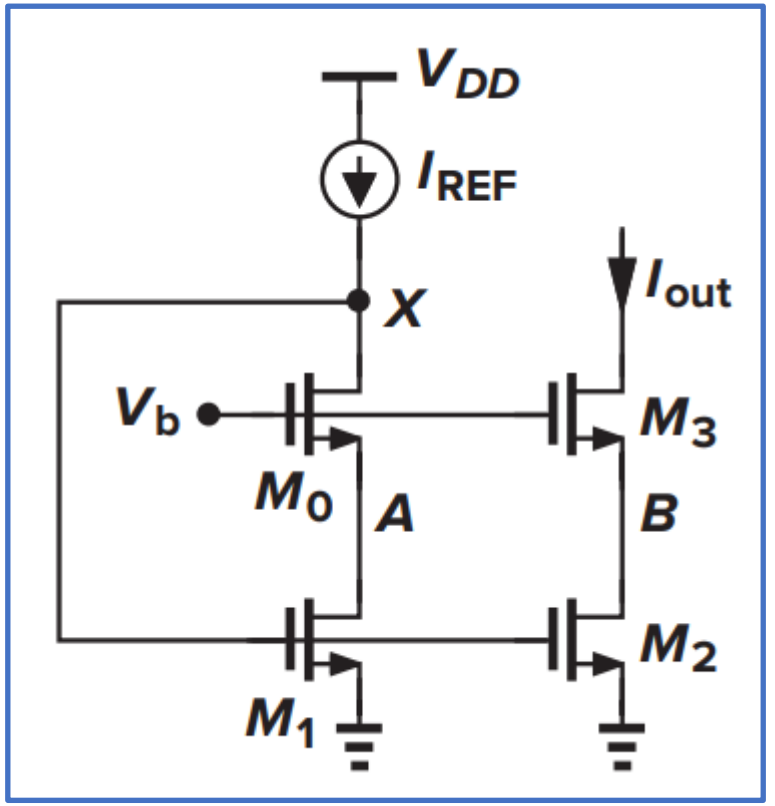


How to generate V_b?

- **Option (1):**
  - $V_b = V_{GS5} + I_6R_6 \rightarrow V_{GS5} = V_{GS3}$
  - $I_6R_6 = V_{GS1} - V_{TH1} = V_{GS1} - I_{REF}R_1$ translates to $I_6R_6 + I_{REF}R_1 = V_{GS1} \rightarrow$ Challenging to meet
- **Option (2):**
  - M_5 establishes the $V_{GS} \rightarrow V_{GS5} = V_{GS3}$
  - M_6 and R_6 generate $V_{ov} \rightarrow V_{ov} = V_{GS6} - I_6R_6 = V_{GS1} - V_{TH1} = V_{GS1} - I_{REF}R_1 \rightarrow V_{GS6} = V_{GS1}$
  - $V_b = V_{GS5} + (V_{GS6} - I_6R_6)$

Low Voltage Cascode Current Mirrors – 2nd Approach (II)

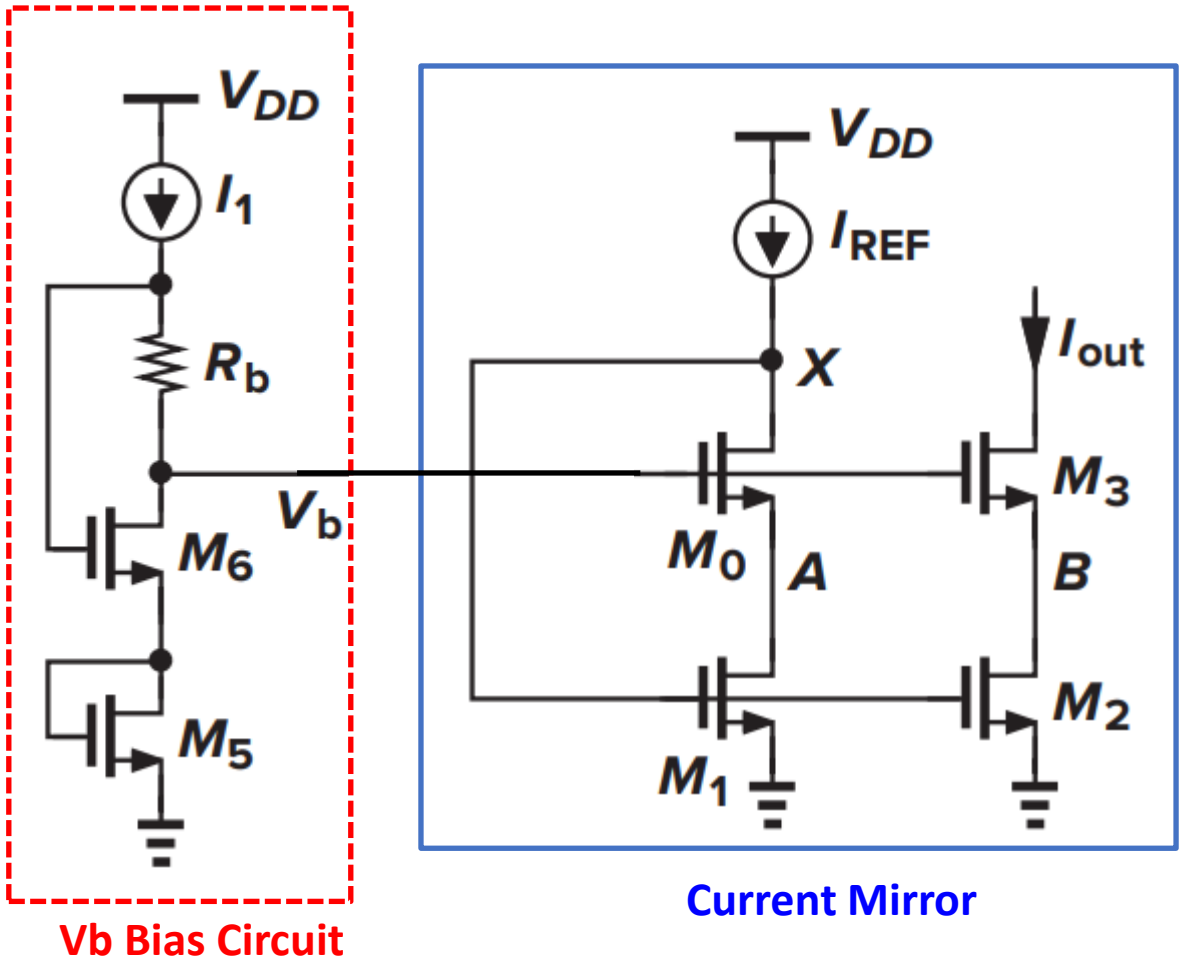
- To achieve high accuracy from the current mirror, we want to make sure that $V_A = V_B$
- If $V_{GS0} = V_{GS3}$ then $V_A = V_B$
- Then we have to size M_0 and M_3 according to the following:
  - $V_{GS0} = V_{TH0} + \sqrt{\frac{2I_{REF}}{K_0}}, \qquad V_{GS3} = V_{TH3} + \sqrt{\frac{2I_{out}}{K_3}}$
  - $\frac{I_{out}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} = \frac{(W/L)_3}{(W/L)_0}$
- V_b can be chosen to bias M_0 and M_3 at the edge of SAT:
  - $V_{b,min} = V_{GS0,3} + V_{ov1,2} = V_{GS0,3} + (V_{GS1,2} - V_{TH1,2})$
- $V_{out,min} = V_{b,min} - V_{TH0,3} = (V_{GS1,2} - V_{TH1,2}) + (V_{GS0,3} - V_{TH0,3}) = V_{ov1,2} + V_{ov0,3}$
- The minimum voltage is equal to 2 over drive voltages → LV cascode



Current Mirror

Low Voltage Cascode Current Mirrors – 2nd Approach (II)

- How can we generate the bias voltage V_b ?
  - $V_{b,min} = V_{GS0} + (V_{GS1} - V_{TH1})$
- In this bias circuit topology:
  - M_5 generates $V_{GS5} \sim V_{GS0,3}$
  - M_6 together with R_b produces $V_{DS6} = V_{GS6} - I_1 R_b \sim V_{GS1,2} - V_{TH1,2}$
- Some inaccuracy arises due to:
  - M_5 does not suffer from body effect whereas $M_{0,3}$ does.
  - The magnitude of $I_1 R_b$ is not well-controlled.



Low Voltage Cascode Current Mirrors – 2nd Approach (II)

- A simpler alternative to generate V_b is shown here.
- The diode-connected transistor M_7 provides the necessary V_{GS}
  - $V_{GS7} = V_{GS0,3}$
- M_6 creates a V_{DS} equal to the required overdrive.
  - $V_{ov6} = V_{GS6} - V_{TH6} = V_{ov1,2}$
- No resistors are used ☺