Lecture 5- Interconnects

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Outline of this Lecture

• Previously on ELCN321
• Parasitic Effects
• Interconnect Parasitic Parameters
  – Capacitance
  – Resistance
  – Inductance
• Electrical Wire Models
  – The Ideal Wire
  – The Lumped C Model
  – The Lumped RC Model
  – The Distributed $rc$ Model
Previously on ELCN321

Layout Design Rules

Design rules specify to the designer certain geometric constraints on the layout so that the patterns on the processed wafer will preserve the topology and geometry of the designs.

The areas handled in the design rules are:

- Minimum width of lines to avoid breaks in a line
- Minimum spacing between lines to avoid shorts between lines
- Minimum required overlap and enclosure between layers
Previously on ELCN321

Layout Design Rules

Industrial design rules are usually specified in microns. This makes migrating from one process to a more advanced process or a different foundry’s process difficult because not all rules scale in the same way.

Mead and Conway popularized scalable design rules based on a single parameter, $\lambda$. $\lambda$ is generally half of the minimum drawn transistor channel length (feature size).

Drawing the layout in terms of $\lambda$ helps in migrating from one technology to another (useful for digital, not much in analog).

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Previously on ELCN321

Layout Design Rules
Previously on ELCN321

Stick Diagrams

Stick diagrams are easy and fast way for the designers to plan cells and estimate area before committing to a full layout.
Introduction

Parasitic Effects

Interconnections usually appear in schematic diagrams of electronic circuits as simple lines with no impact on the circuit performance.

Physical interconnections between elements introduce parasitic effects (capacitive, resistive, and inductive parasitics).

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Introduction

Parasitic Effects

The parasitic effects tend to become important as device dimensions are reduced and circuit speed is increased.

New technologies make the production of larger die sizes economically feasible. This results in an increase in the length of an interconnections and in the associated parasitic effects.

Parasitic effects dominate some of the integrated circuits metrics such as speed (due to parasitic capacitance), energy-consumption (due to parasitic resistance), and reliability (extra noise sources due to coupling effects).
**Parasitic Effects**

**Model of the Parasitic Effects**

Including all parasitic effects in the circuit analysis is very complex and is totally useless for today’s integrated circuits with their millions of circuit nodes.
Parasitic Effects

Model of the Parasitic Effects

Inductive effects can be ignored if the resistance of the wire is substantial or if the rise and fall times of the applied signals are slow.

When the wires are short, the cross-section of the wire is large, or the interconnect material used has a low resistivity, a capacitance-only model can be used.

When the separation between neighboring wires is large, or when the wires only run together for a short distance, inter-wire capacitance can be ignored, and all the parasitic capacitance can be modeled as capacitance to ground.

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Parasitic Effects

Interconnect Parasitic Parameters

Capacitance

The capacitance of a wire is a function of its shape, its environment, its distance to the substrate, and the distance to surrounding wires.

Parallel-plate capacitor model is the simplest way to model the capacitance of the wire to the substrate

\[ C = \frac{\varepsilon d_i}{t_{di}} (W \times L) \]
Parasitic Effects

Interconnect Parasitic Parameters

Capacitance

The capacitance of a wire is a function of its shape, its environment, its distance to the substrate, and the distance to surrounding wires.

The parallel-plate capacitor model is good approximation if the width of the wire is larger than the thickness of the insulating material.

Electrical-field lines assumed to be orthogonal to the capacitor plates.
Parasitic Effects

Interconnect Parasitic Parameters

Capacitance

Small values of $W$ lead to denser wiring and less area overhead. Thus, the $W/H$-ratio witnessed a steady reduction and even dropped below unity in advanced processes.

The capacitance between the side walls of the wires and the substrate (fringing capacitance) can no longer be ignored and contributes to the overall capacitance.
Parasitic Effects

Interconnect Parasitic Parameters

Capacitance

A simplified model that encounters fringing capacitance is a parallel combination of two capacitances:

- Parallel-plate capacitance of width $w = W - H/2$,
- Cylindrical capacitance with a dimension equal to the interconnect thickness $H$.

$$C = \frac{\varepsilon_{di}}{t_{di}} w L + \frac{2\pi \varepsilon_{di}}{\log(t_{di}/H)} L$$

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## Parasitic Effects

### Interconnect Parasitic Parameters

#### Capacitance

**Typical interconnect capacitances for 0.25 µm CMOS process**

<table>
<thead>
<tr>
<th></th>
<th>Field</th>
<th>Active</th>
<th>Poly</th>
<th>Metal 1</th>
<th>Metal 2</th>
<th>Metal 3</th>
<th>Metal 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly</td>
<td>88</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>54</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal 1</td>
<td>30</td>
<td>41</td>
<td>57</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>47</td>
<td>54</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal 2</td>
<td>13</td>
<td>15</td>
<td>17</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>27</td>
<td>29</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal 3</td>
<td>8.9</td>
<td>9.4</td>
<td>10</td>
<td>15</td>
<td>41</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>18</td>
<td>19</td>
<td>20</td>
<td>27</td>
<td>49</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal 4</td>
<td>6.5</td>
<td>6.8</td>
<td>7</td>
<td>8.9</td>
<td>15</td>
<td>35</td>
<td></td>
</tr>
<tr>
<td></td>
<td>14</td>
<td>15</td>
<td>15</td>
<td>18</td>
<td>27</td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>Metal 5</td>
<td>5.2</td>
<td>5.4</td>
<td>5.4</td>
<td>6.6</td>
<td>9.1</td>
<td>14</td>
<td>38</td>
</tr>
<tr>
<td></td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>14</td>
<td>19</td>
<td>27</td>
<td>52</td>
</tr>
</tbody>
</table>

Area capacitances expressed in $aF/\mu m^2$.

Fringe capacitances expressed in $aF/\mu m$.
Interconnect Parasitic Parameters

Capacitance

Each wire is not only coupled to the grounded substrate, but also to the neighboring wires on the same layer and on adjacent layers.

Floating capacitors form a source of noise (crosstalk), and can have a negative impact on the performance of the circuit.

Inter-wire capacitances become dominant for higher interconnect layers as these wires are farther away from the substrate.
Parasitic Effects

Interconnect Parasitic Parameters

Capacitance

The polysilicon wires experience small inter-wire capacitance due to the smaller thickness of the wires.

The thick Metal 5 wires has the highest interwire capacitance. To reduce the capacitance, the separations between the wires are increased above the minimum allowed.

Inter-wire capacitance per unit length for 0.25\(\mu\)m CMOS process

<table>
<thead>
<tr>
<th>Inter-wire Capacitance</th>
<th>Poly</th>
<th>Metal 1</th>
<th>Metal 2</th>
<th>Metal 3</th>
<th>Metal 4</th>
<th>Metal 5</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>40</td>
<td>95</td>
<td>85</td>
<td>85</td>
<td>85</td>
<td>115</td>
</tr>
</tbody>
</table>
Parasitic Effects

Example (1)

For die sizes between 1 and 2 cm, Metal 1 wire can reach a length of 10 cm. Compute the value of the total capacitance of this wire to the ground if its width is 1μm and assume that the wire is running over field oxide.

<table>
<thead>
<tr>
<th></th>
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<td></td>
<td>40</td>
<td>47</td>
<td>54</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

area capacitances expressed in aF/μm²
fringe capacitances expressed in aF/μm

\[ PPC = [(1μm) \times (0.1 \times 10^6 μm)] \times 30 \text{ aF/μm}^2 = 3pF \]

\[ FC = 2 \times [0.1 \times 10^6 μm] \times 40 \text{ aF/μm} = 8pF \]

Total Capacitance = 3 + 8 = 11 pF
Parasitic Effects

Example (2)

If another Metal 1 wire of 10 cm length is routed alongside the first one and separated by the minimum allowed distance. Compute the value of the inter-wire capacitance.

<table>
<thead>
<tr>
<th>Inter-wire Capacitance</th>
<th>Poly</th>
<th>Metal 1</th>
<th>Metal 2</th>
<th>Metal 3</th>
<th>Metal 4</th>
<th>Metal 5</th>
</tr>
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<td>40</td>
<td>95</td>
<td>85</td>
<td>85</td>
<td>85</td>
<td>85</td>
<td>115</td>
</tr>
</tbody>
</table>

\[ IWC = [0.1 \times 10^6 \mu m] \times 95 \text{ aF/\mu m} = 9.5pF \]

The inter-wire capacitance is almost as large as the total capacitance to ground
Parasitic Effects

Interconnect Parasitic Parameters

Resistance

The resistance of a wire is proportional to its length $L$ and inversely proportional to its cross-section $A$.

$$ R = \frac{\rho L}{A} = \frac{\rho L}{HW} = \frac{\rho}{H} \times \frac{L}{W} $$

$\rho$ is the resistivity of the material (in $\Omega \cdot m$).

Since the thickness ($H$) of a given technology is a constant, the sheet resistance $R_\square = \rho / H$ is constant and can be considered as a property of the material. $R_\square$ has the unit $\Omega / \square$. 
Parasitic Effects

Interconnect Parasitic Parameters

Resistances

<table>
<thead>
<tr>
<th>Material</th>
<th>Sheet Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>n- or p-well diffusion</td>
<td>1000 – 1500</td>
</tr>
<tr>
<td>n⁺, p⁺ diffusion</td>
<td>50 – 150</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>150 – 200</td>
</tr>
<tr>
<td>Aluminum</td>
<td>0.05 – 0.1</td>
</tr>
</tbody>
</table>

Aluminum is the preferred material for the wiring of long interconnections.

Polysilicon should only be used for local interconnect.

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Parasitic Effects

Interconnect Parasitic Parameters

Resistance

<table>
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<th>Sheet Resistance</th>
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</tr>
<tr>
<td>$n^+$, $p^+$ diffusion</td>
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</tr>
<tr>
<td>Polysilicon</td>
<td>150 – 200</td>
</tr>
<tr>
<td>Aluminum</td>
<td>0.05 – 0.1</td>
</tr>
</tbody>
</table>

Although the sheet resistance of the diffusion layer is comparable to that of polysilicon, the use of diffusion wires should be avoided due to its large capacitance.

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Parasitic Effects

Interconnect Parasitic Parameters

Resistance

Transitions between routing layers add extra resistance to a wire, called the contact resistance.

To reduce the total resistance of an interconnection, the connection need to be kept on a single layer.

Making the contact holes larger reduces the contact resistance. However, current tends to concentrate around the perimeter in a larger contact hole. This effect is called current crowding and it puts a practical upper limit on the size of the contact
Parasitic Effects

Interconnect Parasitic Parameters

Resistance

For 0.25μm CMOS process, the contact resistances of the minimum size contacts is 5-20Ω (metal or polysilicon to \( n^+ \), \( p^+ \), and metal to polysilicon) and 1-5 Ω for vias (metal-to-metal contacts).
Parasitic Effects

Example (3)

Calculate the total resistance of a 10 cm long and 1 μm wide of Metal 1 wire if it is made of aluminum with sheet resistance of 0.075 Ω/μm. Recalculate the total resistance if the wire is made of polysilicon with a sheet resistance of 175 Ω/μm.

\[ R_M = 0.075 \text{ Ω/μm} \times \frac{0.1 \times 10^6 \text{ μm}}{1 \text{ μm}} = 7.5kΩ \]

\[ R_p = 175 \text{ Ω/μm} \times \frac{0.1 \times 10^6 \text{ μm}}{1 \text{ μm}} = 17.5MΩ \]

The resistance of poly wire is very big, thus is unacceptable.
Parasitic Effects

Interconnect Parasitic Parameters

Resistance

High frequency currents tend to flow primarily on the surface of a conductor with the current density falling off exponentially with depth into the conductor. This phenomenon is called the skin effect.

The skin effect causes the resistance to be frequency-dependent.
Parasitic Effects

Interconnect Parasitic Parameters

Resistance

The skin depth $\delta$ is defined as the depth where the current falls off to a value of $e^{-1}$ of its nominal value and is given by

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}}$$

where $\mu$ the permeability of the surrounding dielectric.

To simplify the calculation of the resistance, the skin effect can be approximated by assuming that the current flows uniformly in an outer shell of the conductor with thickness $\delta$. 

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Parasitic Effects

Interconnect Parasitic Parameters

Resistance

The cross section of the wire through which the current flows can be approximated to

\[ A = 2\delta \times (H + W) \]

The resistance at high frequencies can be calculated as

\[ R = \frac{\rho L}{A} = \frac{\rho L}{2\delta \times (H + W)} = \frac{L\sqrt{\pi f \mu \rho}}{2(H + W)} \]
Parasitic Effects

Interconnect Parasitic Parameters

Resistance

The frequency $f_{se}$ at which skin effect starts can be calculated by

$$\delta = \frac{1}{2} \min(H, W) \quad \rightarrow \quad f_{se} = \frac{4\rho}{\pi\mu[\min(H, W)]^2}$$

The increase in the resistance with frequency causes extra attenuation at high frequency. Thus, distortion occurs.
Parasitic Effects

Interconnect Parasitic Parameters

Inductance

The capacitance $C$ and the inductance $L$ (per unit length) of a wire are related by

$$C \times L = \varepsilon \times \mu$$

where $\varepsilon$ and $\mu$ are the permittivity and permeability of the surrounding dielectric, respectively.
Parasitic Effects

Example (4)

Derive an expression for the inductance per unit length of Metal 1 wire in 250μm CMOS technology if it is routed on top of the field oxide.

For Metal 1 wire in 250μm CMOS technology, the capacitance per unit length is given by

\[ C = 30 \times W + 2 \times 40 \text{ aF/μm} \]

The inductance per unit length of the wire is given by

\[ L = \frac{\varepsilon \times \mu}{C} = \frac{(3.9 \times 8.85 \times 10^{-12})(4\pi \times 10^{-7}) \times 10^{-6}}{(30 \times W + 2 \times 40) \times 10^{-10}} \text{ H/m} \]
Parasitic Effects

Example (4)

Derive an expression for the inductance per unit length of Metal 1 wire in 250µm CMOS technology if it is routed on top of the field oxide.

For wire widths of 0.4µm, 1µm and 10µm

<table>
<thead>
<tr>
<th>W (µm)</th>
<th>C (aF/µm)</th>
<th>L (pH/µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4</td>
<td>92</td>
<td>0.47</td>
</tr>
<tr>
<td>1</td>
<td>110</td>
<td>0.39</td>
</tr>
<tr>
<td>10</td>
<td>380</td>
<td>0.11</td>
</tr>
</tbody>
</table>
Electrical Wire Models

Definition

Interconnect parasitic elements have an impact on the electrical behavior of the circuit and influence its delay, power dissipation, and reliability.

The study of these influences requires the introduction of electrical models that estimate and approximate the real behavior of the wire as a function of its parameters.

Electrical models vary from very simple to very complex depending upon the effects that are being studied and the required accuracy.

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The Ideal Wire

The ideal wire has no parasitic effect.

Ideal wires have no impact on the electrical behavior of the circuit.

A voltage change at one end of the wire propagates immediately to its other ends, even if those are some distance away.

The ideal wire model has its value in the early phases of the design process (concentrate on the of the connected transistors).
The Ideal Wire

For small circuit components such as gates, the wires tend to be very short and their parasitics are ignorable.
The parasitics of a wire are distributed along its length and are not lumped into a single position.

When the resistive component of the wire is small and the switching frequencies are in the low to medium range, only the capacitive component of the wire can be considered, and the distributed capacitance can be lumped into a single capacitor.
Electrical Wire Models

The Lumped C Model

In this model the wire represents an equipotential region (has no resistance).

The only impact on performance is introduced by the loading effect of the capacitor on the driving gate.

The capacitive lumped model is simple, yet effective, and is the model of choice for the analysis of most interconnect wires in digital integrated circuits.

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The Lumped C Model

The advantage of this approach is that the effects of the parasitic then can be described by an ordinary differential equation instead of partial differential equations.
Example (5)

For the shown circuit, assume that a driver with a source resistance of 10 kW is used to drive a 10 cm long, 1 mm wide Al1 wire. Calculate the time to reach the 50% and 90% point when $v_{in}$ is unit step.

The operation of this RC network is described by the following ordinary differential equation

$$\frac{V_{in}(t) - V_{out}(t)}{R_{driver}} = C_{lumped} \frac{dV_{out}(t)}{dt}$$

$$V_{out}(0) = 0$$
Example (5)

For the shown circuit, assume that a driver with a source resistance of 10 kW is used to drive a 10 cm long, 1 mm wide Al1 wire. Calculate the time to reach the 50% and 90% point when \( v_{in} \) is unit step

\[
V_{out}(t) = V_f \left(1 - e^{-\frac{t}{\tau}}\right), \quad \tau = R_{driver} \times C_{lumped} = 110\,\text{ns}
\]

The time to reach the 50% point is given by

\[
0.5 = \left(1 - e^{-\frac{t_{50\%}}{\tau}}\right) \quad \rightarrow \quad t_{50\%} = \tau \ln(2) = 0.69\tau
\]

\[\approx 76\,\text{ns}\]
Electrical Wire Models

Example (5)

For the shown circuit, assume that a driver with a source resistance of 10 kW is used to drive a 10 cm long, 1 mm wide Al1 wire. Calculate the time to reach the 50% and 90% point when \( v_{in} \) is unit step.

The time to reach the 90% point is given by

\[
0.9 = (1 - e^{-t_{90\%}/\tau}) \quad \rightarrow \quad t_{90\%} = \tau \ln(9) = 2.2\tau
\]

\[
\approx 242\text{ns}
\]
Electrical Wire Models

The Lumped RC Model

On-chip metal wires of over a few mm length have a significant resistance. Thus, the equipotential assumption is no longer adequate.

In the lumped RC model, the total wire resistance is lumped into one single $R_{lumped}$ and the total wire capacitance is lumped into a single capacitor $C_{lumped}$.

The lumped RC model is **pessimistic and inaccurate** for long interconnect wires.

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The Distributed $rc$ Model

In this model, the wire is partitioned into identical segments of length $\Delta L$.

The resistance and capacitance of each segment are given by $r\Delta L$ and $c\Delta L$, respectively.
The voltage at node $i$ can be determined by solving a set of partial differential equations

$$c \Delta L \frac{\partial V_i}{\partial t} = \frac{(V_{i+1} - V_i) + (V_{i-1} - V_i)}{r \Delta L}$$
The Distributed \( rc \) Model

The correct behavior of the distributed \( rc \) line is then obtained by reducing \( DL \) asymptotically to 0

\[
c\Delta L \frac{\partial V_i}{\partial t} = \frac{(V_{i+1} - V_i) + (V_{i-1} - V_i)}{r\Delta L} \quad \rightarrow \quad rc \frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}
\]
No closed-form solution exists for this equation. This makes the delay calculation complex.

Elmore delay formula is usually used to simplify the delay calculation.
The Distributed $rc$ Model

Elmore delay formula

There is a unique resistive path between the source node $s$ and any node $i$ in the network. The total resistance along a path is called the path resistance $R_{ii}$.

The path resistance between the source node $s$ and node 2

$$R_{22} = R_1 + R_2$$

The path resistance between the source node $s$ and node 4

$$R_{44} = R_1 + R_3 + R_4$$
Electrical Wire Models

The Distributed $rc$ Model

Elmore delay formula

The shared path resistance $R_{ik}$ represents the resistance shared among the paths from the node $s$ to nodes $k$ and $i$

$$R_{ik} = \sum R_j$$

$R_j \in [path (s \to k) \cap path(s \to i)]$

$$R_{54} = R_1 + R_3$$

$$R_{52} = R_1$$
The Distributed $rc$ Model

Elmore delay formula

Elmore delay formula states that the delay at node $i$ is given by

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

$$\tau_{D3} = R_1 C_1 + R_1 C_2 + (R_1 + R_3)C_3 + (R_1 + R_3)C_4 + (R_1 + R_3)C_5$$

$$\tau_{D5} = R_1 C_1 + R_1 C_2 + (R_1 + R_3)C_3 + (R_1 + R_3)C_4 + (R_1 + R_3 + R_5)C_5$$

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Electrical Wire Models

The Distributed $rc$ Model

Elmore delay formula

Non-branched RC chain (or ladder) is a special case of the RC tree network.

Non-branched RC represents an approximative model of the distributed $rc$ model

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The Distributed $rc$ Model

Elmore delay formula

$$\tau_{DN} = C_1 R_1 + C_2 (R_1 + R_2) + \cdots + C_N (R_1 + R_2 + \cdots + R_N)$$

$$= \sum_{k=1}^{N} C_i \sum_{j=1}^{i} R_j = \sum_{k=1}^{N} C_i R_{ii}$$
Electrical Wire Models

Example (6)

Compute the dominant time constant of a wire of length $L$ using the non-branched RC chain model.

The wire is partitioned into $N$ identical segments, each with a length of $L/N$. The resistance and capacitance of each segment are hence given by $rL/N$ and $cL/N$, respectively.

Using the Elmore formula, the dominant time constant is given by

$$
\tau_{DN} = \frac{cL}{N} \times \frac{rL}{N} + \frac{cL}{N} \times 2 \frac{rL}{N} + \cdots + \frac{cL}{N} \times N \frac{rL}{N}
$$
Electrical Wire Models

Example (6)
Compute the dominant time constant of a wire of length $L$ using the non-branched RC chain model

$$\tau_{DN} = \frac{cL}{N} \times \frac{rL}{N} + \frac{cL}{N} \times 2 \frac{rL}{N} + \cdots + \frac{cL}{N} \times N \frac{rL}{N}$$

$$= \frac{r\!cL^2}{N^2} (1 + 2 + \cdots + N) = \frac{r\!cL^2}{N^2} \frac{N(N + 1)}{2}$$

$$= RC \frac{N + 1}{2N}$$
The Distributed $rc$ Model

\[ \tau_{DN} = RC \frac{N + 1}{2N} \]

For very large values of $N$

\[ \tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2N^2} \]
Electrical Wire Models

The Distributed $rc$ Model

\[ \tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2N^2} \]

The delay of a wire is a **quadratic** function of its length.

The delay of the distributed $rc$ model is **one half** of the delay that would have been predicted by the lumped RC model.

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