Lecture 3 - Differential Pair Part I

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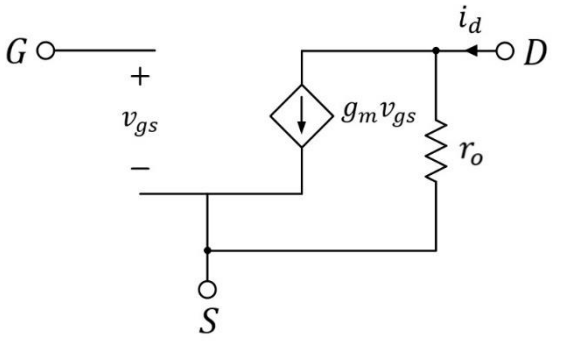
Outline of this Lecture

- Previously on ELCN 201
- Differential and Single
- The MOSFET Differential Pair
  - Operation with a Common Mode Input Voltage
  - Operation with a Differential Input Voltage
  - Common Mode Rejection

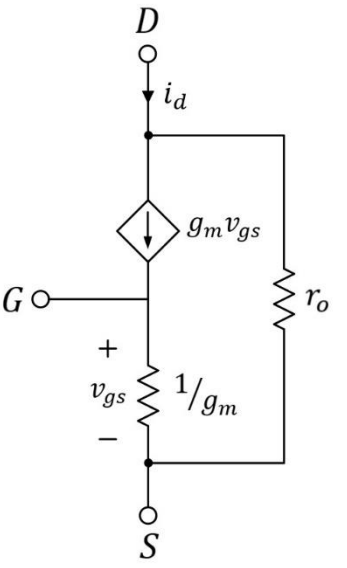
Previously on ELCN 201

Channel Length Modulation

The Hybrid-π Model



The T Model



$i_d' = g_m v_{gs}$	$i_g = 0$
$g_m = k_n V_{ov}$	$r_o = \dfrac{V_A}{I_D'}$

Previously on ELCN 201

Steps of AC Analysis

1. Eliminate the AC source and determine the DC operating point of the MOSFET particularly V_{GS}.
2. Calculate the values of the small-signal model parameters g_m.
3. Eliminate the DC sources by replacing each DC voltage source with a short circuit.
4. Replace the MOSFET with one of its small-signal equivalent circuit models and determine the required quantities.

Previously on ELCN 201

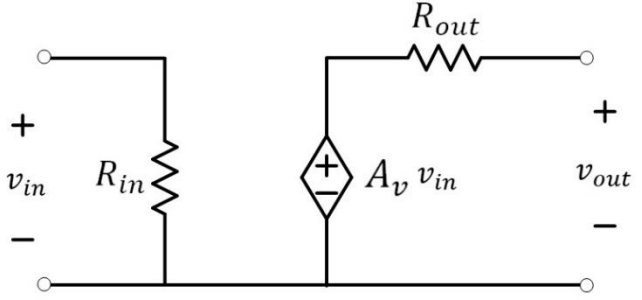
Model of the Amplifier

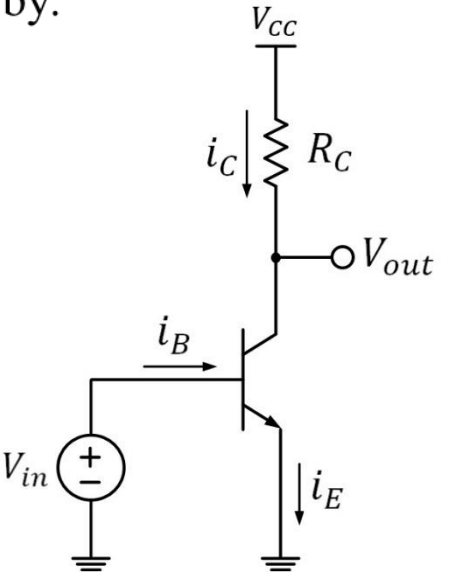
In AC analysis, the amplifier is replaced by:

a) Gain (A_v)

b) Input resistance (R_{in})

c) Output resistance (R_{out})



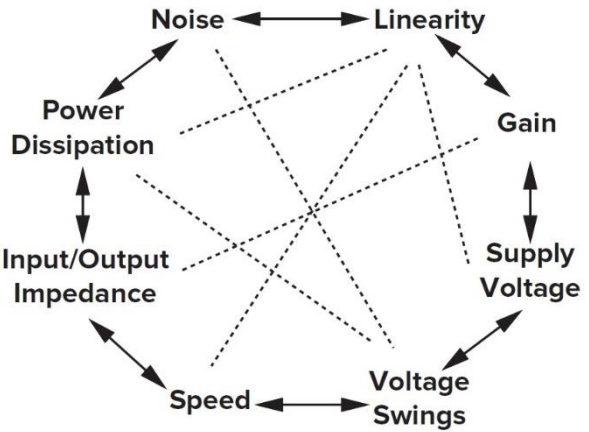


Previously on ELCN 201

Analog Design Octagon

Gain, speed, power dissipation, supply voltage, linearity, noise, or maximum voltage swings are the important aspects of the performance of an amplifier

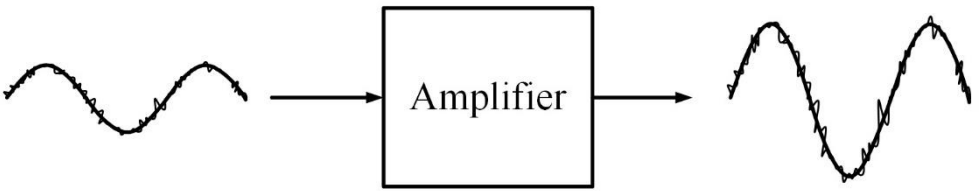
These parameters trade with each other, making the design a multidimensional optimization problem.



Introduction

Differential and Single

Noise and interference are the major problems in electronics circuits specially in the analog circuits.



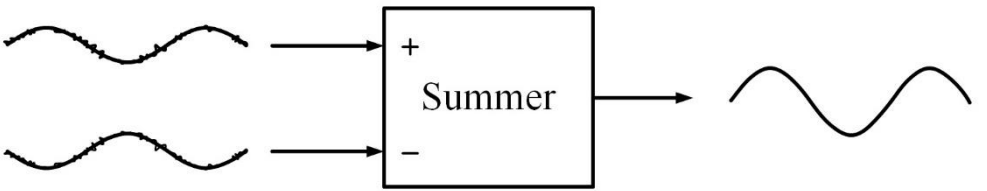
Single ended amplifier suffers from the noise and interference problems.

If two wires are physically close together, the interference voltages on the two wires will be equal.

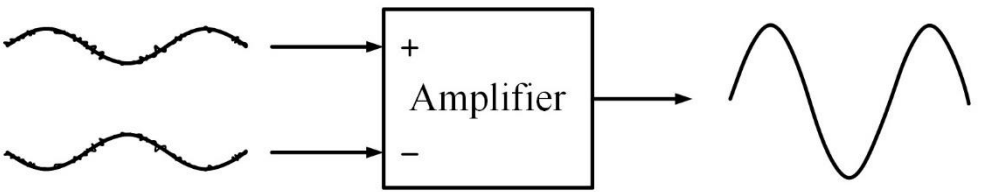
Introduction

Differential and Single

Any signal can be generated from the difference of two out-of-phase signals each has half the required magnitude



The difference signal between the two wires will contain **no** interference component.



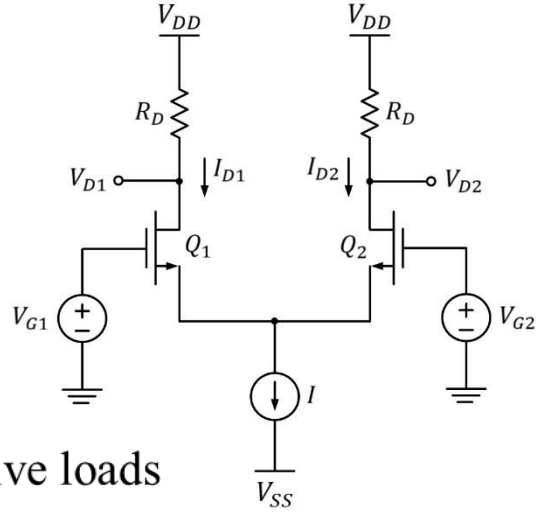
The MOSFET Differential Pair

Configuration

The diff-pair consists of two matched transistors, Q_1 and Q_2, operated in the **saturation** mode whose sources are **joined** together and biased by a **constant** current source I.

The current source I ususually implemented using a MOSFET source/mirror.

The drain of each transistor is connected to the positive supply through a resistance R_D.



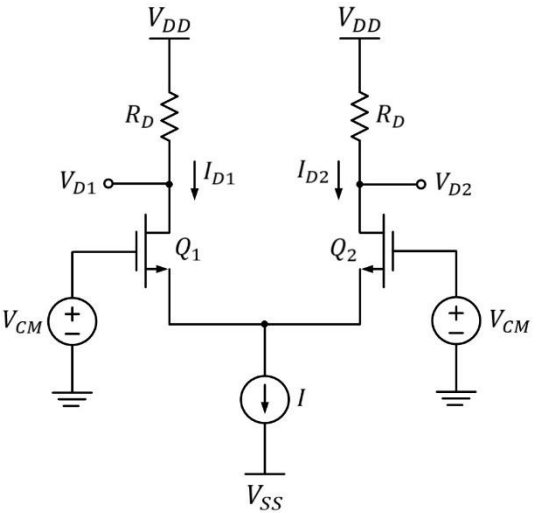
In most cases R_D is replaced by active loads

The MOSFET Differential Pair

Operation with a Common Mode Input Voltage

When a **common mode voltage** V_{CM} is applied to the two gate terminals

$$V_{CM} - V_{CM} = V_{GS1} - V_{GS2}$$
$$= 0$$
$$V_{GS1} = V_{GS2} = V_{GS}$$



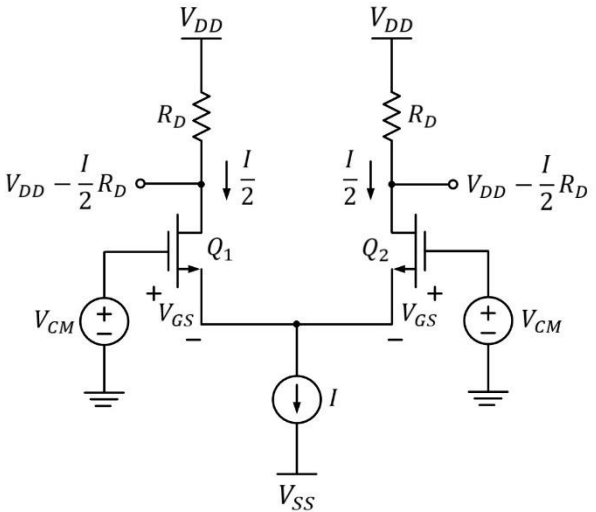
The MOSFET Differential Pair

Operation with a Common Mode Input Voltage

When a **common mode voltage** V_{CM} is applied to the two gate terminals

$$I_{D1} = I_{D2} = \frac{I}{2}$$

$$V_{D1} = V_{D2} = V_{DD} - \frac{I}{2}R_D$$



The MOSFET Differential Pair

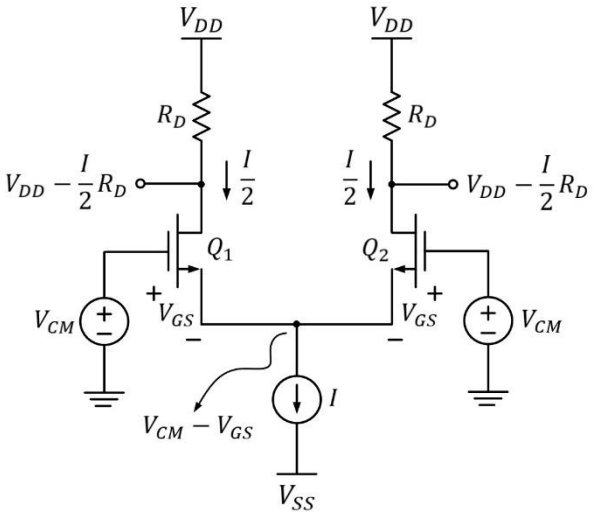
Operation with a Common Mode Input Voltage

$$\frac{I}{2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{ov}^2$$

$$V_{ov} = \sqrt{\frac{I}{k_n' \left(\frac{W}{L}\right)}}$$

$$V_S = V_{CM} - V_{GS}$$

$$= V_{CM} - (V_{ov} + V_T)$$



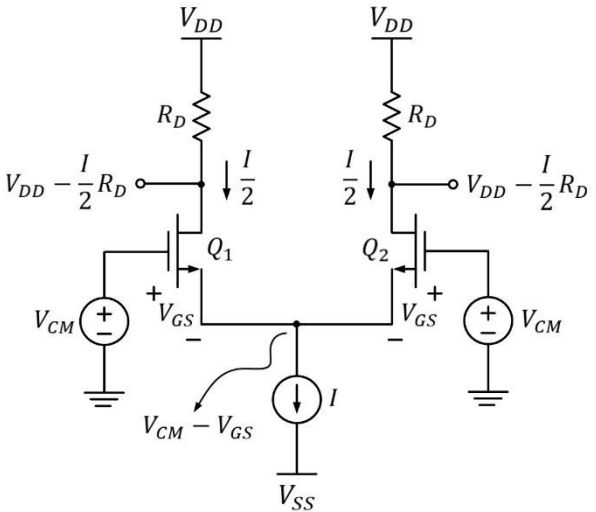
The MOSFET Differential Pair

Operation with a Common Mode Input Voltage

If V_{CM} is varied while keeping Q_1 and Q_2 in the saturation mode, the current I will divide equally.

The output voltages (V_{D1} and V_{D2}) will not change.

The differential pair does not respond to (**rejects**) common-mode input signals.



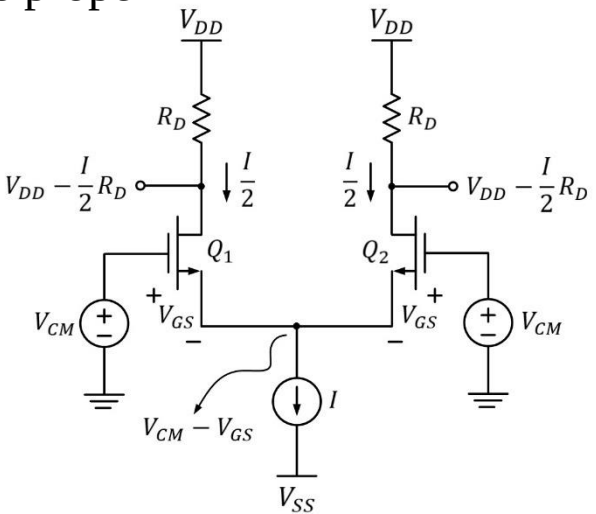
The MOSFET Differential Pair

Operation with a Common Mode Input Voltage

An important specification of a differential amplifier is its input common mode **range** that keeps its proper operation

The highest value of V_{CM} is limited by the requirement that Q_1 and Q_2 remain in saturation

$$V_{CM\,max} = V_{DD} - \frac{I}{2}R_D + V_T$$



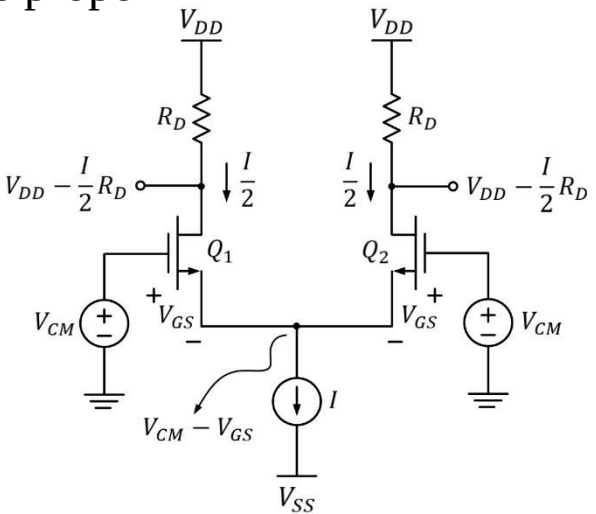
The MOSFET Differential Pair

Operation with a Common Mode Input Voltage

An important specification of a differential amplifier is its input common mode **range** that keeps its proper operation

The lowest value of V_{CM} is determined by the need to allow for a sufficient voltage across the current source I for it to operate properly.

$$V_{CM_{min}} = V_{S_{req}} + V_{ov} + V_T$$



The MOSFET Differential Pair

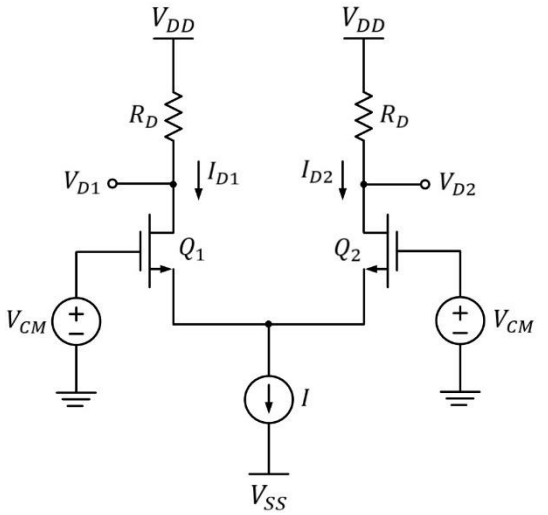
Example (1)

For the MOS differential pair shown, let $V_{DD} = -V_{SS} = 1.5\,V$, $k'_n(W/L) = 4mA/V^2$, $V_T = 0.5V$, $I = 0.4\,mA$, and $R_D = 2.5\,k\Omega$. Assume that the current source requires a minimum voltage of $0.4V$ to operate properly.

a) Find V_{ov} and V_{GS} for each transistor.

b) What is the highest and lowest permitted values of V_{CM}

c) For $V_{CM} = 0$, find V_S , I_{D1}, I_{D2}, V_{D1}, and V_{D2}.



The MOSFET Differential Pair

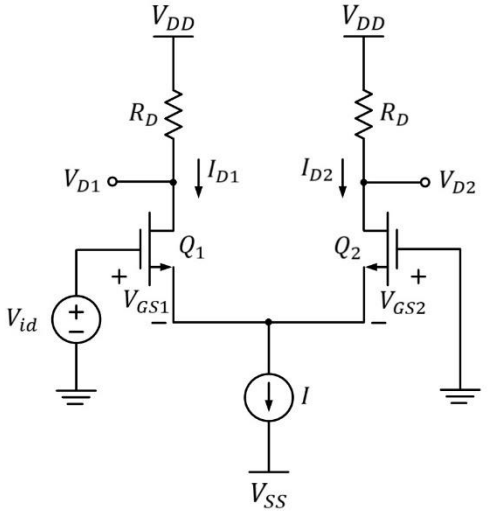
Operation with a Differential Input Voltage

To apply a differential voltage, the gate of Q_2 is grounded and a signal V_{id} is applied to the gate of Q_1.

$$V_{id} = V_{GS1} - V_{GS2}$$

When V_{id} is **positive**, V_{GS1} will be greater than V_{GS2} and I_{D1} will be greater than I_{D2} and the difference output voltage ($V_{od} = V_{D1} - V_{D2}$) will be **negative**.

When V_{id} is **negative**, the difference output voltage will be **positive**.



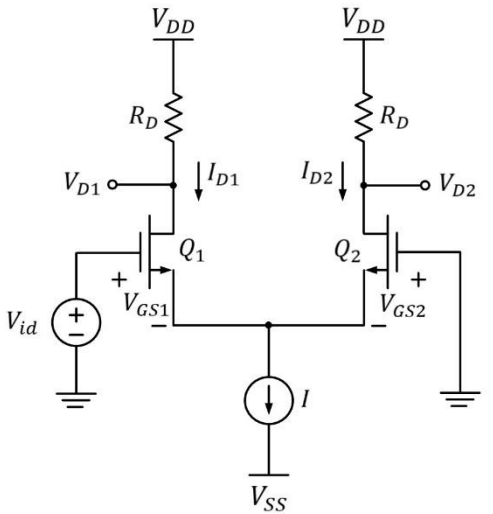
The MOSFET Differential Pair

Operation with a Differential Input Voltage

The differential pair responds to **difference-mode** signals by providing a corresponding **differential output** signal between the two drains.

I will flow completely in Q_1 when V_{GS1} reaches the value that corresponds to $I_{D1} = I$, and V_{GS2} is reduced to a value equal to the threshold voltage V_T

$$I = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{GS1} - V_T)^2$$



The MOSFET Differential Pair

Operation with a Differential Input Voltage

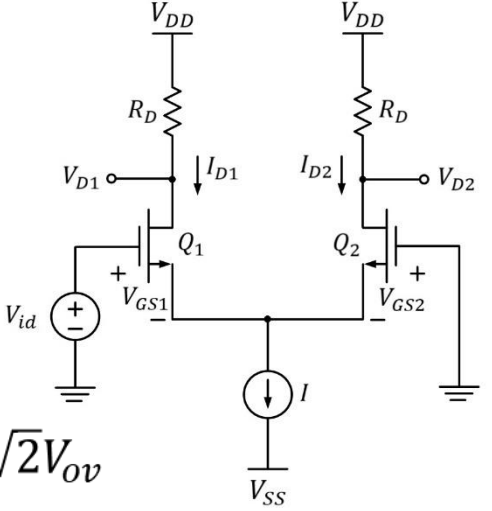
$$V_{GS1} = V_T + \sqrt{\frac{2I}{k_n'(W/L)}} = V_T + \sqrt{2}\sqrt{\frac{I}{k_n'(W/L)}}$$

$$= V_T + \sqrt{2}V_{ov}$$

V_{ov} is the overdrive voltage when $I_{D1} = I/2$

$$V_{id}\Big|_{max} = V_{GS1}\Big|_{max} - V_{GS2}\Big|_{min}$$

$$= \left(V_T + \sqrt{2}V_{ov}\right) - V_T = \sqrt{2}V_{ov}$$



The MOSFET Differential Pair

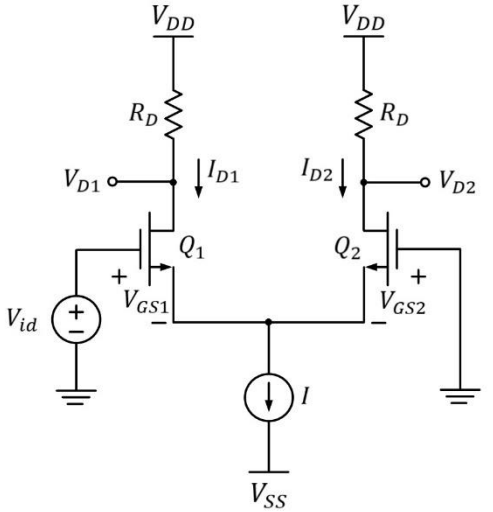
Operation with a Differential Input Voltage

If V_{id} is increased beyond $\sqrt{2}V_{ov}$, I_{D1} **remains** equal to I, V_{GS1} **remains** equal to $V_T + \sqrt{2}V_{ov}$, while V_S **rises** correspondingly, thus Q_2 is kept off.

In the negative direction, as V_{id} reaches $-\sqrt{2}V_{ov}$, Q_1 turns off and Q_2 conducts the entire bias current I.

The range of differential-mode operation is

$$-\sqrt{2}V_{ov} \leq V_{id} \leq \sqrt{2}V_{ov}$$



The MOSFET Differential Pair

Large Signal Operation

$V_{id} = V_{GS1} - V_{GS2}$	$I = I_{D1} + I_{D2}$
$I_{D1} = \frac{1}{2}k'_n\left(\frac{W}{L}\right)(V_{GS1} - V_T)^2$	$I_{D2} = \frac{1}{2}k'_n\left(\frac{W}{L}\right)(V_{GS2} - V_T)^2$

Solving these equations

$$I_{D1} = \frac{I}{2} + \left(\frac{I}{V_{ov}}\right)\left(\frac{V_{id}}{2}\right)\sqrt{1 - \left(\frac{V_{id}/2}{V_{ov}}\right)^2}$$

$$I_{D2} = \frac{I}{2} - \left(\frac{I}{V_{ov}}\right)\left(\frac{V_{id}}{2}\right)\sqrt{1 - \left(\frac{V_{id}/2}{V_{ov}}\right)^2}$$

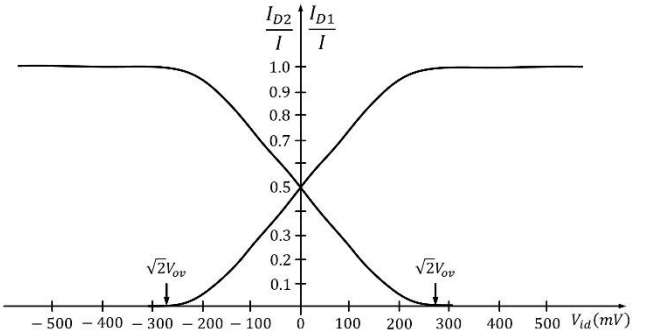
The MOSFET Differential Pair

Large Signal Operation

$$I_{D1,D2} = \frac{I}{2} \pm \left(\frac{I}{V_{ov}}\right)\left(\frac{V_{id}}{2}\right)\sqrt{1 - \left(\frac{V_{id}/2}{V_{ov}}\right)^2}$$

To obtain a linear amplification from the differential pair, and for a given V_{ov} , $V_{id}/2$ needs to be kept much smaller than V_{ov}.

$$I_{D1,D2} = \frac{I}{2} \pm \underbrace{\left(\frac{I}{V_{ov}}\right)\left(\frac{V_{id}}{2}\right)}_{i_d}$$



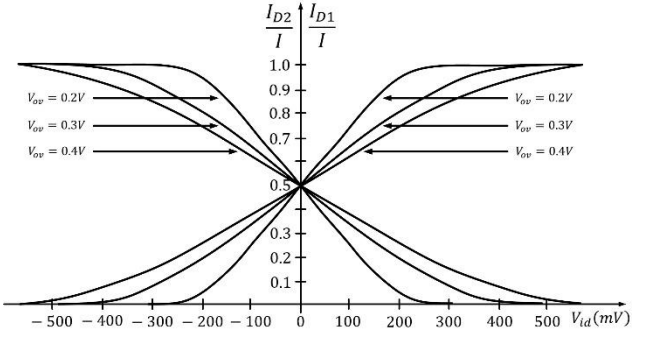
The MOSFET Differential Pair

Large Signal Operation

$$I_{D1,D2} = \frac{I}{2} \pm \left(\frac{I}{V_{ov}}\right)\left(\frac{V_{id}}{2}\right)\sqrt{1 - \left(\frac{V_{id}/2}{V_{ov}}\right)^2}$$

To obtain a linear amplification from the differential pair, and for a given V_{id}, V_{ov} needs to be increased.

Increasing V_{ov} results in a **reduction** in the gain.



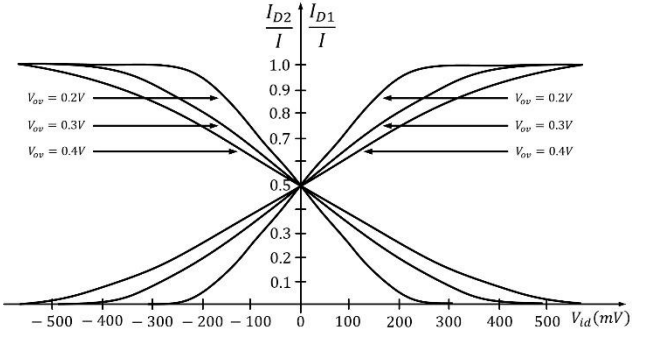
The MOSFET Differential Pair

Large Signal Operation

$$I_{D1,D2} = \frac{I}{2} \pm \left(\frac{I}{V_{ov}}\right)\left(\frac{V_{id}}{2}\right)\sqrt{1 - \left(\frac{V_{id}/2}{V_{ov}}\right)^2}$$

To obtain a linear amplification from the differential pair, and for a given V_{id}, V_{ov} needs to be increased.

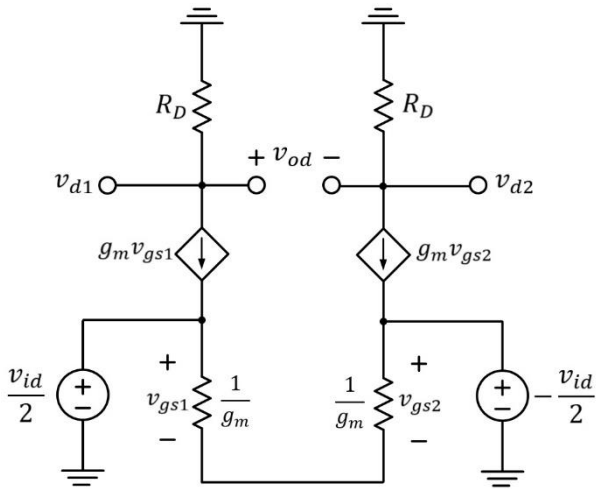
Increasing I restore the gain back. However, increasing I, increases the power dissipation.

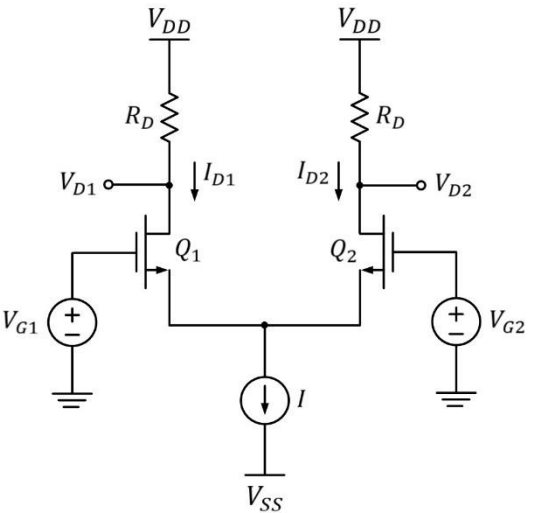


The MOSFET Differential Pair

Small Signal Operation

To obtain the small signal parameters, each of the two MOSFETs is replaced with the corresponding T model





The MOSFET Differential Pair

Small Signal Operation

$$\frac{v_{id}}{2} - \left(-\frac{v_{id}}{2}\right) = v_{gs1} - v_{gs2}$$

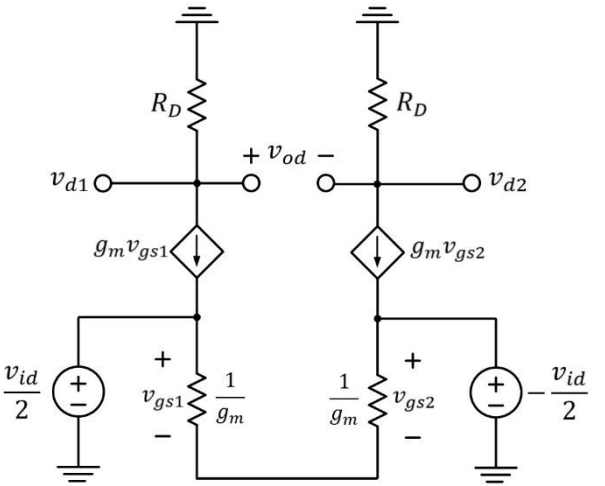
$$v_{id} = v_{gs1} - v_{gs2}$$

As the current is the same in the loop

$$g_m v_{gs1} = -g_m v_{gs2}$$

$$v_{gs1} = -v_{gs2}$$

$$v_{gs1} = \frac{v_{id}}{2}, \qquad v_{gs2} = -\frac{v_{id}}{2}$$



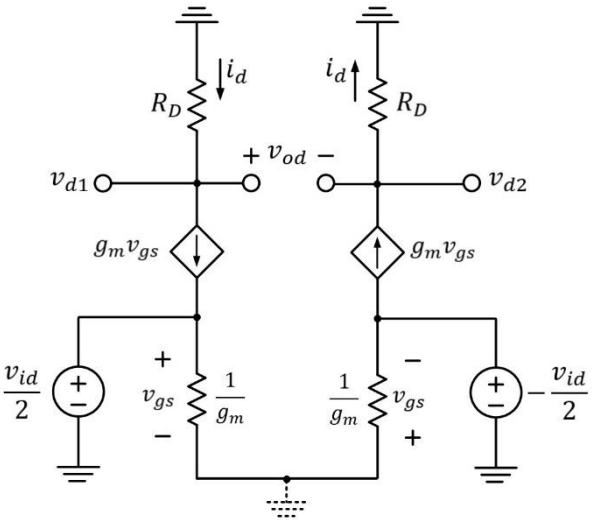
The MOSFET Differential Pair

Small Signal Operation

Dividing v_{id} between the two transistor result in making the signal voltage at the joint source connection to be zero, acting as **virtual ground.**

$$g_m = \frac{2I_D}{V_{ov}} = \frac{2(I/2)}{V_{ov}} = \frac{I}{V_{ov}}$$

$$i_d = g_m v_{gs} = \left(\frac{I}{V_{ov}}\right)\left(\frac{v_{id}}{2}\right)$$



The MOSFET Differential Pair

Small Signal Operation

$$v_{d1} = -g_m v_{gs} R_D$$

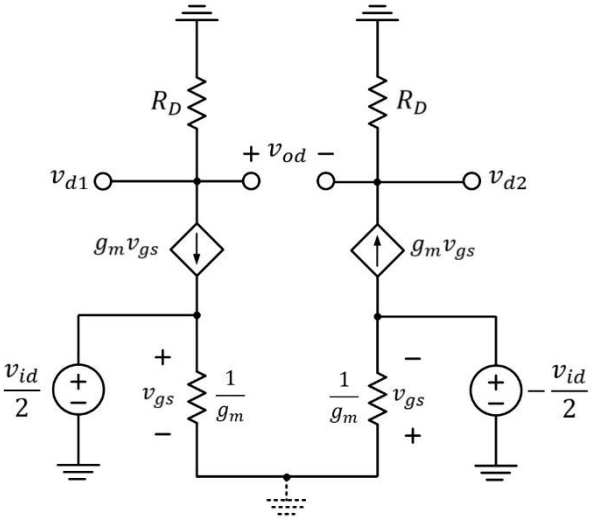
$$= -g_m R_D \frac{v_{id}}{2}$$

$$v_{d2} = g_m v_{gs} R_D$$

$$= g_m R_D \frac{v_{id}}{2}$$

$$v_{od} = v_{d1} - v_{d2}$$

$$= -g_m R_D v_{id}$$



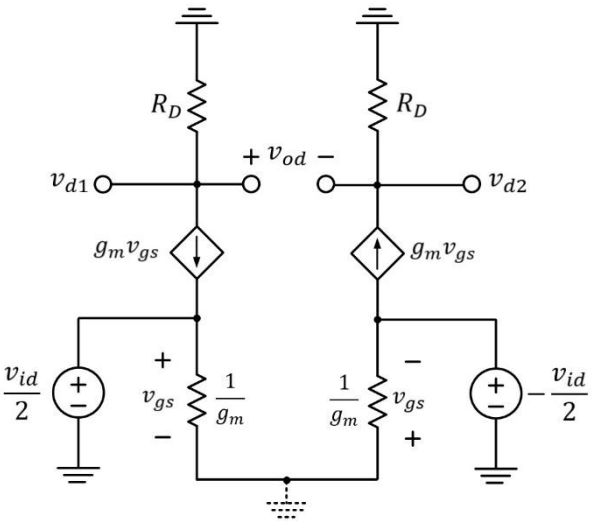
The MOSFET Differential Pair

Small Signal Operation

The gain if the output is taken as a **single ended** from one of the two output terminals

$$\frac{v_{d1}}{v_{id}} = -\frac{1}{2} g_m R_D$$

$$\frac{v_{d2}}{v_{id}} = \frac{1}{2} g_m R_D$$



If the output is taken **differentially**, the gain becomes

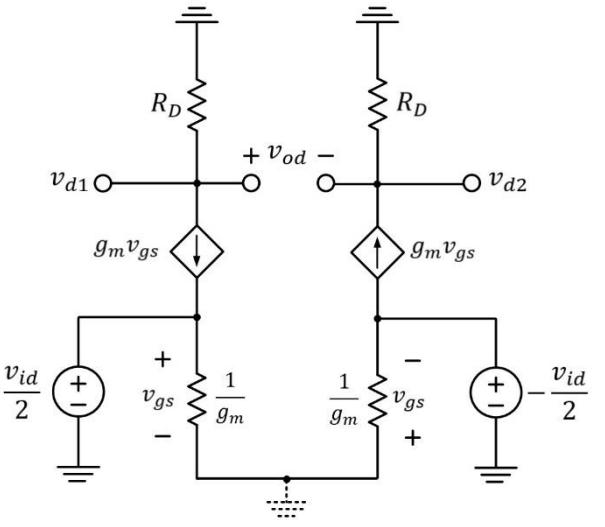
$$\frac{v_{od}}{v_{id}} = -g_m R_D$$

The MOSFET Differential Pair

Small Signal Operation

An advantage of taking the output differentially is an **increase in gain by a factor of 2**.

Single ended	Differential
$\frac{1}{2} g_m R_D$	$g_m R_D$

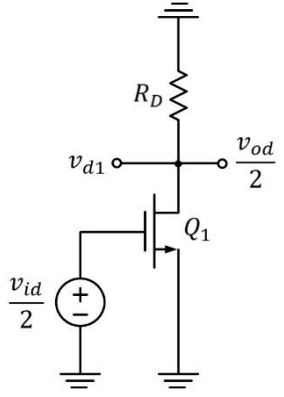


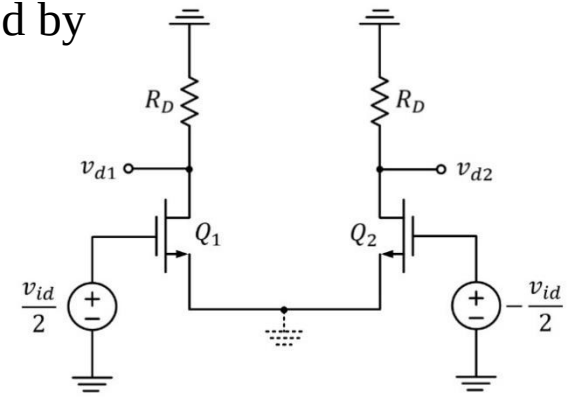
The MOSFET Differential Pair

Small Signal Operation

Differential Half Circuit

Due to the **symmetry** in the differential amplifier and because it is fed with a differential signal in a **balanced** manner, the small signal parameters can be determined by considering only **half** the circuit.



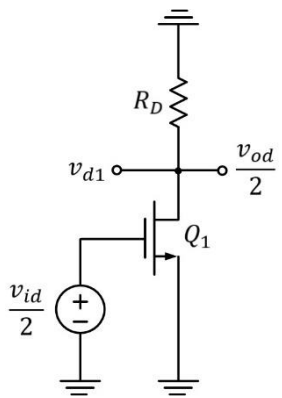


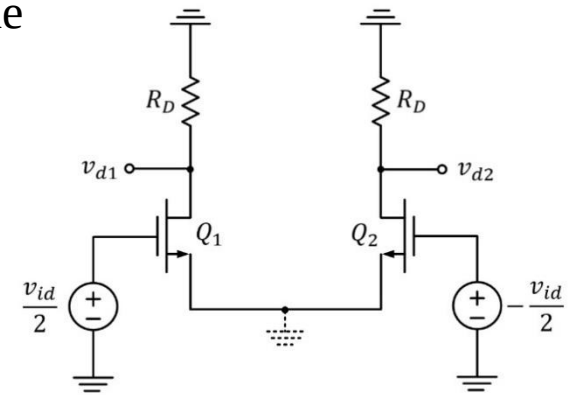
The MOSFET Differential Pair

Small Signal Operation

Differential Half Circuit

The equivalent differential half-circuit has a grounded source, a result of the virtual ground that appears on the common sources' terminal of the MOSFETs in the differential pair.





The MOSFET Differential Pair

Small Signal Operation

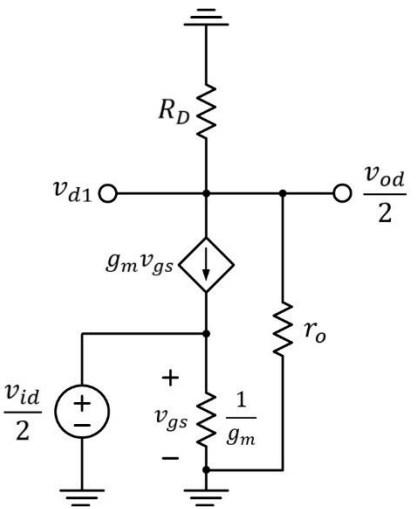
Differential Half Circuit

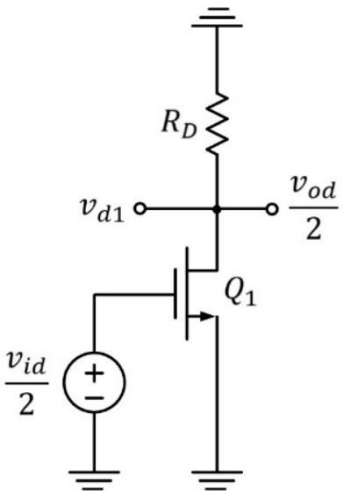
The differential gain can be determined directly from the half circuit.

$$\frac{v_{od}}{v_{id}} = -g_m R_D$$

The half circuit simplify the analysis when r_o is inserted in the model of the MOSFET

$$\frac{v_{od}}{v_{id}} = -g_m(R_D // r_o)$$





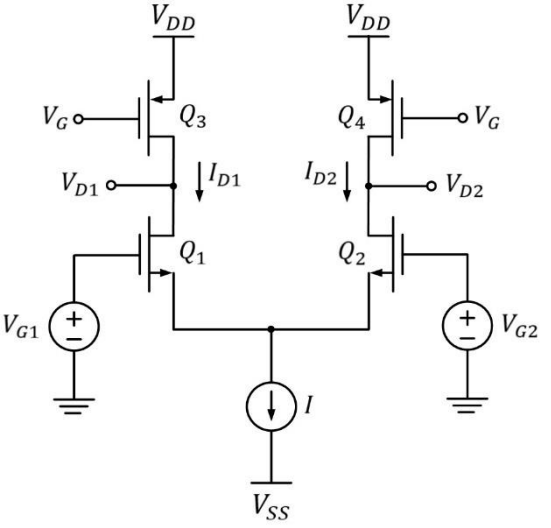
The MOSFET Differential Pair

Differential Amplifier with Active Load

To obtain higher gain, the passive resistances R_D can be replaced with active load (current sources).

The active loads are realized using PMOS transistors Q_3 and Q_4.

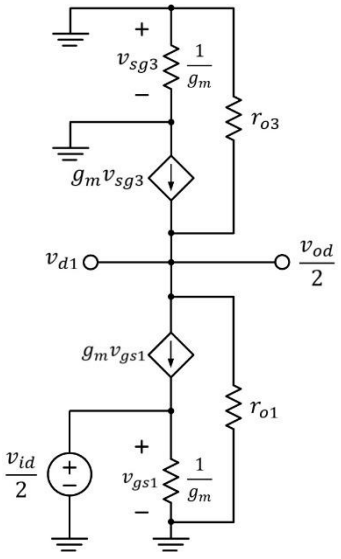
V_G is a DC bias voltage that sets Q_3 and Q_4 each to conducts a current equal to $I/2$.

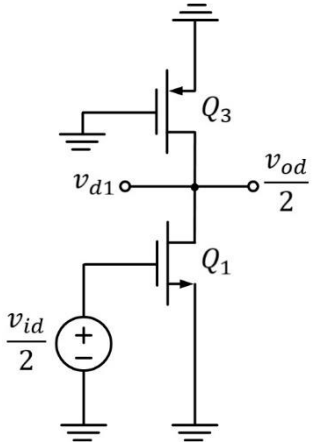


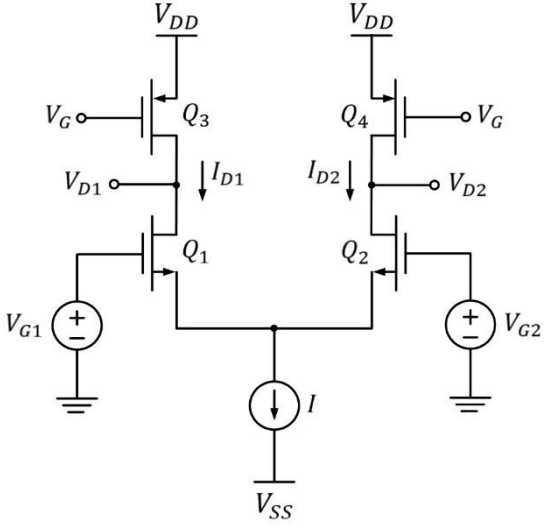
The MOSFET Differential Pair

Differential Amplifier with Active Load

To determine the small signal gain, the differential half-circuit is constructed using Q_1 and Q_3.







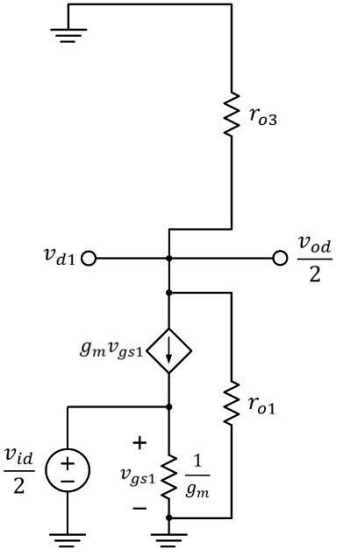
The MOSFET Differential Pair

Differential Amplifier with Active Load

To determine the small signal gain, the differential half-circuit is constructed using Q_1 and Q_3.

The differential voltage gain is given by

$$\frac{v_{od}}{v_{id}} = g_m(r_{o1}//r_{o3})$$

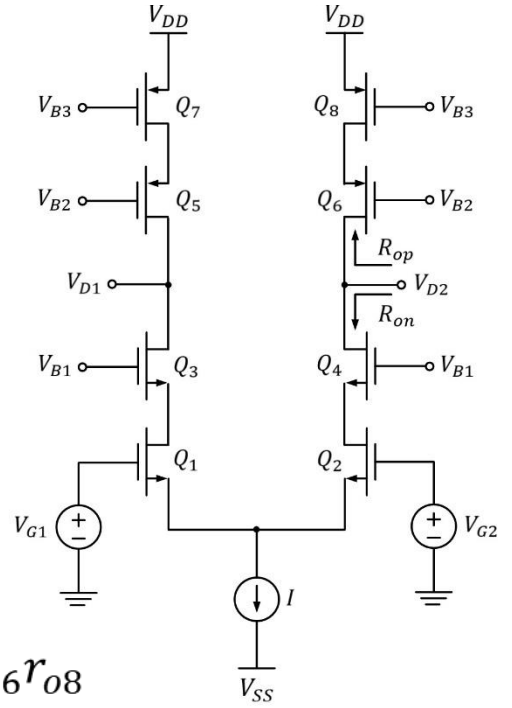


The MOSFET Differential Pair

Cascode Differential Amplifier

Another way to increase the gain of the differential amplifier is to utilize the cascode configuration

Cascoding is applied to the amplifying transistors via Q_3 and Q_4, and to the active load via transistors Q_5 and Q_6.



$$\frac{v_{od}}{v_{id}} = -g_m\left(R_{on}//R_{op}\right)$$

$$R_{on} = g_{m4}r_{o4}r_{o2}, \qquad R_{op} = g_{m6}r_{o6}r_{o8}$$

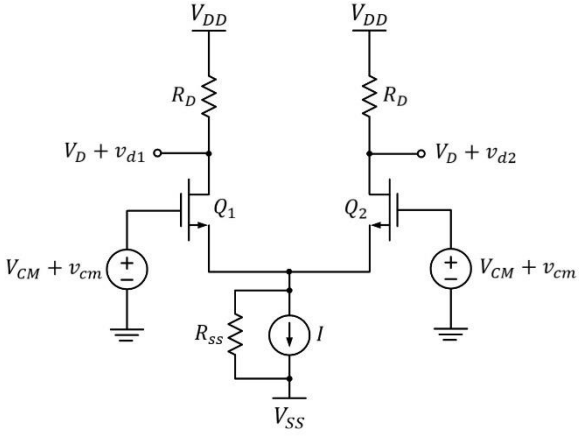
The MOSFET Differential Pair

Common Mode Rejection

When the ideal current source I is replaced with a real current source having a **finite** output resistance, the common mode gain will **no longer** be zero.

With v_{cm} set to zero, the bias current in each of Q_1 and Q_2 will be **larger** than $I/2$ by an amount determined by V_{CM} and R_{SS}.

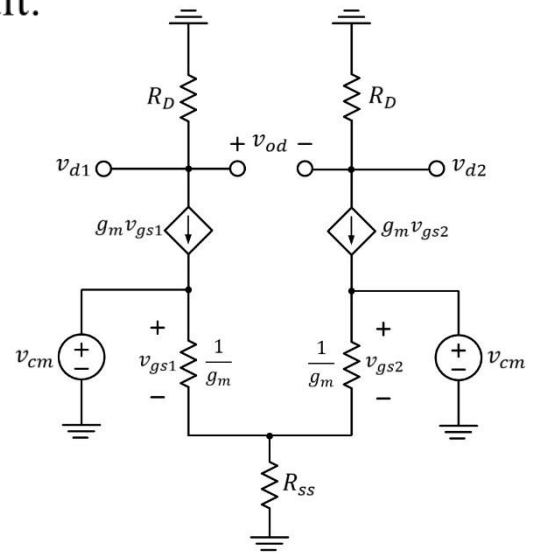
R_{SS} is usually very large. Thus, the additional DC current is usually small and can be neglected.

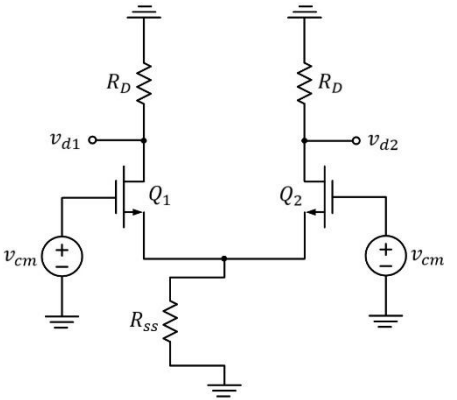


The MOSFET Differential Pair

Common Mode Rejection

To determine the change in the output due to v_{cm}, V_{DD} and V_{SS} are replaced by a short circuit and I is replaced by an open circuit.





The MOSFET Differential Pair

Common Mode Rejection

$$v_{cm} - v_{cm} = v_{gs1} - v_{gs2}$$

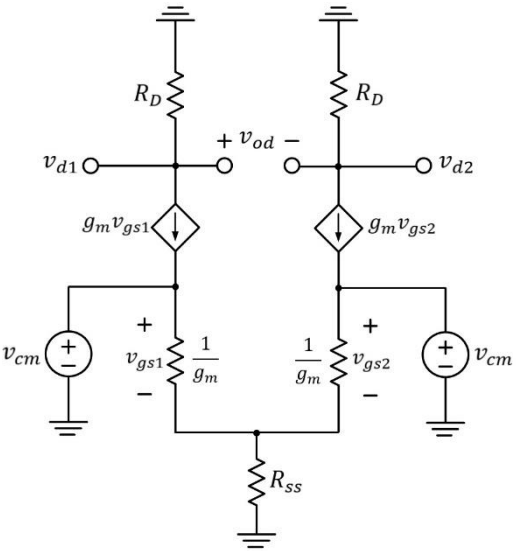
$$= 0$$

$$v_{gs1} = v_{gs2} = v_{gs}$$

$$v_{cm} = v_{gs} + 2(g_m v_{gs}) \times R_{SS}$$

$$v_{gs} = \frac{v_{cm}}{1 + 2g_m R_{SS}}$$

$$v_{d1} = v_{d2} = -g_m v_{gs} R_D$$



The MOSFET Differential Pair

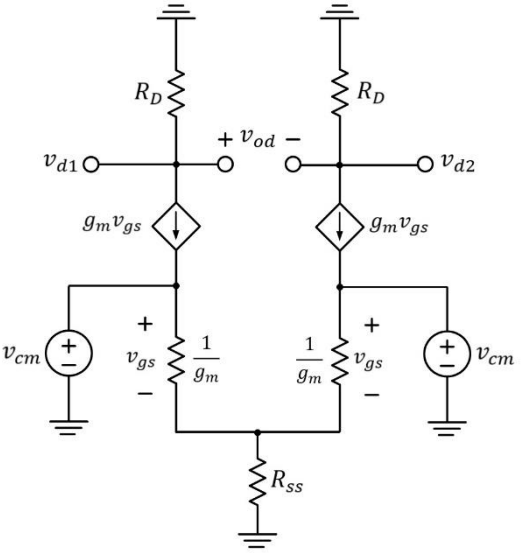
Common Mode Rejection

$$v_{d1} = v_{d2} = \frac{-g_m R_D}{1 + 2g_m R_{SS}} v_{cm}$$

$$\frac{v_{d1}}{v_{cm}} = \frac{v_{d2}}{v_{cm}} = \frac{-g_m R_D}{1 + 2g_m R_{SS}}$$

If $R_{SS} = \infty$ (case of ideal current source)

$$\frac{v_{d1}}{v_{cm}} = \frac{v_{d2}}{v_{cm}} = 0$$



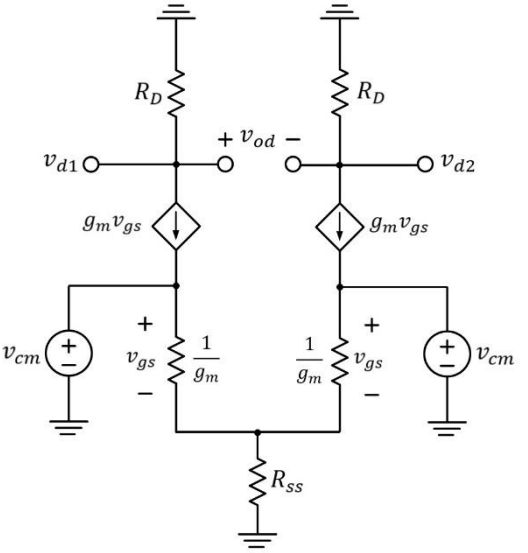
The MOSFET Differential Pair

Common Mode Rejection

$$v_{d1} = v_{d2} = \frac{-g_m R_D}{1 + 2g_m R_{SS}} v_{cm}$$

$$v_{od} = v_{d1} - v_{d2} = 0$$

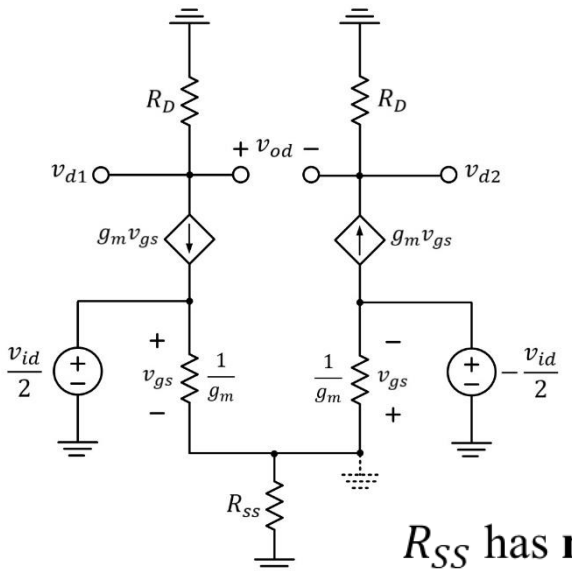
The differential output voltage is **free** of the common mode signal

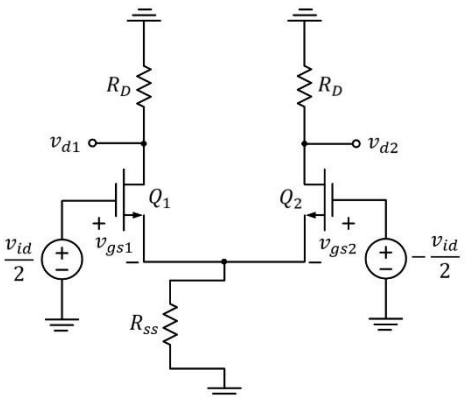


The MOSFET Differential Pair

Common Mode Rejection

For the differential input, a virtual ground develops on the common-source terminal





R_{SS} has **no effect** on the differential gain

The MOSFET Differential Pair

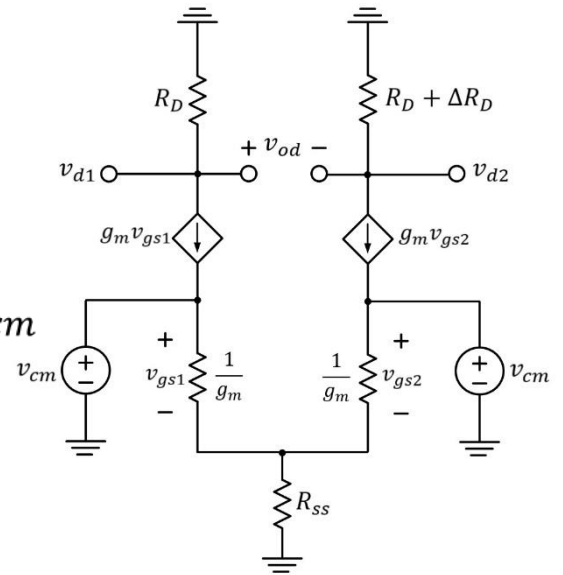
Common Mode Rejection

Effect of R_D Mismatch

$$v_{d1} = \frac{-g_m R_D}{1 + 2g_m R_{SS}} v_{cm}$$

$$v_{d2} = \frac{-g_m (R_D + \Delta R_D)}{1 + 2g_m R_{SS}} v_{cm}$$

$$v_{od} = v_{d1} - v_{d2} = \frac{g_m \Delta R_D}{1 + 2g_m R_{SS}} v_{cm}$$



The common mode gain A_{cm} is

$$A_{CM} = \frac{v_{od}}{v_{cm}} = \frac{g_m \Delta R_D}{1 + 2g_m R_{SS}}$$

The MOSFET Differential Pair

Common Mode Rejection

Common Mode Rejection Ratio

Common mode rejection ratio (CMRR) is a measure of the **effectiveness** of the differential amplifier in **amplifying** differential mode signals and **rejecting** common mode interference

$$CMRR = \frac{|A_d|}{|A_{CM}|}$$

The MOSFET Differential Pair

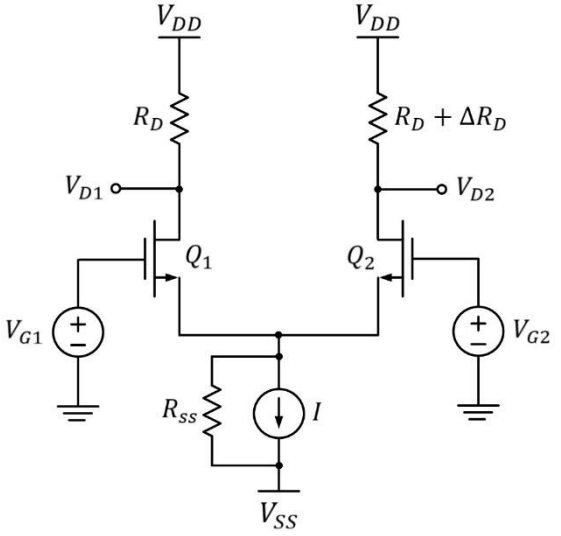
Common Mode Rejection

Effect of R_D Mismatch

$$A_{CM} = \frac{v_{od}}{v_{cm}} = \frac{g_m \Delta R_D}{1 + 2 g_m R_{SS}}$$

$$A_d = \frac{v_{od}}{v_{id}} = -g_m R_D$$

$$CMRR = \frac{|A_d|}{|A_{CM}|} = (1 + 2 g_m R_{SS}) / \left(\frac{\Delta R_D}{R_D} \right)$$



R_{SS} should be as big as possible, ΔR_D should be as small as possible.