



# Lecture 1 - MOSFET

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<http://scholar.cu.edu.eg/refky/>

# Outline of this Lecture

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- Course Contents, References, Course Plan
- Introduction
- MOSFET Transistors
  - Structure
  - Regions of Operation
  - Current-Voltage Characteristics
  - DC Analysis of MOSFET
- Channel Length Modulation

# Course Plan

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- Instructor: Dr. Mohamed Refky (Part 1)  
Dr. Ahmed Hussein (Part 2)
- TA: TBA
- Grading:
  - 40% Final exam
  - 60% term work
    - Midterm 20 %
    - Project 15%
    - Quizzes 15%
    - Assignments 10%
- Office Hours: Appointments are set by email

# Course Contents

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Week	Lecture	Quizzes
1	MOSFET	
2	Single-Stage Amplifier	
3	Differential Pair – Part I	
4	Differential Pair – Part II	Quiz (1)
5	Frequency Response	
6	Feedback Amplifier – Part I	Quiz (2)
7	Feedback Amplifier – Part II	
8	Midterm	
9	Current Sources	
10	Advanced Current Sources	
11	Digital Logic – Part I	Quiz (3)
12	Digital Logic – Part II	
13	Digital Logic – Part III	Quiz (4)
14	Digital Logic – Part IV	

# Course Activities

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## Assignments and Project

Some of the assignments and the project will require the use of simulation tools such as Cadence Spectre, Mentor Graphics Calibre, and Synopsis tools.

**The late penalty is -20% per day (or part of a day) for which the assignment or a project milestone is late.**

# Course Objectives

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The objective of this course is to analysis and design analog and digital CMOS integrated circuits through:

- Simple modelling techniques are used to gain a better understanding of the functions of the circuits.
- Intuitive design methods, quantitative performance measures and practical circuit limitations are emphasized.
- Circuit performance is predicted by means of both hand calculations and computer simulations.

# Textbook & References

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- Textbook:
  - Behzad Razavi, **Design of Analog CMOS Integrated Circuits**, McGraw Hill, 2000.
  - Adel S. Sedra, Kenneth C. Smith, **Microelectronic Circuits**, 8<sup>th</sup> Edition, Oxford University Press, 2019.
- Reference:
  - Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, **Analysis and Design of Analog Integrated Circuits**, 5th Edition, Wiley, 2009.
  - Tony Chan, David Johns, Kenneth Martin, **Analog Integrated Circuit Design**, 2<sup>nd</sup> Edition, Wiley, 2011.

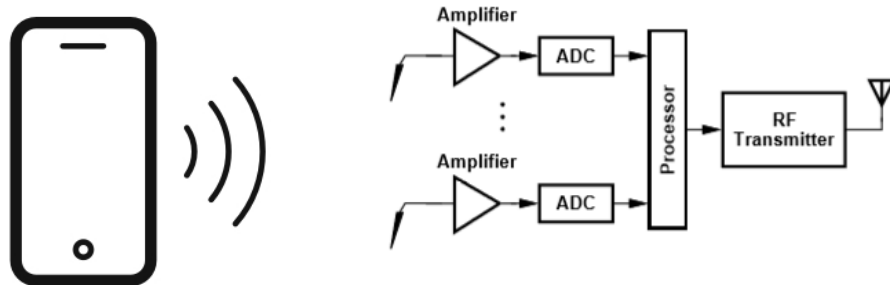
# Introduction

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## Importance of Analog Circuits

Although digital signal processing (DSP) has replaced most of the analog processing blocks since 1980s, some of critical blocks of the system are still analog blocks

Signal sensing and signal conditioning demands high performance analog design.





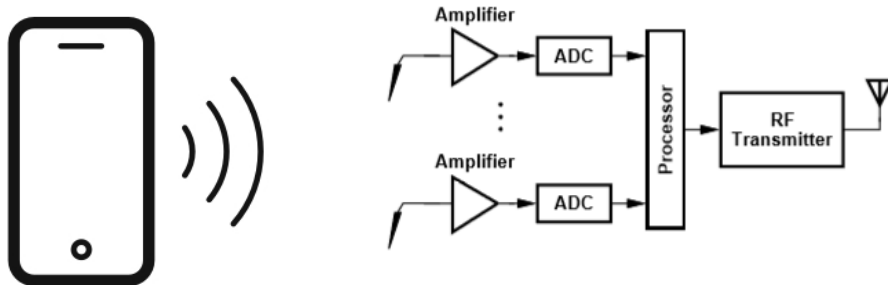
# Introduction

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## Importance of Analog Circuits

Analog circuits usually consume most of the power in any system.

Analog to digital converter (ADC) and digital to analog converters (DAC) are considered main building blocks in many systems.



# Introduction

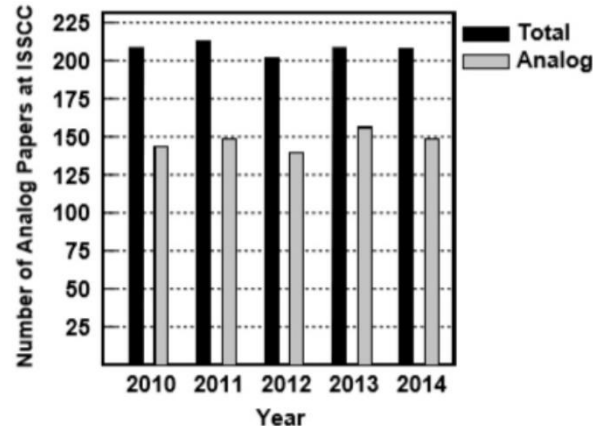
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## Importance of Analog Circuits

In the electronics society, the majority of published papers are belong to analog design.

The challenges in the analog circuits design include

- Transistor imperfections
- Declining supply voltages
- Power consumption
- Circuit complexity
- PVT variations



# MOSFET Transistor

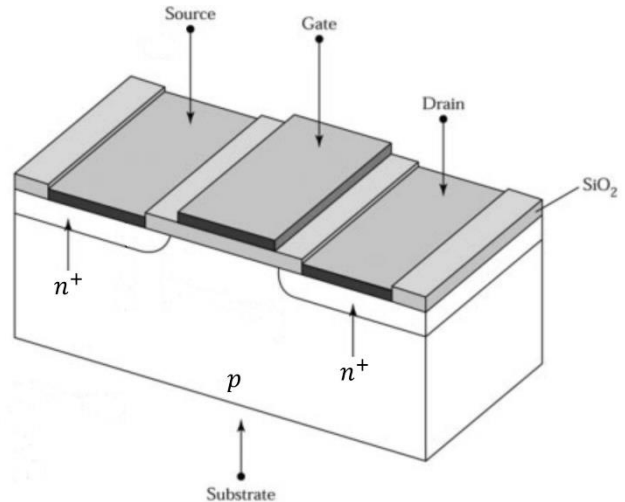
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## Device Structure

The MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor.

The MOSFET has two types :

- *n*-channel MOSFET (NMOS)
- *p*-channel MOSFET (PMOS)



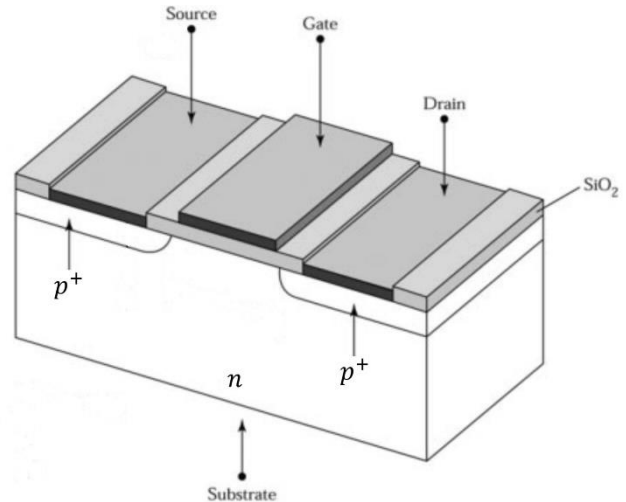
# MOSFET Transistor

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## Device Structure

The MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor.

The *p*-channel MOSFET consists of a *n*-type semiconductor substrate in which two *p*<sup>+</sup> regions are used to form the **Source** and **Drain**. The metal plate on the oxide is called the **Gate**.



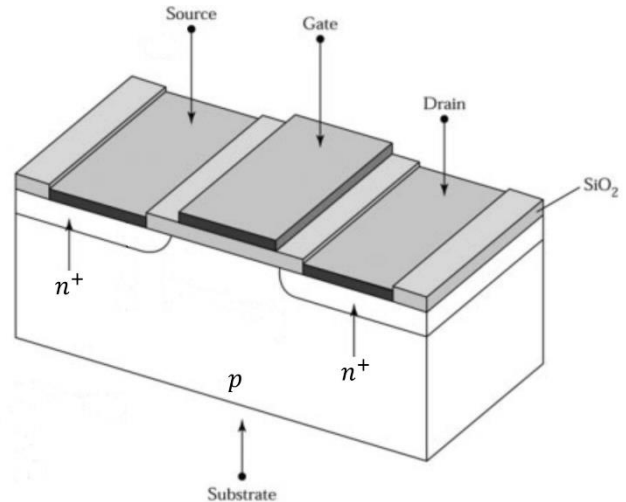
# MOSFET Transistor

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## Device Structure

The MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor.

The  $n$ -channel MOSFET consists of a  $p$ -type semiconductor substrate in which two  $n^+$  regions are used to form the **Source** and **Drain**. The metal plate on the oxide is called the **Gate**.



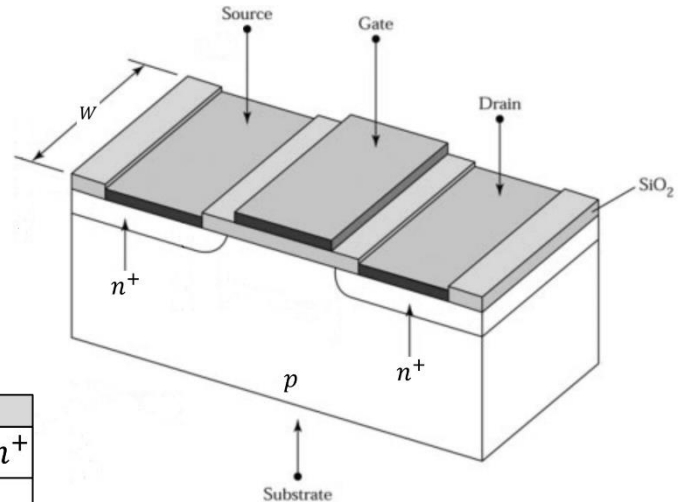
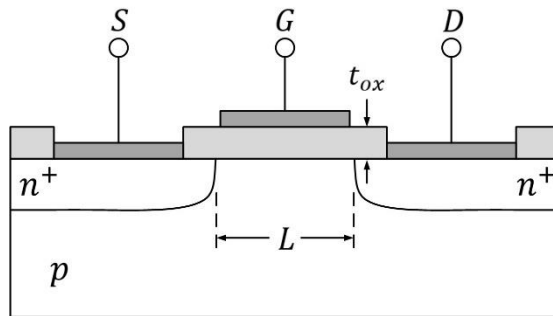
MOSFET is usually known to be a three terminal device (G S D) although it is really a four terminal device (G S D B)

# MOSFET Transistor

## MOSFET Parameters

The basic parameters of the MOSFET are:

- Channel length  $L$ .
- Channel width  $W$ .
- Oxide thickness  $t_{ox}$ .

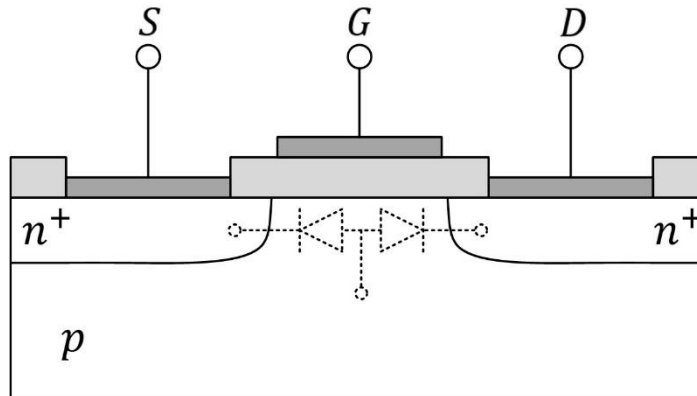


# MOSFET Transistor

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## MOSFET Channel

If there is no voltage applied to the gate, the source, substrate, and drain forms two  $pn$  junctions connected back to back.

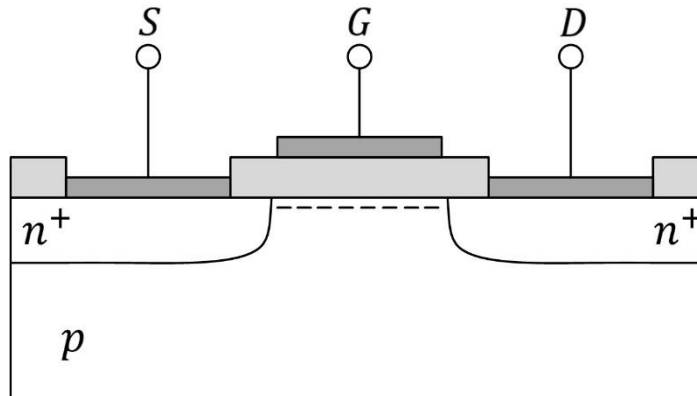


# MOSFET Transistor

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## MOSFET Channel

When a sufficiently large positive bias is applied to the gate, the MOS structure is inverted and a channel is formed between the two  $n^+$  regions.



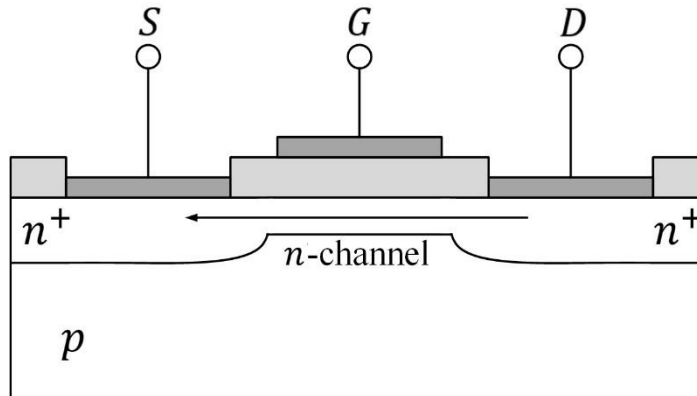


# MOSFET Transistor

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## MOSFET Channel

The value of the vertical field gate (generated from the gate voltage) controls the amount of charge in the channel, and thus it determines the channel conductivity. This is the origin of the name “field-effect transistor” (FET).



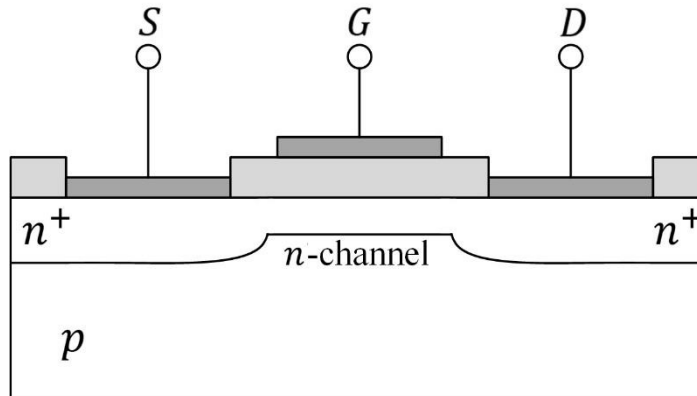
# MOSFET Transistor

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## Regions of Operation

If the gate voltage is small to cause an inversion at the semiconductor surface, the MOSFET is consider off.

When the gate voltage is enough to form a channel between the source and the drain, the MOSFET is considered on.



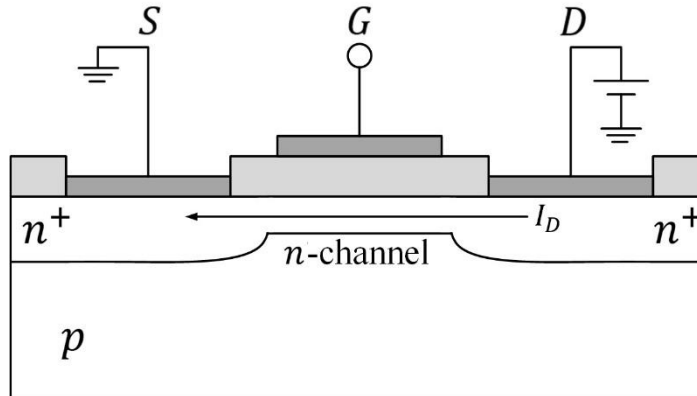
# MOSFET Transistor

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## Regions of Operation

If a small voltage is applied to the drain, electrons will flow from the source to the drain through the channel.

The drain current  $I_D$  is proportional to the drain-source voltage ( $V_{DS}$ ) and the channel acts as a resistor. This is the **Linear Region**.

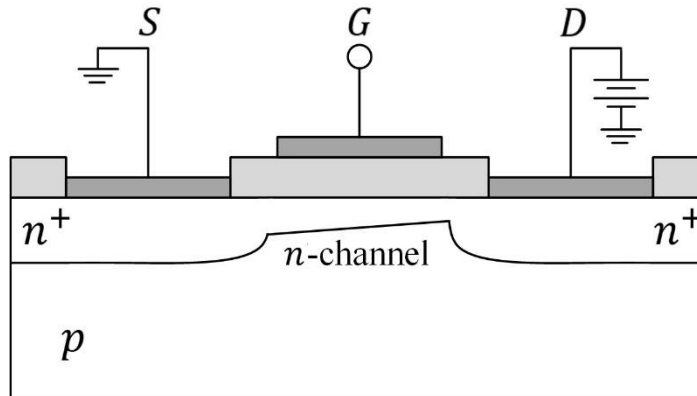


# MOSFET Transistor

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## Regions of Operation

As  $V_{DS}$  increases, the depletion region of the drain-substrate increases and the thickness of the channel near the drain is reduced.

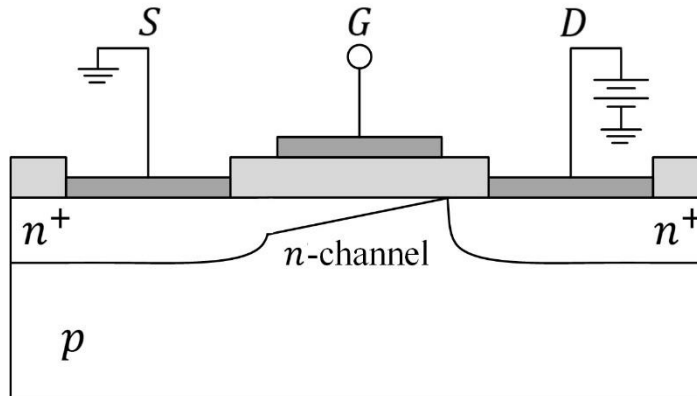


# MOSFET Transistor

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## Regions of Operation

Eventually  $V_{DS}$  reaches  $V_{DS_{sat}}$ , at which the thickness of the channel is reduced to zero. This is called the **Pinch-Off Point**.

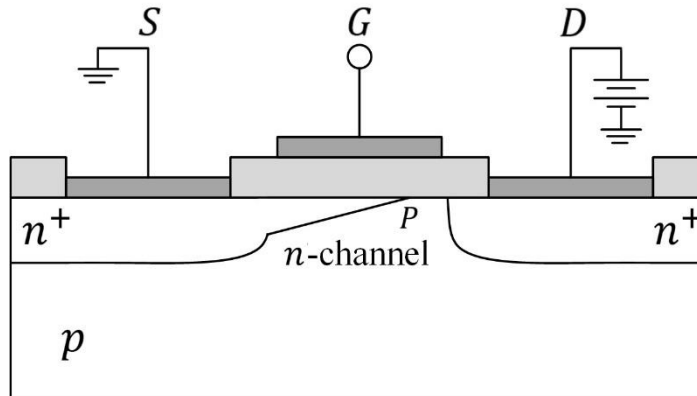


# MOSFET Transistor

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## Regions of Operation

Beyond the pinch-off point, the drain current remains essentially the same because for  $V_{DS} > V_{DS_{sat}}$  the voltage remains  $V_{DS_{sat}}$  at point  $P$ . Carrier injection occurs from  $P$  into the drain

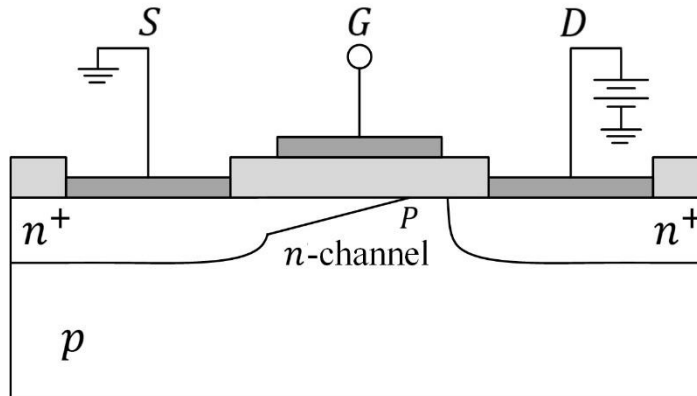


# MOSFET Transistor

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## Regions of Operation

Because  $I_D$  remains constant regardless of the increase in  $V_{DS}$ . This region is called the **Saturation Region**.



# MOSFET Transistor

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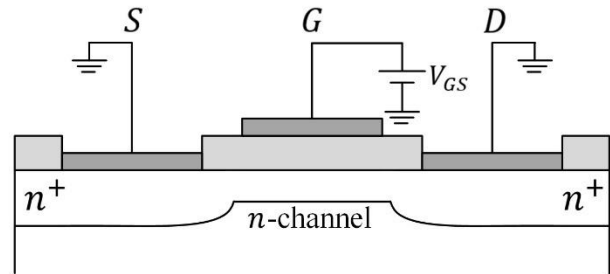
## Current-Voltage Characteristics

### Linear Region

The voltage across the oxide must exceed  $V_T$  for a channel to be formed. When  $V_{DS} = 0$ , the voltage at every point along the channel is zero, and the voltage across the oxide is uniform and equal to  $V_{GS}$ .

The excess of  $V_{GS}$  over  $V_T$  is termed the **effective voltage** or the **overdrive voltage**

$$V_{ov} = V_{GS} - V_T$$





# MOSFET Transistor

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## Current-Voltage Characteristics

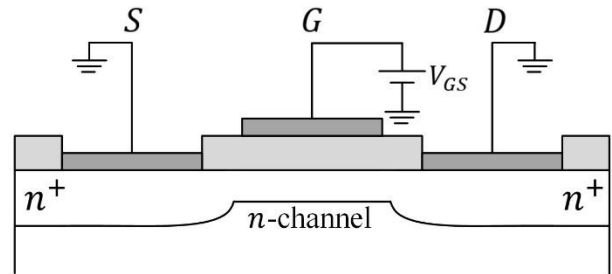
### Linear Region

The magnitude of the total electron charge in the channel is given by

$$Q = C_{ox}(WL)V_{ov}$$

$C_{ox}$  is the **oxide capacitance** and it is the capacitance of the parallel-plate capacitor per unit gate area (in units of  $F/m^2$ )

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$



# MOSFET Transistor

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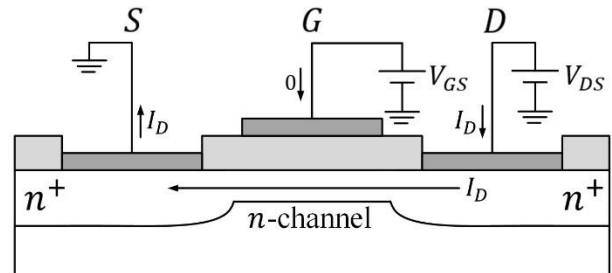
## Current-Voltage Characteristics

### Linear Region

When very small  $V_{DS}$  is applied to the drain, the current  $I_D$  flow through the induced  $n$ -channel from drain to source.

Because  $V_{DS}$  is small, we can continue to assume that the voltage between the gate and various points along the channel remains approximately constant and equal to  $V_{ov}$

$$Q = C_{ox}(WL)V_{ov}$$



# MOSFET Transistor

## Current-Voltage Characteristics

### Linear Region

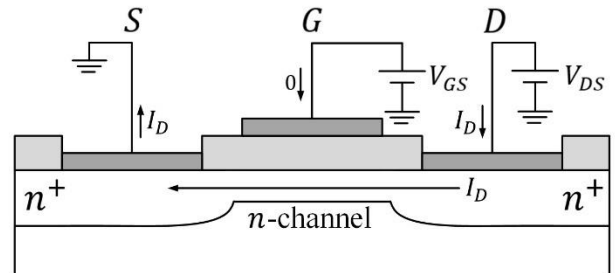
$$I_D = -\frac{dq}{dt} = -Q_S v_n$$

$Q_S$  is the charge density per unit length and is given by

$$Q_S = \frac{Q}{L} = W C_{ox} V_{ov}$$

$$v_n = -\mu_n \mathbb{E} = -\mu_n \frac{V_{DS}}{L}$$

$\mathbb{E}$  is a horizontal field



# MOSFET Transistor

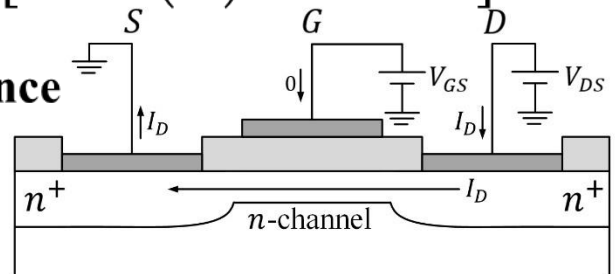
## Current-Voltage Characteristics

### Linear Region

$$I_D = |I_D| = Q_S |v_n| = \left[ \mu_n C_{ox} \left( \frac{W}{L} \right) V_{ov} \right] V_{DS}$$
$$k'_n = \mu_n C_{ox} \qquad = \left[ \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_T) \right] V_{DS}$$

$k'_n$  is the **process transconductance** parameter and has the unit  $A/V^2$

$W/L$  is termed the **aspect ratio**



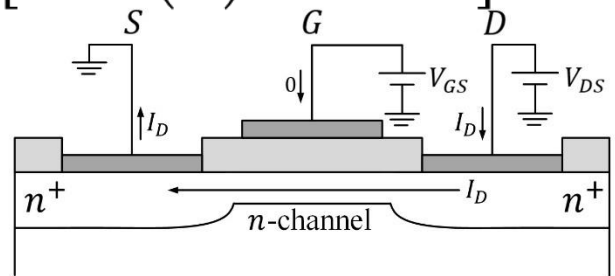
# MOSFET Transistor

## Current-Voltage Characteristics

### Linear Region

$$\begin{aligned} I_D = |I_D| = Q_S |v_n| &= \left[ \mu_n C_{ox} \left( \frac{W}{L} \right) V_{ov} \right] V_{DS} \\ &= \left[ \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_T) \right] V_{DS} \\ k_n &= \mu_n C_{ox} \left( \frac{W}{L} \right) \end{aligned}$$

$k_n$  is the **MOSFET transconductance** parameter and has the unit  $A/V^2$



# MOSFET Transistor

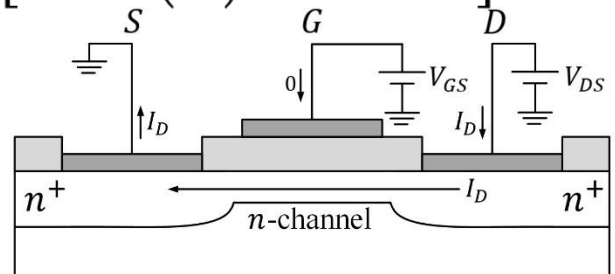
## Current-Voltage Characteristics

### Linear Region

$$I_D = |I_D| = Q_S |v_n| = \left[ \mu_n C_{ox} \left( \frac{W}{L} \right) V_{ov} \right] V_{DS}$$
$$= \left[ \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_T) \right] V_{DS}$$

The MOSFET behaves as a **linear resistance**  $r_{DS}$  whose value is controlled by the gate voltage  $V_{GS}$

$$r_{DS} = \frac{1}{\mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_T)}$$



# MOSFET Transistor

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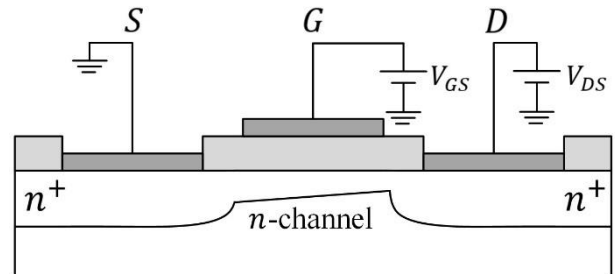
## Current-Voltage Characteristics

### Linear Region

As  $V_{DS}$  is increased, the voltage between the gate and points along the channel decreases from  $V_{GS}$  at the source end to  $V_{GS} - V_{DS}$  at the drain end.

The channel becomes more tapered and its resistance increases correspondingly.

Thus, the  $I_D - V_{DS}$  curve does not continue as a straight line but bends



# MOSFET Transistor

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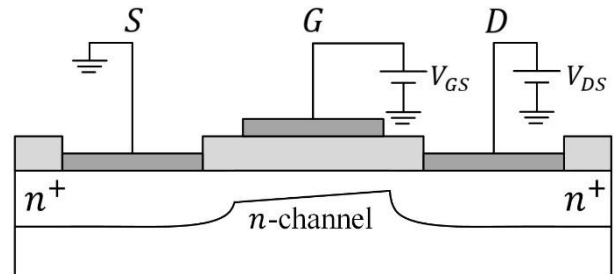
## Current-Voltage Characteristics

### Linear Region

The total charge in the tapered channel ( $Q$ ) is proportional to the channel cross-sectional area.

The cross-sectional area is proportional to

$$\begin{aligned} V_{Cn} &= \frac{1}{2} [V_{ov} + (V_{ov} - V_{DS})] \\ &= V_{ov} - \frac{1}{2} V_{DS} \end{aligned}$$





# MOSFET Transistor

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## Current-Voltage Characteristics

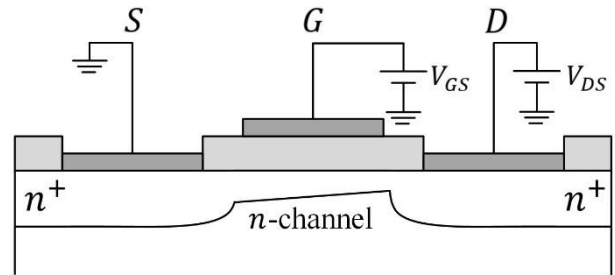
### Linear Region

Replacing  $V_{ov}$  by  $V_{Cn}$  in the equation of  $I_D$  results in

$$I_D = \mu_n C_{ox} \left( \frac{W}{L} \right) \left( (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right)$$

The term  $V_{DS}^2/2$  describes the bend of the  $I_D - V_{DS}$  curve in the linear region

The above equation applies to the **entire** linear region (down to  $V_{DS} = 0$ ).



# MOSFET Transistor

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## Current-Voltage Characteristics

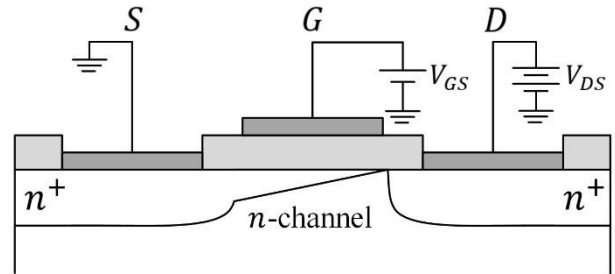
### Saturation Region

The pinch-off point is the boundary between the linear and the saturation regions. The pinch off occurs when  $V_{DS}$  equals the overdrive voltage

$$V_{GS} - V_{DS} = V_T \quad \rightarrow \quad V_{DS} = V_{GS} - V_T = V_{ov}$$

Replacing  $V_{DS}$  by  $V_{GS} - V_T$  in the equation of  $I_D$  results in

$$I_D = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_T)^2$$



The value of  $I_D$  in the saturation region does not depend on  $V_{DS}$

# MOSFET Transistor

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## Current-Voltage Characteristics

### $n$ -channel (NMOS)

<b>Cut off</b>	$V_{GS} < V_{Tn}$	0	
<b>Linear</b>	$V_{GS} > V_{Tn}$	$V_{DS} < V_{GS} - V_{Tn}$	$I_D = \frac{W}{L} \mu_n C_{ox} \left( V_{GS} - V_{Tn} - \frac{V_{DS}}{2} \right) V_{DS}$
<b>Saturation</b>		$V_{DS} > V_{GS} - V_{Tn}$	$I_D = \frac{1}{2} \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_{Tn})^2$

### $p$ -channel (PMOS)

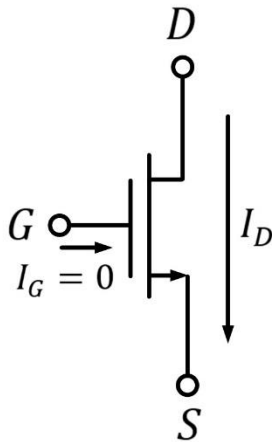
<b>Cut off</b>	$V_{SG} <  V_{Tp} $	0	
<b>Linear</b>	$V_{SG} >  V_{Tp} $	$V_{SD} < V_{SG} -  V_{Tp} $	$I_D = \frac{W}{L} \mu_p C_{ox} \left( V_{SG} -  V_{Tp}  - \frac{V_{SD}}{2} \right) V_{SD}$
<b>Saturation</b>		$V_{SD} > V_{SG} -  V_{Tp} $	$I_D = \frac{1}{2} \frac{W}{L} \mu_p C_{ox} (V_{SG} -  V_{Tp} )^2$

# DC Analysis of MOSFET

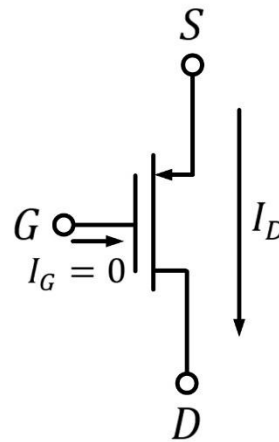
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## Circuit Symbols

In both symbols the source is distinguished by an arrowhead.



*n*-channel



*p*-channel

# DC Analysis of MOSFET

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## DC Analysis steps

- 1) Determine, if you can, whether the MOSFET is operating in the linear mode or in saturation mode.
- 2) If you cannot determine the mode of operation, **assume** the transistor is operating in the saturation mode and check if  $V_{DS} > V_{GS} - V_{Tn}$  for NMOS ( $V_{SD} > V_{SG} - |V_{Tp}|$  for PMOS).
- 3) If the assumption is wrong, resolve the circuit with the transistor operating in the linear mode and check if  $V_{DS} < V_{GS} - V_{Tn}$  for NMOS ( $V_{SD} < V_{SG} - |V_{Tp}|$  for PMOS).

# DC Analysis of MOSFET

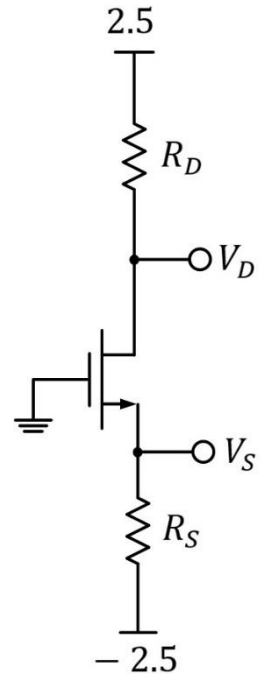
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## Example (1)

Design the circuit so that the transistor operates at  $I_D = 0.4mA$  and  $V_D = 0.5V$ .

The NMOS transistor has  $V_{Tn} = 0.7V$ ,  $\mu_n C_{ox} = 100\mu A/V^2$ ,  $L = 1\mu m$ , and  $W = 32\mu m$ .

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# DC Analysis of MOSFET

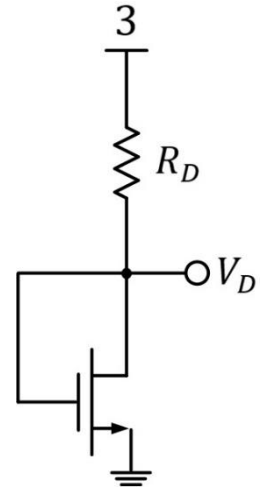
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## Example (2)

Design the circuit to obtain a current  $I_D = 80\mu A$   
Find the voltage  $V_D$ .

The NMOS transistor has  $V_{Tn} = 0.6V$ ,  $\mu_n C_{ox} = 200\mu A/V^2$ ,  $L = 0.8\mu m$ , and  $W = 4\mu m$ .

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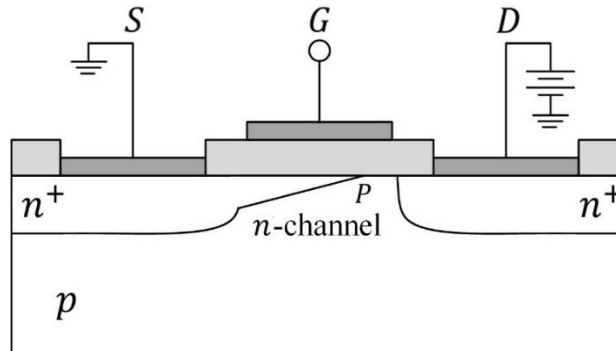
# MOSFET Transistors

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## Channel Length Modulation

In saturation region, the actual length of the channel ( $L' = L - \Delta L$ ) is a function of  $V_{DS}$ , which is an effect called “channel length modulation.

Thus, the value of  $I_D$  slightly changes with the change of  $V_{DS}$





# MOSFET Transistors

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## Channel Length Modulation

Substitute  $L'$  in the expression of  $I_D$

$$\begin{aligned} I_D &= \frac{1}{2} k_n \left( \frac{W}{L'} \right) (V_{GS} - V_{Tn})^2 \\ &= \frac{1}{2} k_n \left( \frac{W}{L - \Delta L} \right) (V_{GS} - V_{Tn})^2 \\ &= \frac{1}{2} k_n \left( \frac{W}{L} \right) \left( \frac{1}{1 - \Delta L/L} \right) (V_{GS} - V_{Tn})^2 \\ &= \frac{1}{2} k_n \left( \frac{W}{L} \right) \underbrace{(1 + \Delta L/L)}_{\lambda V_{DS} = V_{DS}/V_A} (V_{GS} - V_{Tn})^2 \end{aligned}$$

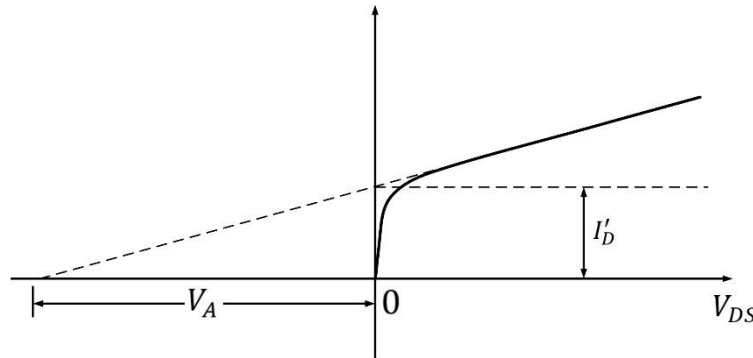
# MOSFET Transistors

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## Channel Length Modulation

To model the effect of the channel length modulation, the expression of  $I_D$  needs to be modified

$$I_D = \underbrace{\frac{1}{2} k_n \left( \frac{W}{L} \right) (V_{GS} - V_{Tn})^2}_{I'_D} \left( 1 + \frac{V_{DS}}{V_A} \right)$$



# MOSFET Transistors

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## Channel Length Modulation

Due to

$$\frac{\Delta L}{L} = \frac{V_{DS}}{V_A} \quad \rightarrow \quad V_A \propto L$$

And given that

$$I_D = \frac{1}{2} k_n \left( \frac{W}{L} \right) (V_{GS} - V_{Tn})^2 \left( 1 + \frac{V_{DS}}{V_A} \right)$$

The slope of the  $I_D - V_{DS}$  curve is given by

$$\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{2} k_n \left( \frac{W}{L} \right) (V_{GS} - V_{Tn})^2 \times \frac{1}{V_A} \quad \rightarrow \quad \frac{\partial I_D}{\partial V_{DS}} \propto \frac{1}{L^2}$$

# MOSFET Transistors

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## Channel Length Modulation

The effect of the channel length modulation is reduced with the increase of the transistor length

To maintain the same current  $I'_D$  and overdrive voltage, the width of the transistor must be increase with the same ratio

