Cairo University
Faculty of Engineering

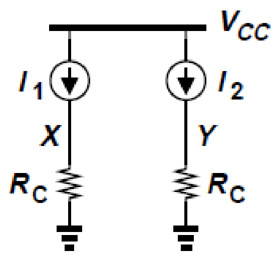
Department of Electronics and
Communications Engineering

Problem Set 3: Differential Amplifiers (Chapter 10)

Fundamental Concepts:

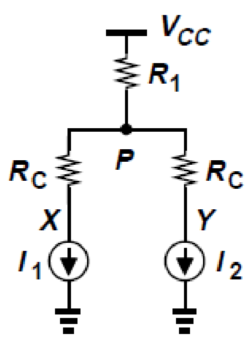
Problem 10.4

In the circuit of Fig. 10.60, $I_1 = I_0 \cos \omega t + I_0$ and $I_2 = -I_0 \cos \omega t + I_0$. Plot the waveforms at X and Y and determine their peak-to-peak swings and common-mode level.



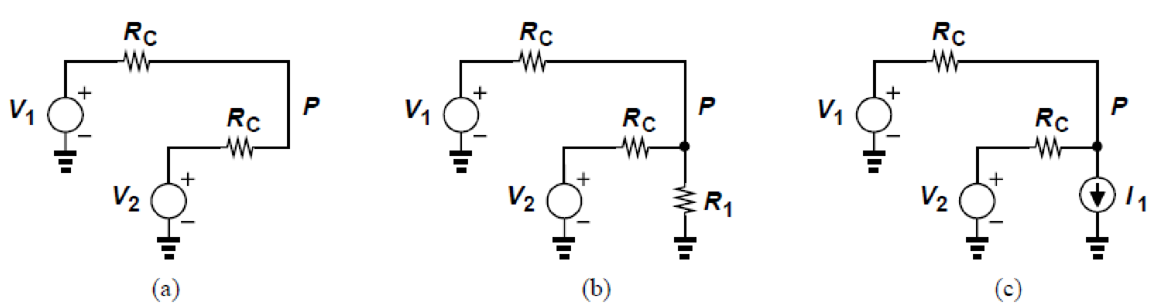
Problem 10.5

In the circuit of Fig. 10.60, $I_1 = I_0 \cos \omega t + I_0$ and $I_2 = -I_0 \cos \omega t + I_0$. Plot the waveforms at X and Y and determine their peak-to-peak swings and common-mode level.
Also, plot the voltage at node P as a function of time.



Problem 10.10

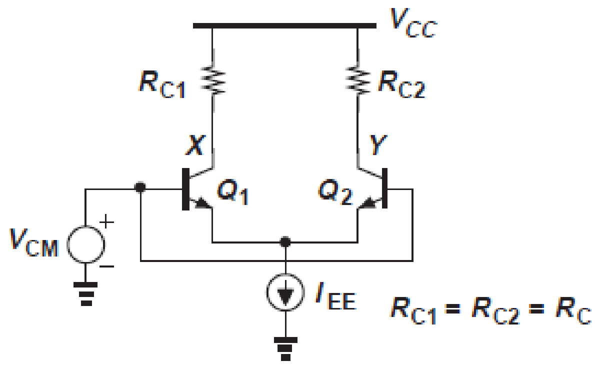
Assuming $V_1 = V_0 \cos \omega t + V_0$ and $V_2 = -V_0 \cos \omega t + V_0$, plot V_P as a function of time for the circuits shown in Fig. 10.65. Assume I_T is constant.



BJT Differential Amplifier:

Problem 10.12

In Fig. 10.7, I_{EE} experiences a change of ΔI. How do V_X, V_Y, and $V_X - V_Y$ change?

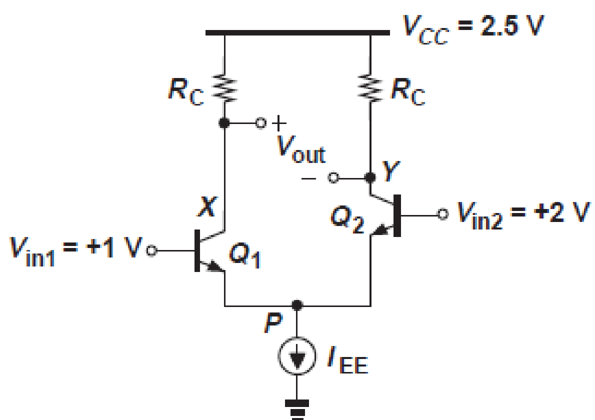


Problem 10.13

Repeat Problem 12, but assuming that $R_{C1} = R_{C2} + \Delta R$. Neglect the Early effect.

Problem 10.15

In the circuit of Fig. 10.9(b), $R_C = 500\ \Omega$. What is the maximum allowable value of I_{EE} if Q_2 must remain in the active region?



Problem 10.19

Suppose the input differential signal applied to a bipolar differential pair must not change the transconductance (and hence the bias current) of each transistor by more than 10%. From Eq. (10.58), determine the maximum allowable input.

$$I_{C2} = \frac{I_{EE}}{1 + \exp \dfrac{V_{in1} - V_{in2}}{V_T}}$$

Problem 10.24

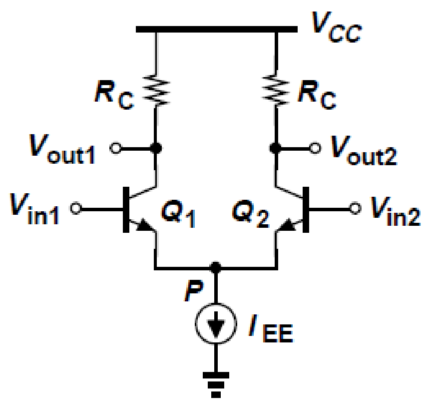
In Example 10.9, $R_C = 500\,\Omega$, $I_{EE} = 1$ mA, and $V_{CC} = 2.5$ V. Assume

$$V_{in1} = V_0 \sin \omega t + V_{CM} \quad (10.214)$$

$$V_{in2} = -V_0 \sin \omega t + V_{CM}, \quad (10.215)$$

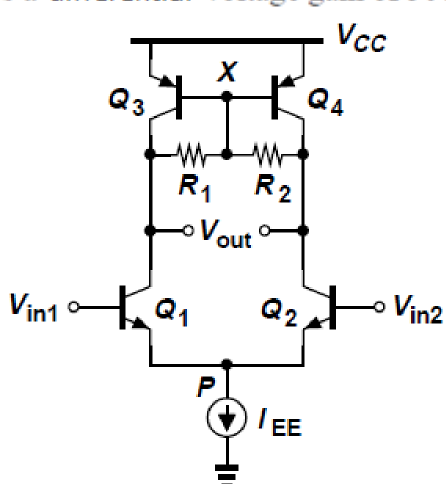
where $V_{CM} = 1$ V denotes the input common-mode level.
(a) If $V_0 = 2$ mV, plot the output waveforms (as a function of time).
(b) If $V_0 = 50$ mV, determine the time t_1 at which one transistor carries 95% of the tail current.

(c) Find the linear input range.



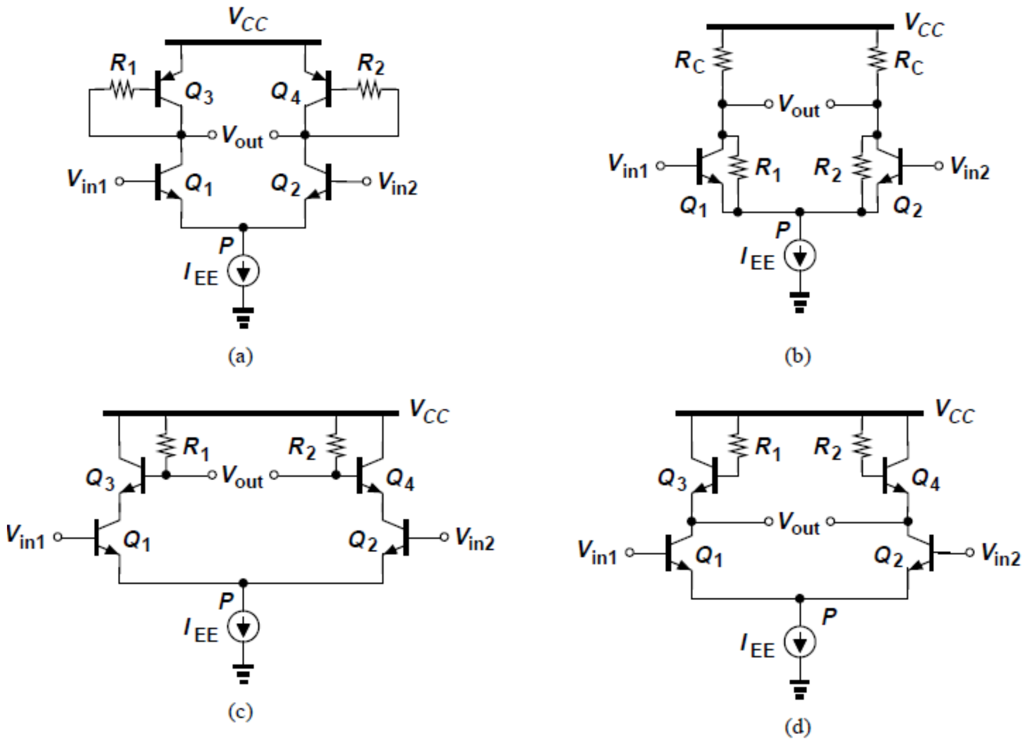
Problem 10.30

Consider the circuit shown in Fig. 10.68, where $I_{EE} = 2$ mA, $V_{A,n} = 5$ V $V_{A,p} = 4$ V. What value of $R_1 = R_2$ allows a differential voltage gain of 50?



Problem 10.32(a)

. Assuming perfect symmetry and $V_A < \infty$, compute the differential voltage gain of each stage depicted in Fig. 10.69.

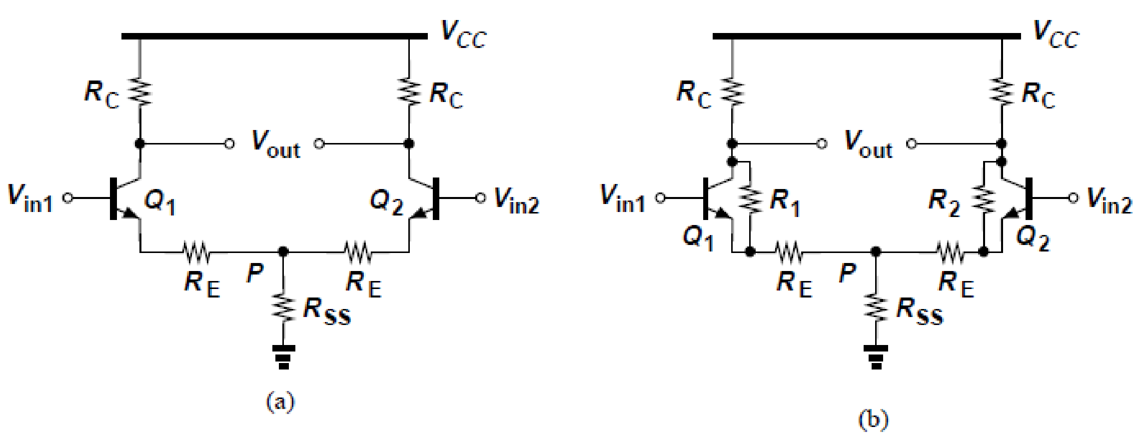


Problem 10.33(a)

Assuming perfect symmetry and $V_A < \infty$, compute the differential voltage gain of each stage depicted in Fig. 10.70. You may need to compute the gain as $A_v = G_m R_{out}$

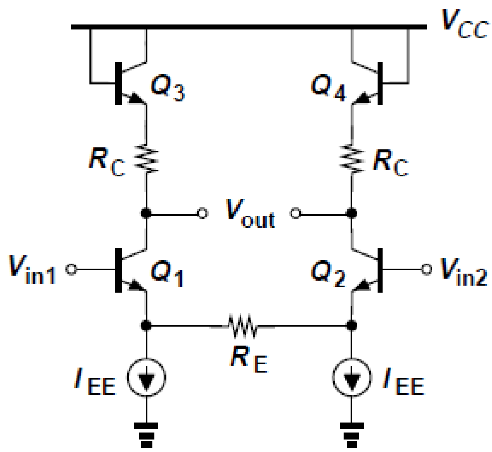
(a) Find A_{dm}, $A_{dm\text{-}cm}$, $A_{cm\text{-}dm}$, A_{cm} and CMRR

(b) Find $R_{in\text{-}dm}$, $R_{in\text{-}cm}$, $R_{out\text{-}dm}$, $R_{out\text{-}cm}$



Problem 10.34

Consider the differential pair illustrated in Fig. 10.71. Assuming perfect symmetry and $V_A = \infty$,
(a) Determine the voltage gain.
(b) Under what condition does the gain become *independent* of the tail currents? This is an example of a very linear circuit because the gain does not vary with the input or output signal levels.

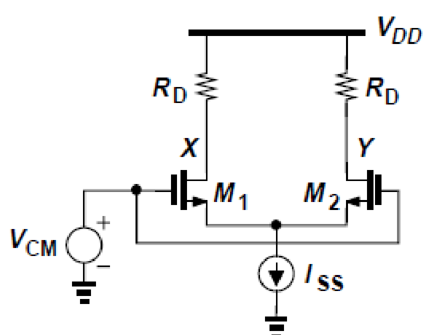


MOS Differential Amplifier:

Problem 10.37

The MOS differential pair of Fig. 10.24 must be designed for an equilibrium overdrive of 200 mV. If $\mu_n C_{ox} = 100\ \mu\text{A}/\text{V}^2$ and $W/L = 20/0.18$, what is the required value of I_{SS}?

Calculate the common-mode input range assuming V_{eff} of I_{SS} is 150mV, V_{TH}=0.5V, V_{DD}=2V, and R_D=5kΩ. Find the linear input range and the output voltage swing.



Problem 10.41

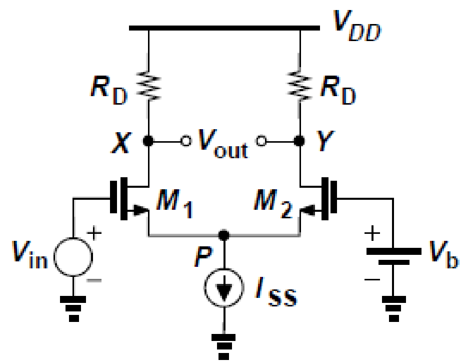
Design an NMOS differential pair for a voltage gain of 5 and a power budget of 2 mW subject to the condition that the stage following the differential pair requires an input CM level of at least 1.6 V. Assume $\mu_n C_{ox} = 100\ \mu\text{A}/\text{V}^2$, $\lambda = 0$, and $V_{DD} = 2$ V. Formulate the trade-off between V_{DD} and W/L for a given output common-mode level.

Problem 10.49

Explain what happens to the characteristics shown in Fig. 10.31 if (a) the gate oxide thickness of the transistor is doubled, (b) the threshold voltage is halved, (c) I_{SS} and W/L are halved.

Problem 10.51

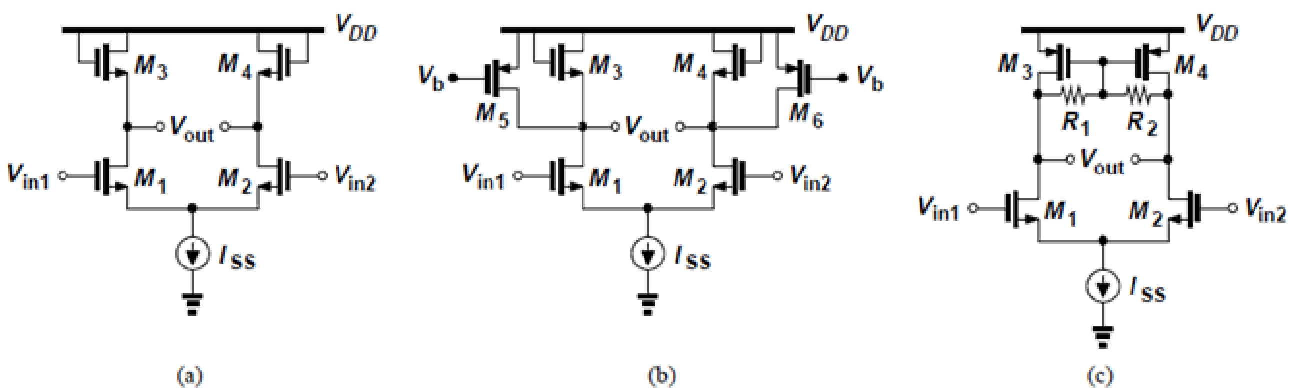
A student who has a single-ended voltage source constructs the circuit shown in Fig. 10.75, hoping to obtain differential outputs. Assume perfect symmetry but $\lambda = 0$ for simplicity.



(a) Viewing M_1 as a common-source stage degenerated by the impedance seen at the source of M_2, calculate v_X in terms of v_{in}.
(b) Viewing M_1 as a source follower and M_2 as a common-gate stage, calculate v_Y in terms of v_{in}.
(c) Add the results obtained in (a) and (b) with proper polarities. If the voltage gain is defined as $(v_X - v_Y)/v_{in}$, how does it compare with the gain of differentially-driven pairs?

Problem 10.52(c)

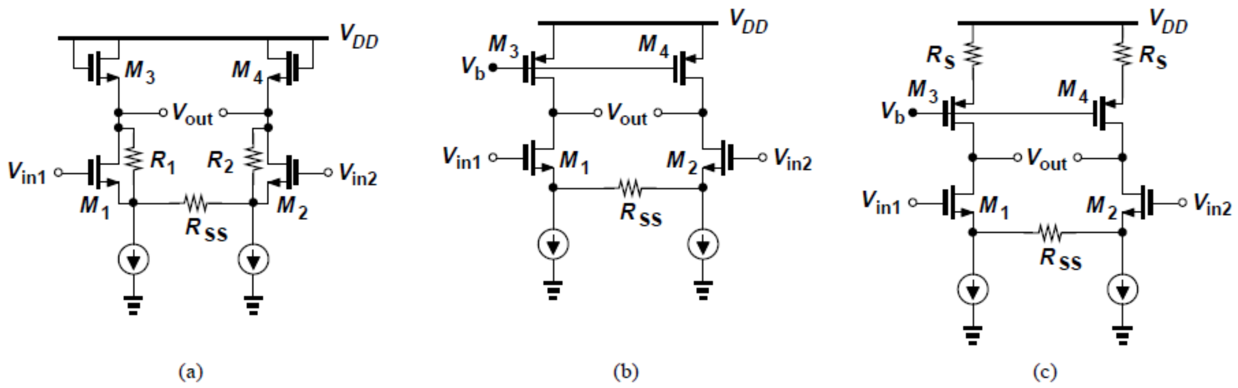
Calculate the differential voltage gain of the circuits depicted in Fig. 10.76. Assume perfect symmetry and $\lambda > 0$.



(a) Find Adm, Adm-cm, Acm-dm, Acm and CMRR
(b) Find Rin-dm, Rin-cm, Rout-dm, Rout-cm

Problem 10.53(b)

Calculate the differential voltage gain of the circuits depicted in Fig. 10.77. Assume perfect symmetry and $\lambda > 0$. You may need to compute the gain as $A_v = G_m R_{out}$ in some cases.



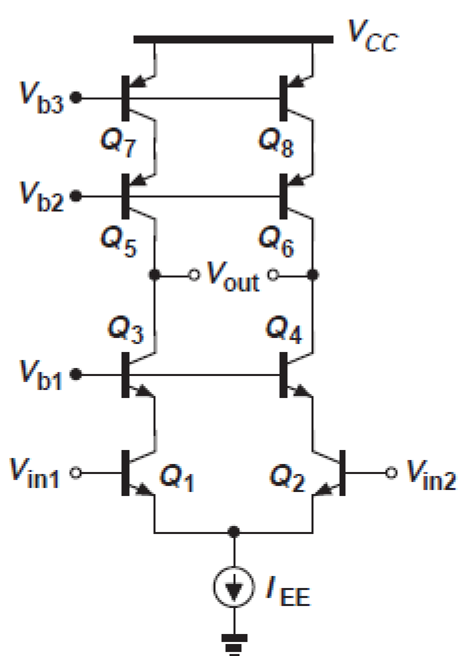
Cascode Differential Amplifies:

Problem 10.60

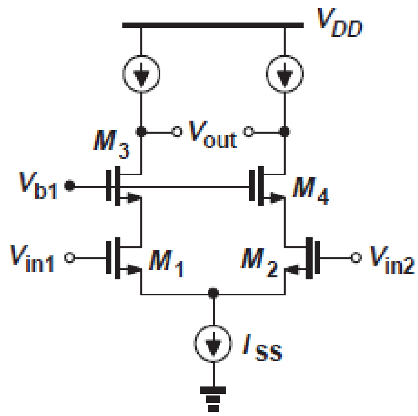
The cascode amplifier shown below is to operate as with a differential gain of 800. If Q_1-Q_4 are identical and so are Q_5-Q_8, determine the minimum allowable Early voltage.
Assume $\beta n = 2\beta p = 100$ and $V_{A,n} = 2V_{A,p}$

Hint:

a) Show that $G_m \cong g_{m1}$
b) Find R_{out} (Use the results of problem 7.4 in the Problem Set #2)



Problem 10.62



The MOS cascode amplifier shown must provide a differential voltage gain of 300.
If W/L = 20µm/180nm for M_1-M_4 and $\mu_n C_{OX}$=100µA/V^2, determine the required tail current.
Assume $\lambda = 0.1V^{-1}$.

Hint:

a) Show that $G_m \cong g_{m1}$

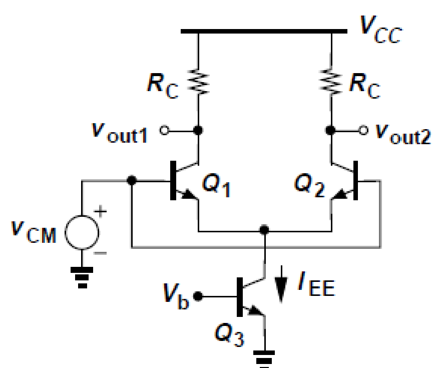
b) Find R_{out}

Common-Mode Rejection:

Problem 10.66

The bipolar differential pair depicted in Fig. 10.85 must exhibit a common-mode gain of less than 0.01. Assuming $V_A = \infty$ for Q_1 and Q_2 but $V_A < \infty$ for Q_3, prove that

$$R_C I_C < 0.02(V_A + V_T). \qquad (10.218)$$

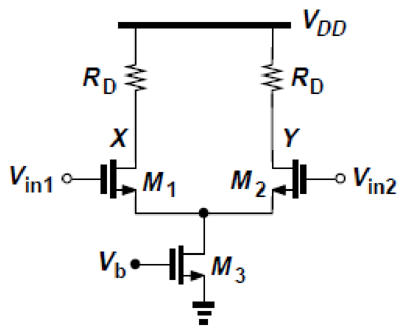


Problem 10.67

Compute the common-mode gain of the MOS differential pair shown in Fig. 10.86. Assume $\lambda = 0$ for M_1 and M_2 but $\lambda \neq 0$ for M_3. Prove

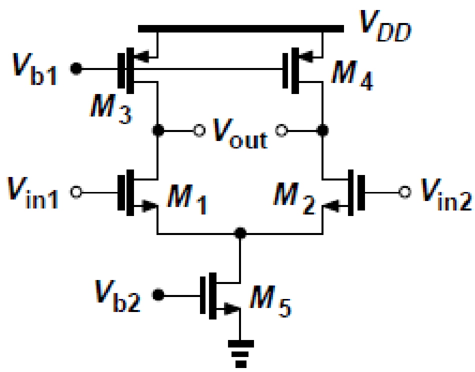
$$A_{CM} = \frac{R_D I_{SS}}{\frac{2}{\lambda} + (V_{GS} - V_{TH})_{eq.}}, \qquad (10.219)$$

where $(V_{GS} - V_{TH})_{eq.}$ denotes the equilibrium overdrive of M_1 and M_2.



Problem 10.68

Calculate the common-mode gain of the circuit depicted in Fig. 10.87. Assume $\lambda > 0$, $g_m r_O \gg 1$, and use the relationship $A_v = -G_m R_{out}$.



Problem 10.70

Compute the common-mode-rejection ratio (**CMRR**) of the differential amplifier shown. For simplicity, neglect channel-length modulation in M1 and M2 but not in M3.