Problem Set 2: MOS Amplifiers (Chapter 7)

Problem 6.46

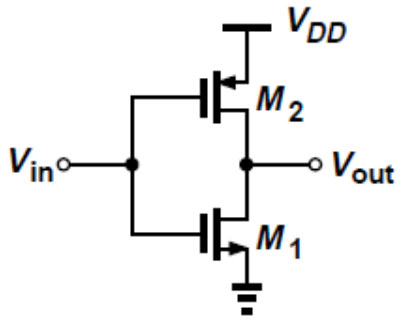
Consider the circuit depicted in Fig. 6.57, where M_1 and M_2 operate in saturation and exhibit channel-length modulation coefficients λ_n and λ_p, respectively.

(a) Construct the small-signal equivalent circuit and explain why M_1 and M_2 appear in "parallel."

(b) Determine the small-signal voltage gain of the circuit.

(c) Determine the output resistance.

(d) Find an expression for the output voltage swing (headroom)?



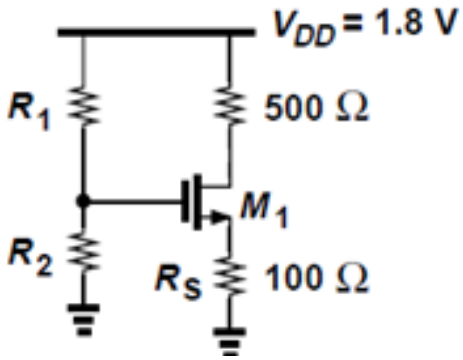
Problem 7.4

The circuit of Fig. 7.42 must be designed for a voltage drop of 200 mV across R_S.

(a) Calculate the minimum allowable value of W/L if M_1 must remain in saturation.

(b) What are the required values of R_1 and R_2 if the input impedance must be at least 30 kΩ.

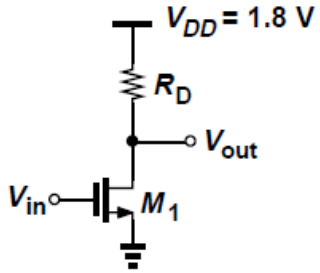
(c) Show that resistance seen from drain of M_1 is given by $R_{seen} = R_S + r_0(1 + g_m R_S)$



Common-Source Topology:

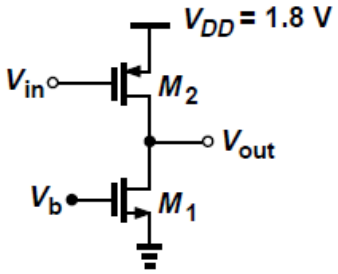
Problem 7.19

We wish to design the stage of Fig. 7.55 for a voltage gain of 5 with $W/L \leq 20/0.18$. Determine the required value of R_D if the power dissipation must not exceed 1 mW.



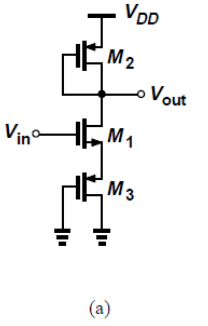
Problem 7.24

The CS stage depicted in Fig. 7.58 must achieve a voltage gain of 15 at a bias current of 0.5 mA. If $\lambda_1 = 0.15\ \text{V}^{-1}$ and $\lambda_2 = 0.05\ \text{V}^{-1}$, determine the required value of $(W/L)_2$.

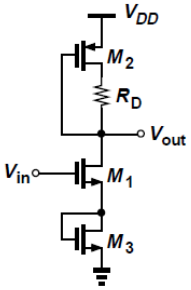


Problem 7.32 (c, e)

Calculate the voltage gain of the circuits depicted in Fig. 7.62. Assume $\lambda = 0$.



(a)



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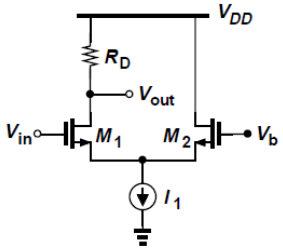
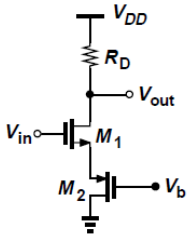
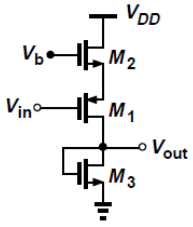


(c)



(d)



(e)

Problem 7.37

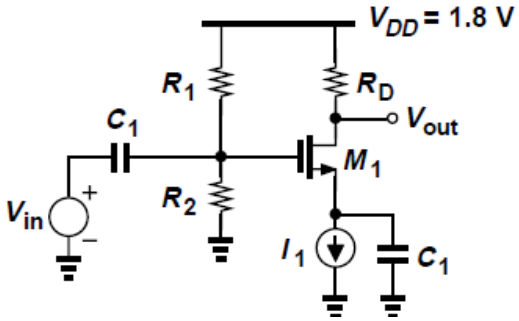
In the common-source stage depicted in Fig. 7.66, the drain current of M_1 is defined by the ideal current source I_1 and remains independent of R_1 and R_2 (why?). Suppose $I_1 = 1$ mA, $R_D = 500\ \Omega$, $\lambda = 0$, and C_1 is very large.

(a) Compute the value of W/L to obtain a voltage gain of 5.

(b) Choose the values of R_1 and R_2 to place the transistor 200 mV away from the triode region while $R_1 + R_2$ draws no more than 0.1 mA from the supply.

(c) Find the value of the linear input range and headroom

(d) With the values found in (b), what happens if W/L is twice that found in (a)? Consider both the bias conditions (e.g., whether M_1 comes closer to the triode region) and the voltage gain.



Common-Gate Topology:

Problem 7.42

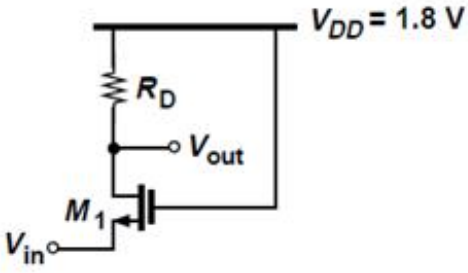
The CG stage depicted in Fig. 7.69 must provide an input impedance of 50 Ω and an output impedance of 500 Ω. Assume $\lambda = 0$.

(a) What is the maximum allowable value of I_D?

(b) With the value obtained in (a), calculate the required value of W/L.

(c) Compute the voltage gain.

(d) Find the value of the linear input range and headroom

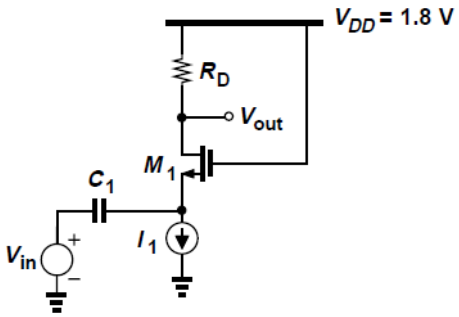


Problem 7.43

The CG amplifier shown in Fig. 7.70 is biased by means of $I_1 = 1$ mA. Assume $\lambda = 0$ and C_1 is very large.

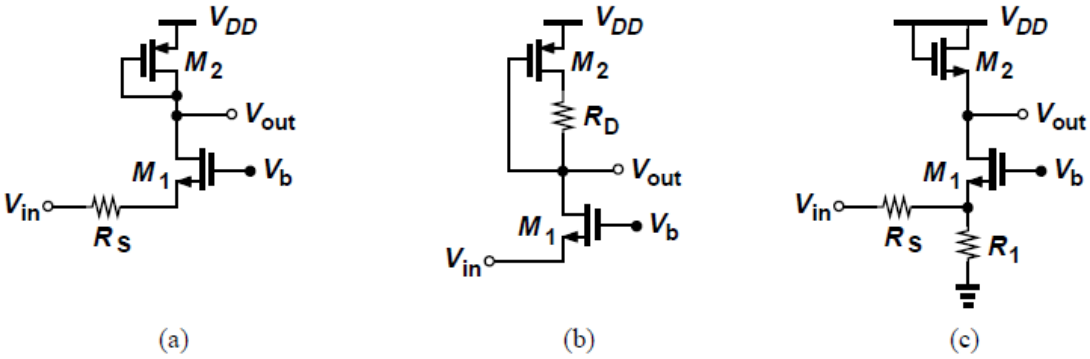
(a) What value of R_D places the transistor M_1 100 mV away from the triode region?

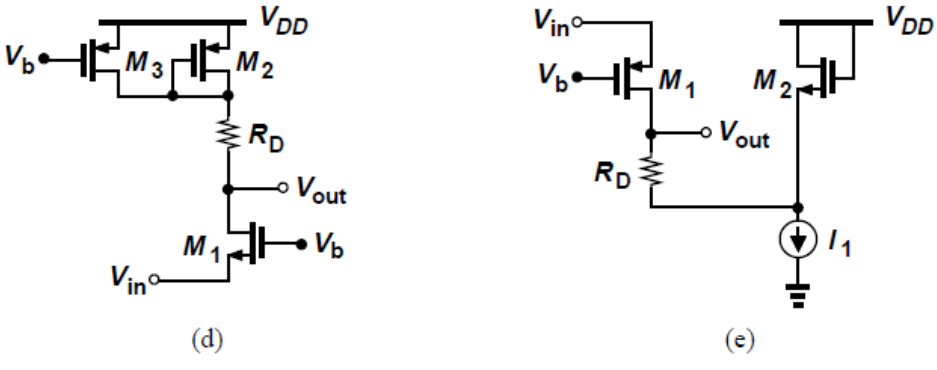
(b) What is the required W/L if the circuit must provide a voltage gain of 5 with the value of R_D obtained in (a)?



Problem 7.44 (c)

Determine the voltage gain of each stage depicted in Fig. 7.71. Assume $\lambda = 0$.



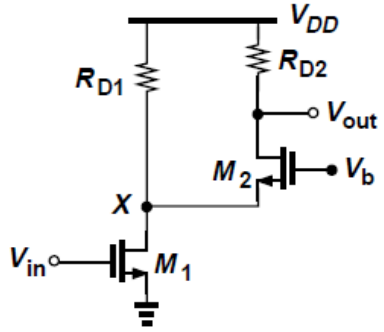


Problem 7.45

Consider the circuit of Fig. 7.72, where a common-source stage (M_1 and R_{D1}) is followed by a common-gate stage (M_2 and R_{D2}).

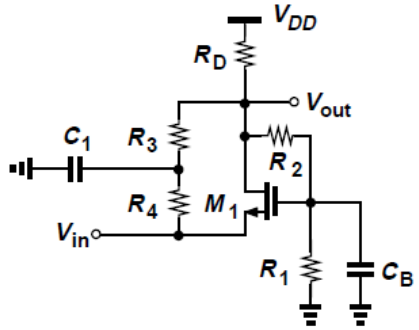
(a) Writing $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$ and assuming $\lambda = 0$, compute the overall voltage gain.

(b) Simplify the result obtained in (a) if $R_{D1} \to \infty$. Explain why this result is to be expected.



Problem 7.48

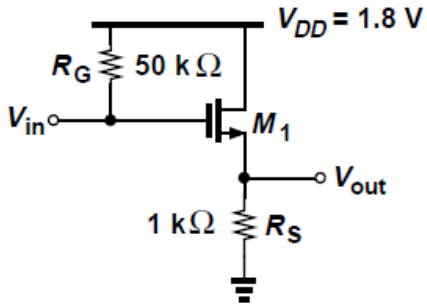
Calculate the voltage gain of the stage depicted in Fig. 7.75. Assume $\lambda = 0$ and the capacitors are very large.



Common-Drain (Source-Follower) Topology:

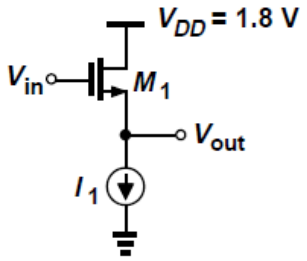
Problem 7.49

The source follower shown in Fig. 7.76 is biased through R_G. Calculate the voltage gain if $W/L = 20/0.18$ and $\lambda = 0.1\ \mathrm{V}^{-1}$. Find the linear input range and headroom.



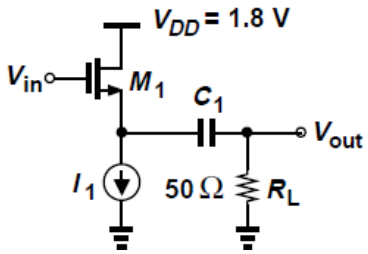
Problem 7.52

The source follower depicted in Fig. 7.78 employs a current source. Determine the values of I_1 and W/L if the circuit must provide an output impedance less than 100 Ω with $V_{GS} = 0.9$ V. Assume $\lambda = 0$.



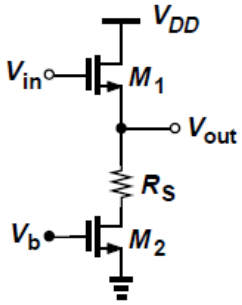
Problem 7.54

We wish to design the source follower of Fig. 7.79 for a voltage gain of 0.8 with a power budget of 3 mW. Compute the required value of W/L. Assume C_1 is very large and $\lambda = 0$.

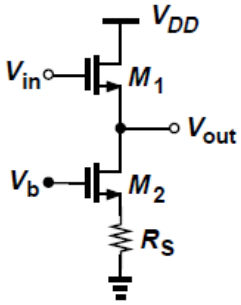


Problem 7.55 (e)

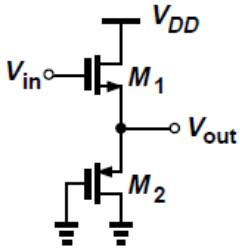
Determine the voltage gain of the stages shown in Fig. 7.80. Assume $\lambda \neq 0$.



(a)



(b)



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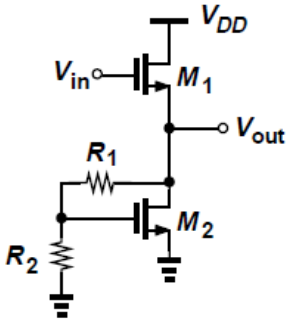

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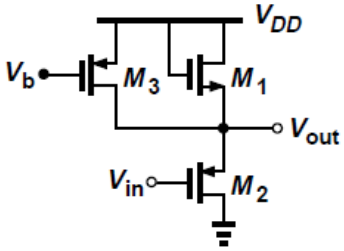
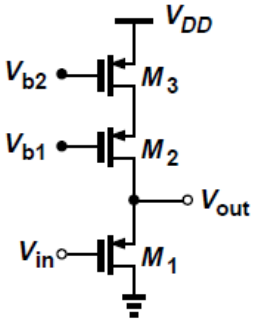


(e)



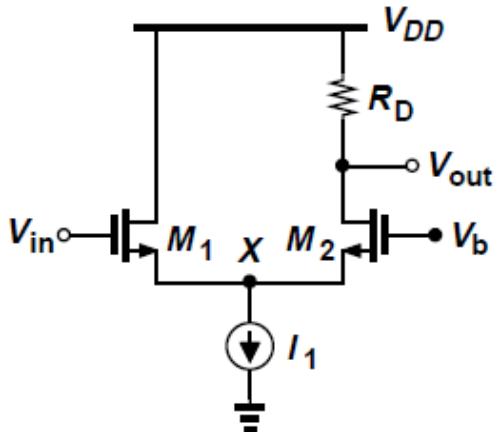
(f)

Problem 7.56

Consider the circuit shown in Fig. 7.81, where a source follower (M_1 and I_1) precedes a common-gate stage (M_2 and R_D).

(a) Writing $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$, compute the overall voltage gain.

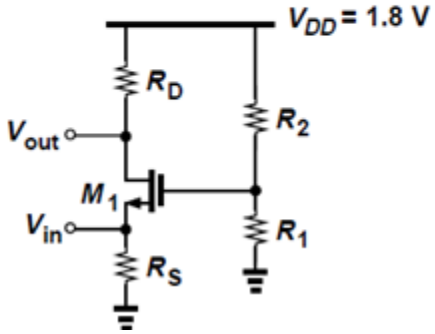
(b) Simplify the result obtained in (a) if $g_{m1} = g_{m2}$.



Design

Problem 7.70

Design the CG stage shown in Fig. 7.92 such that it can accommodate an output swing of 500 mV_{pp}, i.e., V_{out} can fall below its bias value by 250 mV without driving M_1 into the triode region. Assume a voltage gain of 4 and an input impedance of 50 Ω. Select $R_S \approx 10/g_m$ and $R_1 + R_2 = 20\ k\Omega$. (Hint: since M_1 is biased 250 mV away from the triode region, we have $R_S I_D + V_{GS} - V_{TH} + 250\ mV = V_{DD} - I_D R_D$.)



Problem 7.73

In the source follower of Fig. 7.95, M_3 serves as a current source. The circuit must operate with a power budget of 3 mW, a voltage gain of 0.9, and a minimum allowable output of 0.3V (i.e., M_2 must remain in saturation if $V_{DS2} \geq 0.3$ V) Assuming $\lambda = 0.1\ V^{-1}$ for both transistors, design the circuit.