Charge-compensated correlated level shifting for single-stage opamps

M.R. Abdelhamid✉, F.A. Hussien and M.M. Aboudina

High-precision analogue circuits suffer from the finite gain and nonlinearity of operational amplifiers (opamps). Correlated level shifting is one efficient technique that provides gain and swing enhancement for switched-capacitor circuits. Charge-compensated correlated level shifting is proposed, a modification for the correlated level shifting technique, that improves the efficiency of gain enhancement for single-stage opamps.

Introduction: The intrinsic gain of transistors is getting smaller with technology scaling, thus it has become almost impossible to design high gain, high bandwidth operational amplifiers (opamps) for high-resolution, high-speed analogue-to-digital converters (ADCs). Moreover, lower supply voltages result in limitations to achieve high swing implementations. Different techniques have been implemented to account for the analogue non-idealities, such as digital calibration. Different algorithms have been implemented to reverse the effects of finite gain and nonlinearity in opamps [1] or the incomplete settling of the closed-loop system [2]. Other techniques have aimed at replacing the opamp with other circuit elements, such as comparator-based circuits [3] or zero-crossing-detector-based circuits [4]. In addition, several switched-capacitor techniques have been developed to increase the effective gain of opamps, such as correlated level shifting (CLS) [5], correlated double sampling [6] and sequential-CLS [7]. An optimum design for high-resolution, high-speed ADCs would achieve both the gain and bandwidth requirements through incorporating a simple low-power single-stage opamp.

Correlated level shifting: Conventional CLS is implemented as shown in Fig. 1*a*. CLS utilises a level shifting capacitor (C_{LS}) along with two phases to store an estimate of the output voltage in the estimation phase (ϕ_{EST}). Then, in the level shifting phase (ϕ_{LS}), the C_{LS} forces the input of the opamp to approach a virtual ground causing an accurate transfer of charge to the load capacitor.

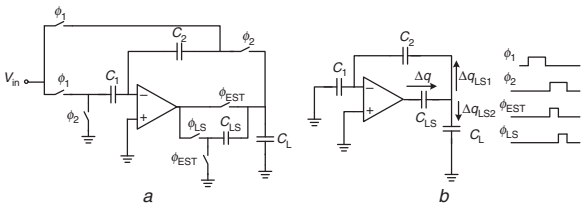

Fig. 1 *Conventional CLS circuit architecture (Fig. 1a) and level shifting phase (Fig. 1b)*

By applying charge conservation during the transitions between each phase and assuming a large level shifting capacitor (C_{LS}), the effective loop gain is found to be, as derived in [5], $G_{eff} \approx G^2$given that G is the amplifier loop gain during the estimation phase

$$G = A\beta = A\frac{C_2}{C_1 + C_2 + C_{IN}} \tag{1}$$

where C_1 and C_2 are the sampling and feedback capacitors, respectively, while C_{IN} is the input capacitance of the opamp.

Finite LS capacitor effect: Owing to using a finite capacitance for level shifting (C_{LS}), it loses some of its charges in the level shifting phase reducing the overall effective loop gain. As shown in Fig. 1*b*, the charge provided by the opamp (Δq), in order to accumulate an accurate charge on C_L, causes the C_{LS} to lose some of its pre-charged voltage. The charge loss is given by $\Delta q = \Delta q_{LS1} + \Delta q_{LS2}$, where Δq_{LS1} and Δq_{LS2} are the level shifting charges needed by the load capacitor and the feedback circuit, respectively. This charge loss directly affects the estimate voltage across the C_{LS} by

$$\Delta V_{CLS} = V_{CLS}\big|_{\phi_{EST}} - V_{CLS}\big|_{\phi_{LS}} = \frac{\Delta q}{C_{LS}} \tag{2}$$

This effect is quantified in [5] by the term λ, and it can be shown that

$$\begin{aligned}\Delta V_{CLS} &= \frac{\Delta q_{LS1} + \Delta q_{LS2}}{C_{LS}} \\ &= \frac{1}{C_{LS}}\left[C_L(\hat{\hat{V}}_o - \hat{V}_o) + C_2(1-\beta)(\hat{\hat{V}}_o - \hat{V}_o)\right] \\ &= \lambda(\hat{\hat{V}}_o - \hat{V}_o)\end{aligned} \tag{3}$$

where $\hat{\hat{V}}_o$ and $\hat{V}_o$ are the output voltages at the level shifting and the estimation phases, respectively, and β is the feedback factor. An ideal level shifting requires this voltage drop to be zero so as to achieve the square of the loop gain. However, it will approach zero only if C_{LS} is infinite or quite a large value. Such capacitance will definitely be area inefficient and power consuming, especially for high-speed settling requirements. Hence, the effective loop gain becomes $G_{eff} \approx \frac{G^2}{1+\lambda}$ where for a single-stage opamp

$$\lambda = \frac{1}{C_{LS}}\left(\frac{(C_1 + C_{IN})C_2}{C_1 + C_2 + C_{IN}} + C_L\right) \tag{4}$$

Therefore, using CLS conventional single-stage opamps can achieve high speed but suffers from less gain enhancement because of the finite C_{LS} effect.

Charge-compensated CLS (CC-CLS): A modified level shifting technique is proposed to efficiently utilise CLS with single-stage opamps to achieve much higher loop gains. This technique tackles the problem of charge loss during ϕ_{LS} presented in Fig. 1*b*. Its idea is based on providing a new path for the accurate charge transfer other than (C_{LS}) to compensate any charge loss. The proposed circuit is shown in Fig. 2*a* where a new path is created using the capacitor (C_{ch}) in order to provide the required charge to C_L in the level shifting phase without decreasing the estimated charge on C_{LS}.

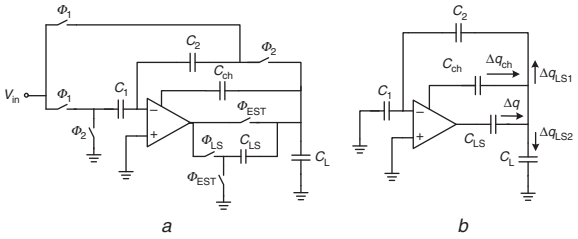

Fig. 2 *The CC-CLS circuit architecture (Fig. 2a) and level shifting phase (Fig. 2b)*

As shown in Fig. 2*b*, the charge lost by C_{LS} is given by $\Delta q = \Delta q_{LS1} + \Delta q_{LS2} - \Delta q_{ch}$, where the charge ($\Delta q_{ch}$) provided by the charging capacitor (C_{ch}) can be designed to be sufficient for the level shifting charges needed by both the load capacitor and the feedback circuit, Δq_{LS1} and Δq_{LS2}, respectively. Therefore, the charge lost by C_{LS} approaches zero leaving the estimate voltage across it without change. The finite C_{LS} effect is quantified by

$$\begin{aligned}\Delta V_{CLS} &= \frac{1}{C_{LS}}(\Delta q_{LS1} + \Delta q_{LS2} - \Delta q_{ch}) \\ &= \frac{1}{C_{LS}}\left(\frac{(C_1 + C_{IN})C_2}{C_1 + C_2 + C_{IN}} + C_L\right. \\ &\left. -C_{ch}\left(\frac{A_x C_2}{C_1 + C_2 + C_{IN}} - 1\right)\right)(\hat{\hat{V}}_o - \hat{V}_o) \\ &= \lambda(\hat{\hat{V}}_o - \hat{V}_o)\end{aligned} \tag{5}$$

Therefore

$$\lambda = \frac{1}{C_{LS}}\left((C_1 + C_{IN})\beta + C_L - C_{ch}(A_x\beta - 1)\right) \tag{6}$$

where C_{ch} is the charging capacitor and A_x is the gain from the input of the opamp to the charging capacitor path. Both C_{ch} and A_x can be designed to achieve a value of λ close to zero and thus an effective loop gain close to the square of the amplifier loop gain. In addition,

the term λ can be designed to be a negative value in order to provide even higher gain enhancement without causing the feedback loop to be unstable. In fact, the condition to achieve the square of the loop gain ($\lambda = 0$) becomes

$$(A_x\beta - 1)C_{ch} = C_L + (C_1 + C_{IN})\beta \quad (7)$$

This condition can be satisfied regardless of the value of C_{LS}. Hence, a high loop gain can be achieved with small values of C_{LS} in order to obtain higher frequencies with less power consumption.

The multipath node can be as simple as the folding node in a folded cascode architecture. A folded cascode opamp with charging capacitors in the estimation phase is shown in Fig. 3. Here, $A_x \approx g_m r_o$ as the resistance seen by the drain of the cascode device is much higher than its own resistance. The charging capacitors must be placed in the correct path in order to provide the necessary charge in the level shifting phase instead of acquiring more charges which will cause the effective loop gain to deteriorate even more. For the CC-CLS technique to work correctly, the charging capacitors must be inserted across a negative gain from the multipath node to the output of the opamp. As shown in Fig. 3, the negative gain is achieved by utilising the symmetry between the two halves of the fully differential opamp.

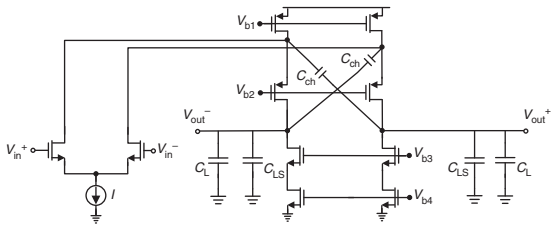

Fig. 3 *Schematic of folded-cascode opamp with charging capacitance (C_{ch}) during estimation phase*

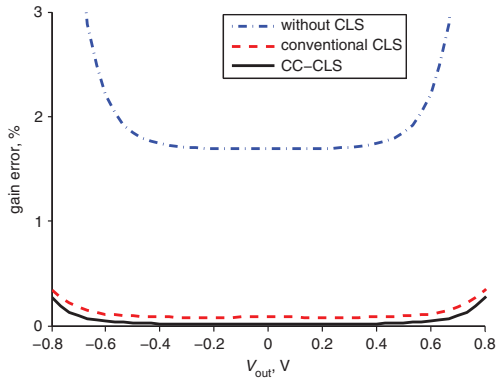

Fig. 4 *Gain error percentage against output voltage using 42.4 dB opamp without CLS, with CLS and with CC-CLS*

Simulation results: A flip-around switched-capacitor amplifier with a closed-loop gain of 2 is implemented in CMOS 130 nm with a folded-cascode opamp using three different configurations: simple opamp without level shifting, with CLS, and with CC-CLS. A comparison between the settling accuracy of the three configurations is made for the same power consumption and the same total added capacitance in CLS and CC-CLS. The opamp is designed with a DC open-loop gain of 42.4 dB, achieving a loop gain of about 35.4 dB. The conventional CLS uses a level shifting capacitance of 800 fF while the CC-CLS utilises the same 800 fF divided as 300 fF for C_{LS} along with a 500 fF for C_{ch}.

The simple opamp settles to 1.69% error which corresponds to a loop gain of 35.4 dB, as shown in Fig. 4. The conventional CLS settles within an error of 0.082% achieving a 61.7 dB loop gain accuracy. With the addition of the new path in the CC-CLS technique, the effective loop gain experiences an improvement of up to 74.4 dB yielding a settling error as low as 0.019% and achieving an overall 12.76-bit settling accuracy. Therefore, using the CC-CLS technique improves system accuracy from lower than 7-bit with a simple opamp and 10.8-bit with conventional CLS up to 12.76-bit without adding extra phases as in [7], and hence is more suitable for high speed applications with high settling accuracy.

A prototype pipeline ADC has been implemented with a first stage as shown in Fig. 2, using a single-stage opamp shown in Fig. 3 while having an ideal backend ADC. Table 1 compares the performance of the three opamp designs (single-stage opamp, single-stage opamp with CLS and single-stage opamp with CC-CLS) as well as the ADC performance utilising each of the three techniques as a first stage.

Table 1: Performance summary of first stage in ADC prototype

Specification	Simple	CLS	CC-CLS
Technology and supply voltage	CMOS 130 nm, 1.2 V		
Input voltage (V_{pp})	1.2	1.2	1.2
Sampling rate (MHz)	10	10	10
Sampling and feedback capacitors (pF)	1	1	1
Load capacitor (pF)	1	1	1
Opamp DC gain (dB)	42.4	42.4	42.4
Gain-bandwidth product (MHz)	356	245	210
Added capacitance (fF)	0	$C_{LS} = 800$	$C_{LS} = 300$ $C_{ch} = 500$
Output steady-state error (%)	1.69	0.082	0.019
Effective loop gain (G_{eff}) (dB)	35.4	61.7	74.4
ADC SNDR (dB)	42.9	66.9	78.65
ADC ENOB (bits)	6.83	10.82	12.76
Power consumption (mW)	1.19	1.19	1.19

Conclusion: This Letter presents the CC-CLS technique as a switched-capacitor technique suitable for low-power and high-accuracy and high-speed circuits. This technique modifies the conventional CLS technique which provides accuracy and swing improvements to be more suitable for single-stage opamps. The proposed CC-CLS technique provides multipath for level shifting so as to eliminate the effect of finite level shifting capacitance and to further enhance the opamp gain and swing.

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One or more of the Figures in this Letter are available in colour online.

M.R. Abdelhamid, F.A. Hussien and M.M. Aboudina (*Department of Electronics and Electrical Communications Engineering, Cairo University, Egypt*)

✉ E-mail: m_radwan8@cu.edu.eg

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