MOHAMED A. Y. ABDALLA, B.E., M.Sc., Ph.D.

402-169 ST. George st., Toronto, ON, M5R 2M4, Canada

Phone: 647-836-8222 email: mohamed.abdulla@utoronto.ca

PROFILE

Solid background in Analog and RF/high-speed circuit design, with strong emphasis in high-speed analog design for serial applications. Strong theoretical background and good experience in system and circuit level design.

EDUCATION

2002 - 2008 **Ph.D.** Dept. of Elec. & Comp. Eng., University of Toronto, Canada.
- Thesis: "Metamaterial-inspired CMOS tunable RF and microwave circuits for steerable antenna arrays"
- Supervisors: Prof. Khoman Phang & Prof. George V. Eleftheriades

2000 - 2002 **M.Sc.** Elec. & Comm. Dept., Cairo University, Egypt. GPA: 3.7/4, with honours.
- Thesis: "Novel Analog CMOS current-mode building blocks for filtering and VGA applications"
- Supervisor: Prof. Ahmed M. Soliman

1995 - 2000 **B.E.** Elec. & Comm. Dept., Cairo Univ., Egypt. GPA: 3.7/4, with honours, ranked 2nd of the 2000 class.
- Project: "CMOS mixed signal fingerprint sensing and parallel processing architecture"
- Supervisor: Prof. Ahmed M. Soliman

PROFESSIONAL EXPERIENCE

2011 - present **Senior Analog IC Designer at Snowbush IP, A Division of Gennum Corp., ON, Canada.**

- Designed a 1-14Gbps 0.85V 5-tap edge and data DFE in 28nm with eye monitoring functionality and offset cancellation capability for half rate CDRs
- Experience in 25Gbps DFE techniques for quarter rate CDRs
- Authored/ Co-authored several patents on adaptive equalizations techniques for serial link equalizers including: TX feed-forward equalizers (FFE), RX continuous time linear equalizers (CLTE), and decision feedback linear equalizers (DFE), RX Feed-forward equalizer, and RX reflection canceller.
- Lead a team of 4 physical designers and mentored junior IC designers
- Helped in providing analog effort estimates for scheduling purposes

2008 - 2011 **Analog IC Designer at Snowbush IP, A Division of Gennum Corp., ON, Canada.**

- Experienced in the design of 1-10Gbps multi-standard SERDES IP blocks including VGA, CTLE, DFE, transmit driver, CDR, PLL, VCO, and ESD/clamp structures in deep submicron CMOS processes
- Designed a 500Mbps 1V bi-directional LVDS driver/receiver in 65nm CMOS
- Verification of various IP blocks in different technologies such as: VCO, Tx driver, Tx clock path, ESD for high-speed I/O
- Developed novel adaptation algorithms for serial link equalizers including: TX feed-forward equalizers (FFE), RX CLTE, and decision feedback linear equalizers (DFE), RX Feed-forward equalizer, and RX reflection canceller
- System level verification of serial links & modelling of various SERDES IP blocks in Matlab/Simulink such as VGA, FFE, DFE, bang-bang CDR, VCO phase noise, and Tx
- Presented to customers on several occasions results of various system level investigations

- Co-authored an ISSCC paper describing the SERDES IP
- Created IBIS Models for a 40nm & 65nm CMOS SERDES including differential TX driver models with/without pre-emphasis

2002 - 2008 **Research & Teaching Assistant at the Dept. of Elec. & Comp. Eng., University of Toronto, ON, Canada.**

- Designed, fabricated & tested 1-5.4GHz tunable active inductors in *0.13μm CMOS*, with independent inductance & quality factor control.
- Designed, fabricated & tested 2.1-3.1GHz 0.13*μm CMOS* directional coupler, with tunable operating freq. & coupling coefficient.
- Designed, fabricated & tested 2.6GHz & 4GHz fully-integrated wide tuning range phase shifters, with constant input & output impedance, in *0.13μm CMOS*.
- Designed a 10GHz fully differential tuned cascode LNA in 0.5*μm SiGe BiCMOS* process.
- Designed a 0.13*μm CMOS* 10GHz limiting amplifier with output amplitude control.
- Designed, fabricated & tested 2.5GHz PCB wide tuning range phase shifters with very low return loss, and used them to build a series-fed electronically steerable patch array for ISM band applications.
- High-frequency modelling of spiral inductors using Asitic & Agilent Design System ADS/Momentum.

2000 – 2002 **Research & Teaching Assistant at the Dept. of Elec. & Comm., Faculty of Eng., Cairo University, Giza, Egypt.**

- Rail-to-rail low-distortion 0.5*μm CMOS* differential transconductors using the dynamic biasing technique.
- Highly-linear transconductors designed in 0.5*μm CMOS*; Based on the input common-mode tracking technique, the input level shifting technique, and the cross-coupling technique.
- Differential squaring circuits designed in 0.5*μm CMOS*.
- Differential current operation amplifier (COA) designed in 0.5*μm CMOS*.
- Differential current-mode digitally controlled variable gain amplifier (VGA) designed in 0.5*μm CMOS*.
- Differential G_m-C & current-mode filters, band-pass & low-pass, designed in 0.5*μm CMOS*.

2000 - 2001 **Part-time design engineer**

- Worked with an industry related research group at the Dept. of Elec. & Comm., Cairo Univ. on designing an MPEG decoder for TV satellite receivers.

ADMINISTRATIVE EXPERIENCE

- Helped organizing the IEEE International Solid-State Circuits Conference (ISSCC) in 2005 & 2008.
- Co-organized the distinguished lecture series for the IEEE Solid-State Toronto Section.

LIST OF JOURNAL PUBLICATIONS

- M. A. Youssef and A. M. Soliman "A Modified CMOS Balanced Output Transconductor with Extended Linearity," *Analog integr. circ. & signal processing*, Sept. 2003.
- M. A. Youssef and A. M. Soliman "A New CMOS Rail to Rail Low Distortion Balanced Output Transconductor," *Analog integr. circ. & signal processing*, July 2004.
- M. A. Youssef and A. M. Soliman "A Novel CMOS Realization of the Differential Input Balanced Output Current Operational Amplifier and its Applications," *Analog integr. circ. & signal processing*, July 2005.

- M. Abdalla, K. Phang, and G. V. Eleftheriades, "A 0.13µm CMOS phase shifter using tunable positive/negative refractive index transmission line," *IEEE Microw. Wireless Components Lett.*, Vol. 16, no. 12, pp. 705-707, Dec. 2006.
- M. Abdalla, K. Phang, and G. V. Eleftheriades, "Printed and integrated CMOS positive/negative refractive-index phase shifters using tunable active inductors," *IEEE Trans. Microw. Theory and Tech.,* Vol. 55, no. 8, pp. 1611-1623, August 2007.
- M. Abdalla, K. Phang, and G. V. Eleftheriades, "A compact highly- reconfigurable CMOS MMIC directional coupler," *IEEE Trans. Microw. Theory and Tech.,* Vol. 56, no. 2, pp. 305-3019, Feb. 2008.
- M. Abdalla, K. Phang, and G. V. Eleftheriades, "A Planar Electronically Steerable Patch Array Using Tunable PRI/NRI Phase Shifters," *IEEE Trans. Microw. Theory and Tech.,* Vol. 57, no. 3, pp. 531 - 541, March 2009.

LIST OF CONFERENCE PUBLICATIONS

- F. El Seddeek, M.H. Ismail, M.M. Aboudina, M.A. Youssef, A.M. Soliman "CMOS mixed signal fingerprint sensing and parallel processing architecture," *Electrotechnical Conference, 2002. MELECON 2002. 11th Mediterranean*, 7-9 May 2002.
- M. Youssef, E. Chong, K. Phang, "Distortion analysis using signal flow graphs and Volterra series," Proc. 46th IEEE Inter. Midwest Symp. on Circuits & Systems MWSCAS 2003, Cairo, Egypt, Vol. 1, pp. 84-89, Dec. 2003.
- M. Abdalla, and K. Phang , "A 0.13µm CMOS active inductor based on a modified gyrator-C architecture," *Micronet Annual Workshop,* Ottawa, Canada, May 2005.
- M. Abdalla, G. V. Eleftheriades, and K. Phang, "A differential 0.13µm CMOS active inductor for high frequency phase shifters," *Proc. IEEE Circuits and Systems ISCAS 06,* Kos, Greece, pp. 3341-3344, May 2006.
- M. A. Y. Abdalla, K. Phang, and G. V. Eleftheriades, "a tunable metamaterial phase-shifter structure based on a 0.13µm CMOS active inductor," *Proc. 36th European Microwave Conf.,* Manchester, Great Britain, pp. 325-328, Sept. 2006.
- M. A. Y. Abdalla, K. Phang, and G. V. Eleftheriades, "A bi-directional electronically tunable CMOS phase shifter using the high-pass topology," *2007 IEEE MTT-S Int. Microwave Symp. Dig.,* Honolulu, Hawaii, pp. 2173-2176, June 2007.
- M. A. Y. Abdalla, K. Phang, and G. V. Eleftheriades, "A steerable series-fed phased array architecture using tunable PRI/NRI phase shifters," Invited paper, *Int. Workshop on Antenna Tech. iWAT 08,* Chiba, Japan, March 2008.
- M. A. Y. Abdalla, K. Phang, and G. V. Eleftheriades, "A metamaterial-based passive MMIC tunable phase shifter," *in Proc. IEEE AP-S Int. Symp.*, Toronto, Canada, July 2010.
- M. Ramezani, M. Abdalla, A. Shoval, M. Van Ierssel, A. Rezayee, A. McLaren, C. Holdenried, J. Pham, E. So, D. Cassan, S. Sadr "An 8.4mW/Gbps 4-Lane 48Gbps Multi-Standard Compliant Transceiver in 40nm digital CMOS Technology," *Submitted to the 2011 International Solid-State Circuits Conference*.

SELECTED SKILLS & QUALIFICATIONS

- Excellent analytical and design skills for CMOS Analog & RF circuits
- Experienced in layout using CADENCE Virtuoso & Tanner L-Edit as well as verification using Assura, Calibre & Diva.
- Solid performance under work pressure
- The ability to meet deadlines, taped-out three RF *0.13µm* CMOS chips during Ph.D.
- Experienced in high-speed testing as well as high-speed die probing.
- Strong communication & presentation skills, acquired through the numerous courses I taught as well as presenting my research work at different conferences and through many customer presentations
- Expert in, SpectreRF, Analog Artist & Smartspice
- Proficient in MATLAB/SIMULINK, LABVIEW
- Comfortable with Vhdl & C/C++

AWARDS & FELLOWSHIPS

- Gennum Innovation Award for 2009 for contributions to the 10Gbps KR Platform
- Rogers Ph.D. Fellowship 2004
- Univ. of Toronto Ph.D. Fellowship 2002, 2003, & 2005
- Univ. of Toronto, Dept. of Elec. & Comp. Eng. “Best teaching assistant award” for 2002-2003
- Cairo University, Dept. of Elec. & Comm. Eng. graduation project award 2000
- Second position in Egypt IEEE student contest 2000
- Mobinil award for the distinguished students 2000
- Mentor Graphics award for graduation projects 2000
- Cairo University, Dept. of Elec. and Comm. Eng. award for distinguished students 2000
- Distinguished student faculty of Eng. award 1995-2000