Design of All Optical Digital Circuits

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Abstract

Designing digital circuits has a high priority in research field in the present time. It shall also still the main concern of many researchers in the future. Many studies in this field are in progress some are published and other still confidential. This paper proposes a design for elementary digital circuits; NOT, OR, and AND. Using light as direct input. These circuits process these optical inputs to produce optical outputs without changing the light rays to any other type of energy or waves. The proposed design depends on mirrors, lenses and properties of light to introduce new digital circuits design using infrared rays as inputs.

Key words:
Optical Digital Circuits, light, Constructive Interference, Destructive Interference, NOT, AND, OR, Ray beams.

Abbreviations:
c: Speed of light in vacuum, *v*: speed of light in a materials, *n*: refraction index ,

1. Introduction:

There are many different methods and alternatives to design any digital circuit or system. Every method has its advantages and suffers from its weakness. The way to evaluate any design depends on operational time, distortion of the output signal, noise, wrong operations, faults, power consuming, other types of energy that the circuit produces while operation, availability of emerging with an other circuits or systems, its life time and availability of maintenance [1].

Optical design depends almost on properties of light which include reflection, refraction, dispersion and absorption, and on materials properties like index of refraction, transparency and density [2]. Optical reflection and refraction have some simple rules for phase shifts due to material [3]:

- Reflection or refraction at a surface behind which is a medium with lower n (where n is the refraction index of the medium) causes no phase shift.
- Reflection at a surface behind which is a medium with higher n causes a phase shift of half a wavelength.
- The speed of light is slower in medium with n > 1, this causes a phase shift proportional to n * length traveled.

Given the above rules; mirrors, including half-silvered ones, have the following properties:

- A half wavelength phase shift occurs upon reflection from the front of a mirror, since the medium behind the mirror (glass) has a higher refractive index than the medium the light is traveling in air.

Let k be the constant phase shift incurred by passing through a standard glass plate on which a mirror resides; a total of 2k phase shift occurs when reflecting off the rear of a mirror, since light traveling toward the rear of a mirror will enter the glass plate, incurring k phase shift, and then reflect off the mirror with no additional phase shift since only air is now behind the mirror, and travel again back through the glass plate incurring an additional k phase shift [3].

This paper is organized as follow:
Section 2: shows previous studies.

Section 3, represents the proposed NOT circuit, its operation verification and delay time analysis.
Section 4: demonstrates The AND circuit Design, operation verification, delay time analysis, design enhancement, multi- input and multi-stages Design and multi-input single chip design.
Section 5: represents the OR circuit Design, operation verification, design enhancement, multi- inputs and multi-stage design and multi-inputs single chip design.
Section 6: represents conclusion and future work.

2. Previous Studies

Many researches are in progress in the field of optical circuits, especially in digital circuit design. NASA has started a project for inventing high-speed optical digital circuits. Its researcher publish an AND circuit operates by using laser beams in [8], figure 1, shows this circuit. NEC, Pentagon and many other organizations are working confidentially on similar projects.

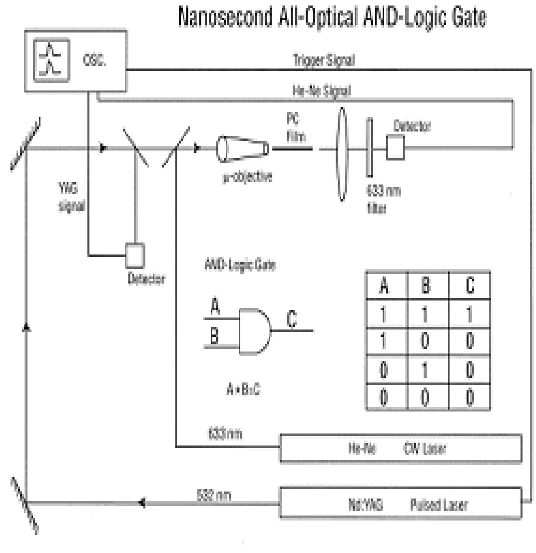

Figure 1- Structure of optical AND circuit NASA project

3. The Proposed NOT Circuit

The proposed NOT circuit design depends on many facts:

1. According to reflection law of light from a flat mirror, the reflected angle of a ray is equal to the incident angle.
2. A beam can be a destructive beam if its frequency is shifted by π (180°) which equals half of the wavelength of the interfering beam [3,4].
3. Mirrors and lenses properties.

According to the NOT circuit function, an input of logical 1 produces an output logical 0. Meaning that although no light is entered in the input, light must be produced at the output. This raises an important problem: how to produce a light ray from nothing. This is solved by using the enable input as a pulse signal equal to logic 1, to be the output if the input equal logic 0. The energy of any light wave (E)

$$E = h * f \qquad (1)$$

Where h is blank's constant and f is the frequency of the wave.
Since the frequency,

$$f = c/\lambda \qquad (2)$$

Where c is the velocity of light in vacuum (where $c = 2.998 * 10^8$ m/s) and λ is wavelength of light wave. So frequency increases proportionally to decrease in wavelength:

$$f \propto 1/\lambda. \qquad (3)$$

From the relations (1),(2) and (3); The light waves with short wavelengths has more energy than the long ones. We find that ultraviolet rays have more energy than visible light and visible light have energy greater than infrared [5].

Our proposed design is using infrared as inputs and outputs. It is depends on using the same frequency and the same wavelength for the different inputs. The input beams have the same phase and the impulse modulation for logic 1 and 0. Silicon (Si) is a transparent material for infrared and its compounds like silicon dioxide (silica) also are transparent materials, so glass is a transparent material for infrared so we use a glass lenses and a high polished mirror which reflects almost of beam falling on it. The mirror is arranged where the reflecting metal in the front and the glass in behind to take the advantage of shifting phase by $\lambda/2$. The angle of incident beam on the mirror $\theta = 45°$. A thin lens is used to minimize the operation time of the circuit. Paths length must have equal distance to prevent random errors and undesired shifting so the path b_2b_2' equals the bath of b_1 figure 2; illustrates the architecture of the circuit.

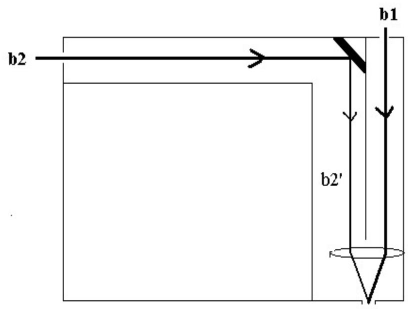

Figure 21, Structure of the proposed optical NOT circuit

As shown in figure 1, we have two beams b_1 and b_2. The beam b_1 enables the circuit; it always has the value of logic 1. While the beam b_2 holds the input value, which alternate between logic 0 and logic 1. The two beams b_1 and b_2 have the same phase, the same wavelength and the same frequency.

When the beam b_2 is dropped on the mirror m, which is a high polished flat mirror, the beam b_2 is reflected from m as the beam b_2'. The beam b_2' has the opposite angle and phase shifted by half of the wavelength of b_2. The lens L is used to gather the parallel beams b_1 and b_2' at its focal where they interfere together (destructive interference) where beam b_2' has experienced a half wavelength phase shift and beam b_1 has no phase shift. thus yielding a phase difference of exactly half a wavelength, implying that the crest and troughs of the two waves cancel each other and that produces logic 0 when beam b_2 equal to logic 1. When beam b_2 equal to logic 0 there is no illumination at the input port so beam b_1 will pass the lens L and no interference will occurs at the lens L focus so the output value will equal to logic 1.

3. 1. NOT Operation Verification:

The NOT circuit has two inputs:

- One enabled b_1, always equal to logic 1 in order to produce logical one as output when b_2 equal to logical 0.
- One data input b_2, which has two cases:

1. b_2= logical 0: In this case, there is no illumination and subsequently the interfering between the beams b2' and b1 will not happen, so b_1 will pass through the lens L with a value of logic 1 at the focus of the lens L.
2. b_2= logical 1:

- According to the falling of the input beam b2 on the mirror, the phase of the beam b_2` will be shifted by π (180°) which equal have the wavelength of b2.
- When b_2 fills on the mirror m_1, the mirror will reflects b_2 as b_2' towards the lens.
- The lens L gathers b_1 and b_2' at its focus, where they interfere together in a destructive interference, in this case the distance between interference fringes can be recognized. So we can find more than one minimum point of the interference field (dark parts) at which we can get value of logic 0.

3. 2. Circuit Delay Analysis:

In the study of the circuit delay we will use analytical study for different types of glass and different range of infrared light beams from near IR (λ = 800 nm) to far IR (λ = 2500 nm). To work at 500 femto second operation delay time, the longest path of any beam must not exceed $3 * 10^8 * 500/ 10^{15} = 150$ µm.

Table 1. NOT circuit behavior

b_2	b_1	b_2'	Interference between b_1, b_2'	Output
0	1	The amplitude of $b_2 = 0$ then the amplitude of $b_2' = 0$ Value = 0	There is no signal from b_2' So there no interference	1
1	1	Value = 1, phase shifted by π(180°) which equal half of the wavelength	Destructive interference	0

3. 2. 1. Lens Delay analysis:

In determining the delay parts in the circuit, we find that only lens is the bottleneck of operation where it is the only material the light pass through has refractive index n>1 by using good quality glass which has low aberration effect: we find many different glass type in materials handbooks[4,5,6,7,8].

We can calculate the glass index of refraction (n) by cutting the three left most digits from the glass number then, dividing them by 1000 and add 1 to the result [5].

$n = \text{float}(\text{integer}(N/1000))/1000 + 1$ (4).

$c = 2.998 * 10^8$ m/s $\approx 3 * 10^8$ m/s. (5)

$v = c / n$. (6)

Where

c is the speed of light in vacuum.
v is the speed of light inside a material.
n is the refractive index of the material.

From (5) and (6) we can calculate the speed of light inside the different types of glass. The delay time (t) in a glass type depends on the thickness and the speed of light inside a particular type of glass.

$t = k / v$ (7)

Where k = lens thickness, v =the speed of light in glass type;

Table 2 illustrates glass types and their numbers, density, refraction index and speed of light inside them, figure 3 represents the relation between refraction index and speed of light inside glass. For example; if lens thickness equal 1 mm then delay time for example in Crown K5 glass will equal $0.001 / (1.899 * 10^8) = 0.526 * 10^{-12}$ s = 0.526 ps. Delay time for different thickness is illustrated in figure 4.

Table 2. Four Glass major types and their properties

Glass Type	Glass Number (N)	Density d=gm/cm^3	n	Speed of light v m/s
Borosilicate BK7	517642	2.51	1.517	$1.91 * 10^8$
Crown K5	522595	2.59	1.522	$1.899 * 10^8$
Dense barium crown SK4	618551	3.57	1.618	$1.787 * 10^8$
Dense flint SF6	805254	5.18	1.805	$1.602 * 10^8$

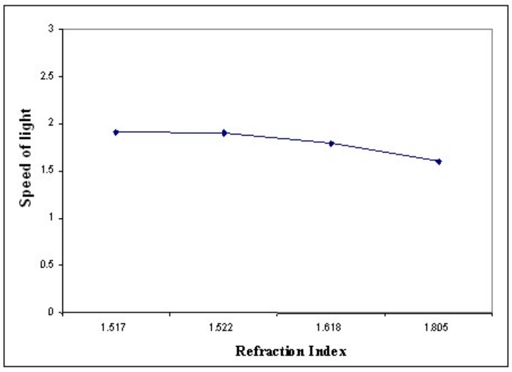

Figure 3. Relation between refraction Index(n) and speed of light in glass

3. 2. 2. The Total Delay Time

The total delay time for the circuit depends on total beam length and time delay inside the lens.

$T = t_p + t_L$ (8)

Where

T = The total delay time.
t_p = propagation time(path length delay).
t_L = delay time in the lens.

For instance; if we implement the circuit with path length of 2 μm and with lens thickness of .2 μm and made from dense barium crown SK4 then:

The total operation time = $2/(2.998*10^8 * 10^6) + 1.119 = .667 *10^{-14} + 1.119 = 6.67+1.119 = 7.789$ fs.

And these results are compatible with the fasted pulse (5 fs), which has been generated.

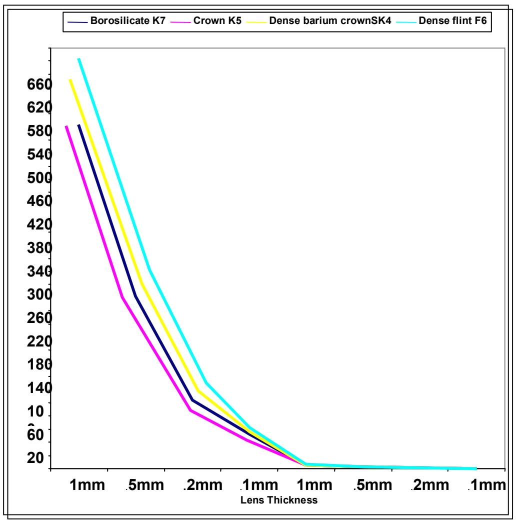

Figure 4. Delay comparison between the four types of glass at a different thickness.

3. 2. 3. Total delay time for selected path lengths, different glass type and thickness:

Glass type: Borosilicate K7:

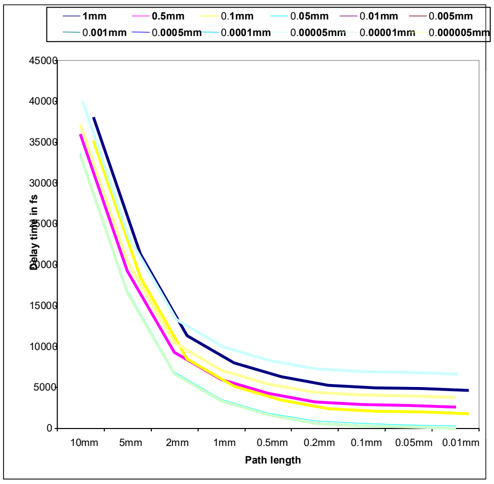

Figure 4. Total Operation time in fs for different thickness forBorosilicate K5.

Crown K5:

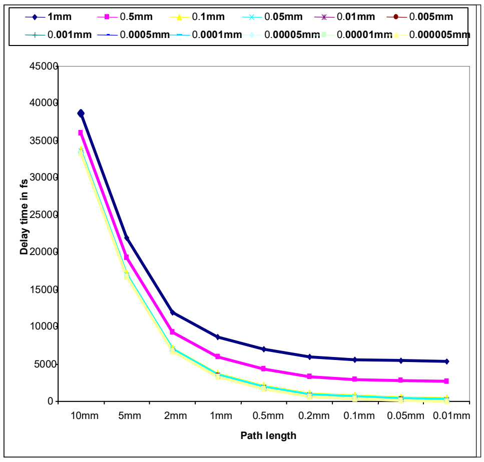

Figure 5. Total Operation time in fs for different thickness for Crown K5.

Dense barium crown SK4:

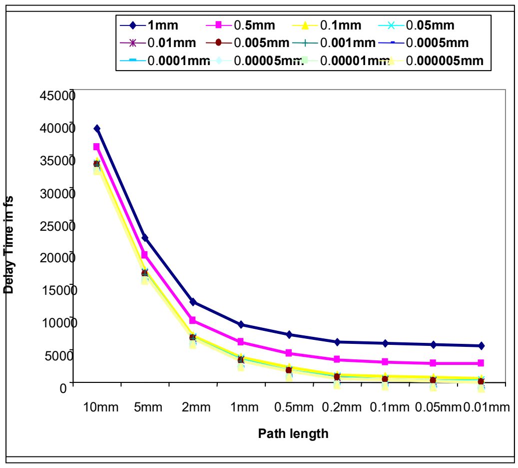

Figure 6. Total Operation time in fs, for different thickness for Dense barium Crown SK5.

Dense flint SF6:

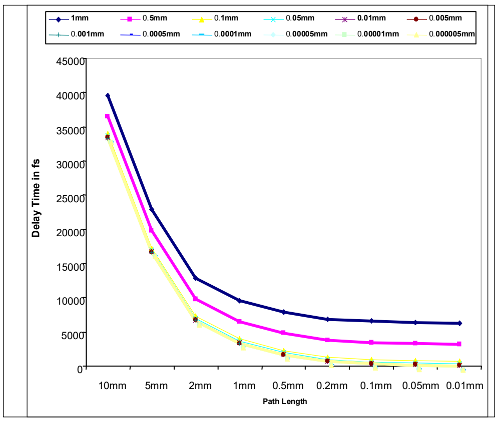

Figure 7. Total Operation time in fs, for different thickness for Dense flint SF5.

3.3 The Advantages of This Design:

1- It is all-optical circuit design, for all light spectral pulses except ultraviolet pulses and do not suffer of.
2- It is faster than any other design; it is almost, has no time in operation.
3- Its elements are stable and they are not affected with internal or external causes of miss operation or faults.
4- Depends on same type of light for inputs and outputs.
5- It is not affected by previous stages problems.

4. The Proposed AND circuit

Recall the digital circuit AND, it has two or more digital inputs X, Y, …., and N. These inputs have only two values logic 0 and logic 1, that's make total 2^N input alternatives for the circuit, ranged from X'Y'…N', which equal 00…0, to XY….N which equals 11….1. For two Inputs AND circuit the alternatives are equal to four cases, X'Y` equal to 00, X'Y which equal to 01, XY' which equal 10 and the last input alternative that has the value of XY which equal 11. The circuit has only one output depends on Boolean algebra, AND gate output logic 1; if and only if all inputs have the value of logic 1, otherwise its output equal to logic 0. The different operation states for digital AND circuit with two inputs, X and Y, are illustrated in table 3 [1].

Table 3, Truth table of AND logic circuit.

X	Y	X AND Y
0	0	0
0	1	0
1	0	0
1	1	1

4. 1. The Proposed Design Description

The proposed AND circuit uses reflection and interference laws. As shown in figure 9. The circuit has two inputs ports and one output port, two 50% polished flat mirrors m1 and m_2 and three thin lenses, L_1, L_2 and L_3. The function of the flat mirrors, m_1 and m_2 is to shift and reflect the input beams b_1' and b_2' towards the correspondent lens L_1 or L_2. The lenses L_1 and L_2 each of them gathers the direct input pulsed beam and the reflected pulsed beam from the correspondent mirror together at its focus where they interfere together and the result is passed to the lens L_3. The proposed circuit has three stages; First, input pulsed beams b_1 and b_2 and their complement b_1' and b_2'; Second, the resulted beams b_3, b_4 from the lenses L_1 and L_2 and third the final output from the lens L_3.

All of the three ports of the circuit work at the same range of frequencies and wavelength and their values are equal to digital logic 0 or logic 1. The circuit works upon incoming digital pulsed beams b_1 and b_2, from its two ports and outputs digital pulsed beam at its output port. Each of the two inputs beams is split to two beams, one moves direct to the correspondent lens as b_1 or b_2, and the other is shifted and reflected by the corresponding flat mirror m_1 or m_2 towards the opposite lens as b_1' and b_2' respectively.

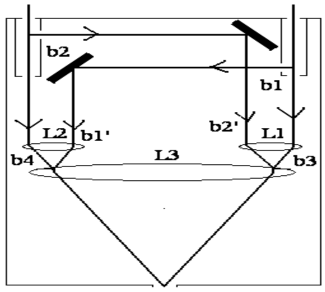

Figure 9, Structure of the proposed optical AND circuit

The function of the mirror m_1; is to reflect the beam b_1' towards the lens L_2. The function of the mirror m_2; is to reflect the beam b_2' towards the lens L_1. The beam b_1' has the same pulse shape like b_1 and has half amplitude of b_1, b_1' is a phase shift by half of the wave length which equal π (180°). On the other hand, b_2' is treated like b_1' when it falls on the mirror m_2. Though we have a pulsed shift phase beams b_1' and b_2' and their amplitudes is equal to half amplitudes of the beams b_1 and b_2.

The following scenario is followed in case of logical 1 for both of the two inputs beams:

- Since the transparency of the mirrors m_1 and m_2 =50%, so about 50% of the beam is refracted through each corresponding mirror and lost.

- Since the polishing ratio of the mirror m_1 and m_2 =50%. So, the corresponding mirror will reflect about 50% of the incident beam towards the appropriate mirror as a new beam. The reflected beam will have a phase shift by half of the wavelength of the original beam which equal π (180°).
- Since the transparency of the lens L_1=100% then 100% of the beam b_2' (which is phase shifted by half wavelength of the beams b_2 and the beam b_1) and 100% of the beam b_1 will bass to L_1 focus with their initial values and interfere together (destructive interference) producing the beam b_3 which has the same phase as b_1 and b_2 and 50% of b_1 amplitude.
- Since the transparency of the lens L_2=100% then 100% of the beam b_1' (which is phase shifted by half wavelength of the beams b_1) and 100% of the beam b_2 will bass to L_2 focus with their initial values and interfere together (destructive interference) producing the beam b_4 which has the same phase as b_1 and b_2 and 50% of b_2 amplitude.
- Since the amplitude of the new beams b_3 and b_4 is about 50% of the original one the transparency of the lens L_3=100% then 100% of the beam b_3 and the beam b_4 (have the same phase the beams b_1 and b_2) then 100% of the beam b_3 and the beam b_4 will pass to the lens L_3 focus with their initial values and interfere together (constructive interference) producing the output beam which has the same phase as b_1 and b_2 and 100% of their amplitude. Therefore, we can recognize illumination at the output port, which gives value of logic 1.

The following scenario is followed in case of logical 1 for only one of the inputs beams and the other one equal to logic 0:

- The original beam moves directly to its corresponding lens and passes through its focus.
- 50% is shifted by half of the wavelength and reflected from its correspondent flat mirror towards its corresponding lens as a new beam b_1' or b_2'.
- The new beams pass through the focuses of the lens $L_1$and L_2.
- L_3 gather the two beams at its focus, where they interfere together (destructive interference) and produces a beam with amplitude $\leq$ 50% of the original pulse which can be recognized as logical 0.

When the two inputs equal to logic 0, the values of the beams $b_1$and b_2 equal to logic 0, then both of b_1' and b_2' will equal to logic 0 because there is no illumination from the input ports. In such a case the resulting b_3 and b_4 will equal to logic 0 which leads to an output with the value of logic 0.

4. 2. Operation Verification

The standard AND circuit has two inputs b_1 and b_2, so its truth table has four cases, first case all inputs equal to logic 0, second and third one of them equal to logic 1 and the other equal to logic 0, forth all of the two inputs equal to logic 1. Table 4 shows the four case of operation:

1- **b_1=b_2= logical 0:** Of course, no illumination at the output exists at the output port and the resulting value =0.

2- **b_1=logical 0 and b_2= logical 1:**
- The phase of b_2 will be shifted by π and then reflected from the flat mirror m_1 towards the lens L_1 as b_2' with 50% of the amplitude of b_2.
- The original beam b_2 moves directly to the lens L_2 and passes through its focus as b_3.
- b_2' passes through the focus of L_1 as b_4.
- L_3 gather the two beams b_3 and b_4 at its focus, where they interfere together (destructive interference). Therefore, the resulting amplitude doesn't exceed 50% of the input amplitude and a weak illumination is recognized so the resulting value is logical 0.

3- **b_1=logical 1 and b_2= logical 0:**
- The phase of b_1 will be shifted by π and then reflected from the flat mirror m_2 towards the lens L_2 as b_1' with 50% of the amplitude of b_1.
- The original beam b_1 moves directly to the lens L_1 and passes its focus as b_3.
- b_1' passes through the focus of L_2 as b_4.
- L_3 gather the two beams b_3 and b_4 at its focus, where they interfere together

destructively. Therefore, the resulting amplitude doesn't exceed 50% of the input amplitude and a weak illumination is recognized so the resulting value is logical 0.

4- b_1=logical 1 and b_2= logical 1:

- As explained before, b_1 and b_2' (which has a 50% value of b_2 and its phase is shifted by π) interfere together, at the focus of L_1. Also, b_2 and b_1' (which has a value 50% of b_1 and its phase is shifted by π), interfere together, at the focus of L_2,
- The two beams b_3 and b_4 are collected near a minimum point of the interference field with a value about 50% of the original beam and has the same phase.
- L_3 gather b_3 and b_4 at its focus where they interfere together with a constructive interference (they have the same phase). So, output a ray with final illumination equal approximately to the sum of the incident rays in constructive interference, i.e. equal to b_3+ b_4=50% +50%=100% of the original beam, resulting a value of logic1.

4. 3. Delay Analysis

In analyzing of the circuit operation we find that it has three stages:

1- First stage; Using mirrors for shifting and reflecting 50% as b_x' (where x = 1,2.) and this stage doesn't affect the operation time where b1 and b2 are moving in air so the only delay of operation is path length.

2- Second stage; the lenses L_1 and L_2 which gather the beams b_1,b_2' and b_2,b_1' respectively and this stage is in parallel in time operation so the lenses must has the same thickness and the same type of glass to avoid un matched results at the last stage.

3- Third stage; The lens L3, which gather the resulted beams b3 and b4 from the previous stage to produce the final output and delay time depends on the thickness and the glass type of the lens.

Table 4. AND circuit behavior

b_2	b_1	b_1'	b_2'	b3	b4	output
0	0	Amplitude = 0	Amplitude =0	Amplitude = 0	Amplitude = 0	Amplitude = 0, value =0
0	1	Amplitude = 50% of b_1 shifted phase by π	Amplitude = 0	Amplitude = 100% same phase as b_1 value=1	Amplitude = 50% of b_1 shifted phase by π	Amplitude ≤ 50% of b_1 Destructive Interference value =0
1	0	Amplitude = 0	Amplitude = 50% of b_2 shifted phase by π	Amplitude = 50% of b_2 shifted phase by π	Amplitude = 100% same phase as b_2 value=1	Amplitude ≤ 50% of b_2 Destructive Interference value =0
1	1	Amplitude = 50% of b_1 shifted phase by π	Amplitude = 50% of b_2 shifted phase by π	Destructive Interference Amplitude = =50% same phase as b_1 or b_2	Destructive Interference Amplitude =50% same phase as b_1 or b_2	Constructive Interference Amplitude = 100% same phase as b_1 or b_2 value=1

The critical stages that affect the operation and make a delay in the circuit are the two stages of lenses; the first stage (mirrors doesn't affect the delay where the beams b_1 and b_2 are moving directly to the lenses). So we have two stages of lenses the beams must travel through. We suppose that all the lenses have the same thickness and the same type of glass then the total delay time in lenses is:

$$T = 2 * t_L \quad (9)$$

Where T, is the delay time in lenses.

t_L, is the delay time in one lens according to lens thickness and lens glass type.

The lenses delay time for the four glass types and different thickness is illustrated in figure 10.

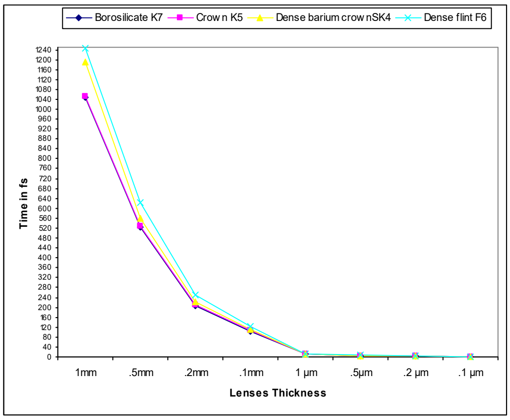

Figure 10, Delay time in fs for different thickness for glass types.

4. 4. Total Delay Time

The total operational time for the circuit depends on total path length and time delay inside the lens. For instance; if we implement the circuit with path length of 2 µm and with lens thickness of .2 µm and made from dense barium crown SK4 then:

The total operation time = time of passing the bath length + delay time in the lens. (10)

The total operation time = $2/(2.998*10^8 * 10^6) + 2.238$

$= .667 *10^{-14} + 2.238 = 6.67+2.238 = 8.908$ fs.

And these results are compatible with the fastest pulse (5 fs), which has been generated.

4. 4. 1. Total delay time for selected path lengths, different glass type and thickness:

delay time for propagation = path length in (m) / light speed in vacuum

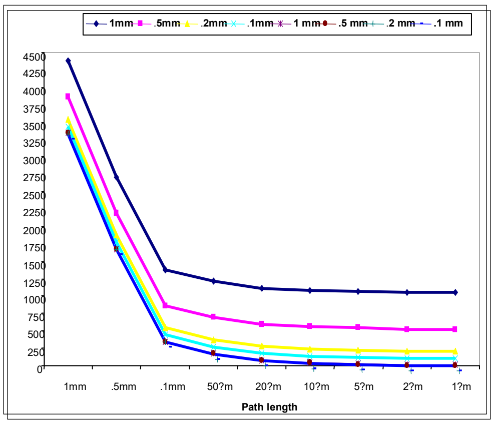

Figure 11. Total Delay time in fs for different Path lengths and different thickness for glass type Borosilicate K7

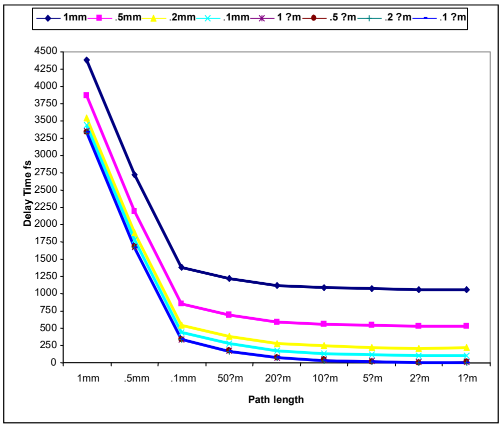

Figure 12. Total Delay time in fs for different Path lengths and different thickness for glass type Crown K5

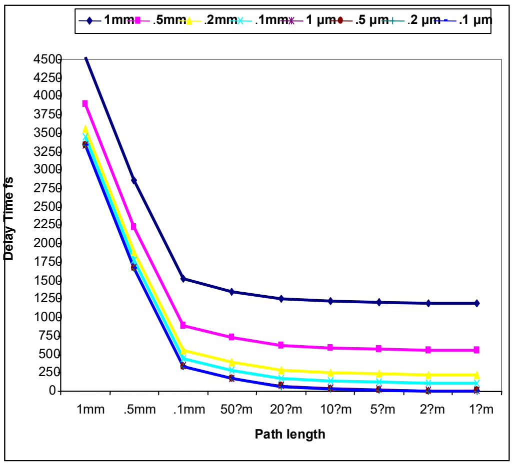

Figure 13. Total Delay time in fs for different Path lengths and different thickness for glass type Dense barium crownSK4

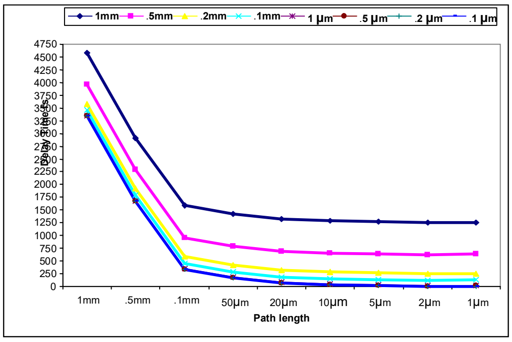

Figure 14. Total Delay time in fs for different Path lengths and different thickness for glass type Dense flint F6

4. 5. The Advantages of This Design

It is all-optical circuit design, for all light spectral pulses except ultraviolet pulses, which doesn't support.

It is faster than any other design; it is almost, has no time in operation.

Its elements are stable and they are not affected with internal or external causes of miss operation or faults.

Depends on same type of light for inputs and outputs.

It is not affected by previous stages problems.

4. 6. Design Enhancement

To make the circuit operates ideally we must be sure that its outputs amplitude value are exact equal logic 0 or logic 1. To eliminate the rising amplitude of the output cases 2 and 3 where one of the inputs equal to logic 0 and the other equal to logic 1. These values equal 50% of the input beam b1 or b2. the way to reduce these values to 0% is to add a 50% filter which eliminates an amplitude value of 50% of the original beam from the output such that the final output will be in the sequence 0,0,0,50% as an output. This leads to a decrease in the forth output which must equal 100% of the original signal so an amplifier must be attached to the circuit to solve this problem which amplify the output beam from the filter with 200% amplification power then the final output will be 0,0,0,100% which gives the binary values 0,0,0,1 as an ideal AND circuit outputs. The enhancement design is illustrated in figure 15.

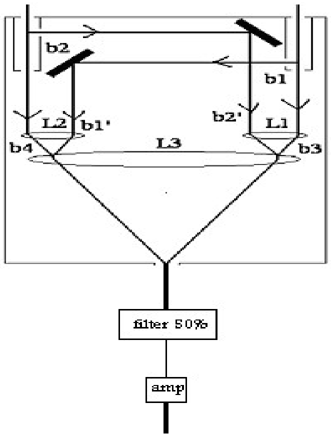

Figure 15, Structure of the enhanced proposed optical AND circuit

The verification of the new addition filter and amplifier is presented in table 13.

- When b1 = b2 =0 ,there is no illumination at the input port of the filter and consequently there is no signal to amplify then the output will equal logic 0.
- When either b1 or b2 = 1, then the input to the filter will have a maximum amplitude of 50% of the beam b1 or b2 in this case the filter will eliminate the beam amplitude and the output from the filter will equal 0 which leads to 0 output from the amplifier.
- When b1 and b2 equal to 1; in this case the input beam to the filter will equal 100% of the amplitude of the beam b1 or b2. the filter will reduce the beam amplitude to 50% of the original beam b1 or b2. The amplifier [9],will amplify the amplitude of the beam to 100% of the original beam b1 or b2 the final output will equal to logic 1.

Table 5. Enhanced AND circuit behavior

b_2	b_1	b_1'	b_2'	b_3	b_4	Output	Filter output	Amp. Output
0	0	Amplitude = 0	Amplitude = 0	Amplitude = 0	Amplitude = 0	Amplitude = 0	Amplitude = 0	Amplitude = 0 Value = 0
0	1	Amplitude = 50% of b_1 shifted phase by π	0	value=1 same phase as b_1	Amplitude = 50% of b_1 shifted phase by π	Amplitude = 50% of b_1 Destructive Interference value =0	Amplitude = 0 Value = 0	Amplitude = 0 Value = 0
1	0	0	Amplitude = 50% of b_2 shifted phase by π	Amplitude = 50% of b_2 shifted phase by π	value=1 same phase as b_2	Amplitude = 50% of b_2 Destructive Interference value =0	Amplitude = 0 Value = 0	Amplitude = 0 Value = 0
1	1	Amplitude = 50% of b_1 shifted phase by π	Amplitude = 50% of b_2 shifted phase by π	Destructive Interference Amplitude = =50% same phase as b_1 or b_2	Destructive Interference Amplitude = =50% same phase as b_1 or b_2	Constructive Interference Amplitude = 100% same phase as b_1 or b_2 value=1	Amplitude = 50% same phase as b_1 or b_2	Amplitude = 100% same phase as b_1 or b_2 value=1

4. 7. Multi-inputs AND Design:

4. 7. 1. Series Design

The pervious design for two input AND circuit can be use to design multi-input AND circuit by using multi-stages hierarchal two input AND for instance to design three input AND we need two circuits as illustrated in figure 16 [1].

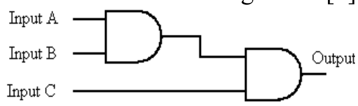

Figure 16. Three input AND structure.

The disadvantage for this design is input c is moving directly to the second stage where it may cause a difference in arrival time for the second circuit, this could led to un desired output in this case we need to delay the input C until the result of A and B arrive to the second input this can done by using extra AND gate in the first stage where it two inputs are connected to the input C; figure 17 demonstrate this idea. The AND circuit number 1.1 works as a buffer where its two inputs are connected to the input C and its output will be the same as the input C. this will resolve the synchronization problem [1].

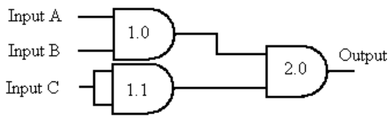

Figure 17. Three inputs synchronized AND structure.

A new problem will arise in multi-stage design which is time delay for circuit processing where delay time will equal to number of stages * time delay in the elementary circuit.

Total Delay Time = N * T (11)

Where N is number of stages, T is the delay time per stage

In case of three Input AND Time Delay will equal double of time delay of a single two inputs AND circuit, if the number of input is increased the total time delay will increase too.

4. 7. 2. Single chip Design

To make multi-inputs AND works at the same bit rate as the two inputs we need a new design to eliminate the delay of multi-stages design to accomplish this we need to reduce the amplitude of all inputs by a ratio of (N-1)/N (where N is the number of inputs) in the input stage this can done by using double slits with two narrow holes they allow only 1/N beam rays to pass. Then using a telescope consists of two lenses to gather the total beams in parallel, where the beam interfere together (constructive interference) producing a new beam with maximum amplitude equal to logic 1 the next step is to passing the resulting beam through a filter [4,5,9,10] which absorbs (N-1) /N of the original beam, after that the beam pass through an N*100 amplifier to get the final output. Figure 18 illustrates this design.

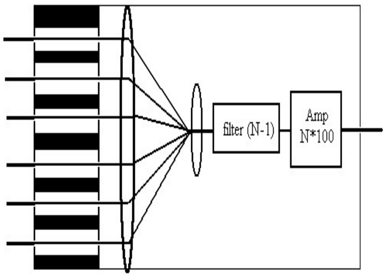

Figure18. Multi inputs direct AND structure.

5. The Proposed OR circuit

According to OR digital circuit function, it has two input, x and y; It has four inputs alternatives X'Y' which equal 00, X'Y which equals 01, XY' which equal 10 and the last input alternative that has the value of XY which equal 11. OR circuit always has an output value of logic 1 except when the two inputs X and Y are equal to logic 0 in this case the output of the OR circuit will equal logic 0. Table 6 illustrates OR truth table [1].

Table 6, Truth table of OR logic circuit.

X	Y	X OR Y
0	0	0
0	1	1
1	0	1
1	1	1

5. 1. The Proposed Design

The proposed OR circuit uses reflection and refraction laws. The circuit is shown in figure 19; it consists of three mirrors m_1, m_2 and m_3. The mirrors; m_1 and m_2 are high polished (90% polished) and they are flat mirrors. While mirror, m_3 is a mid polished mirror (70% polished) and it is a concave mirror. The circuit has two input and one output ports. All of the three ports works with the same range of frequencies and wavelength and their values is equal to logic 0 or logic 1. The circuit works upon incoming digital pulses from its two input ports and outputs digital pulse at its output port.

The function of the mirror m_1; is to reflect the beam b_1 near the center of m_3 as b_1'. And the function of the mirror m_2; is to reflect the beam b_2 near the center of the concave mirror m_3 as b_2'. The beam b_1' has the same pulse shape like b_1 but its amplitude is less than the amplitude of b_1 by 10% that the mirror m_1 transmit. This 10% is ignored and absorbed in the outer shield of the circuit. The beam b_1' is a phase shift by half of the wave length which equal π (180°). On the other hand, b_2' is treated like b_1' when it falls on the mirror m_2. Though we have a pulsed shift phase beams b_1' and b_2' and their amplitudes is 90% of the original beams b_1 and b_2.

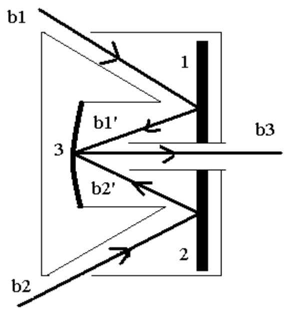

Figure 19, Structure of the proposed optical OR circuit

When b_1' and b_2' fall on the mirror m_3, it reflects 70% of the amplitude of the beams b_1' and b_2' as the beam b_3. The other 30% is transmitted and absorbed in the outer shield of the circuit. The phase of the beam b_3 is differ from the phase of b_1'and b_2' by half of the wave length which equals π (180°). That's mean that the beam b_3 has a shifted phase equal to one wavelength 2π (360°) of the original beams b_1 and b_2. Which indicate that it has the same phase as the original beams b_1 and b_2. The following scenario is followed in case of logical 1 input beam for either or both of the two inputs:

- Since the transparency of the mirrors m_1 and m_2 =10%, so about 10% of the beam is refracted through each corresponding mirror and lost.
- Since the polishing ratio of the mirror m_1 and m_2 =90%. So, the corresponding mirror will reflect about 90% of the incident beam towards the concave mirror m_3 as a new beam near its center. The reflected beam will have a phase

shift by half of the wavelength of the original beam which equal π (180°).

- Since the transparency of the mirror m_3=30% and the polishing ratio of its surface=70%. So, the mirror m_3 refracts about 30% and reflects 70% of the new beam that is phase shifted by half wavelength of the incident beams b_1'and b_2' and phase shift of one wavelength of the original beams b_1 and b_2.
- Since the amplitude of the new beam is about 90% of the original one. So, the final beam b_3 obtain about 63% (90%*70%) of the original beam for a single beam b_1 or b_2. Therefore, we can recognize illumination at the output port, which gives value of logic 1.
- Since the beams are in the same phase, b_1'and b_2' and the amplitude of both of them equal to 70% of the original beams, so when they reflected from the mirror m_3 they still has the same phase so they will interfere together (constructive interference) and produce beam b_3 and the amplitude of the final beam, beam b_3 will equal 2* 63% = 1.2 of one of the original beams b_1 or b_2, so we can recognize high illumination at the output port, which gives value of logic 1.

5. 2. OR operation verification:

The OR circuit has two inputs b_1 and b_2, so its truth table has four cases, the different alternatives are illustrated in table 7:

1- b_1=b_2= logical 0:
   - Of course, no illumination at the output exists and b_3= 0.

2- b_1=logical 0 and b_2= logical 1:
   - The beam b_2 fills on the appropriate flat mirror m_2.
   - Approximately 10% of b_2 is refracted through the mirror m_2 and lost.
   - The flat mirror m_2 reflects about 90% of the incident beam b_2 towards the concave mirror m_3 as b_2', and near to center of m_3.
   - The mirror m_3 refracts about 30% and reflects 70%of the incident beam b_2', so the final beam b_3 obtain about 63% of original beam b_2. Therefore, we can recognize illumination at the output port, which gives value of logic 1.

3- b_1=logical 1 and b_2= logical 0:
   - The beam b_1 fills on the appropriate flat mirror m_1.
   - Approximately 10% of b_1 is refracted through the mirror m_1 and lost.
   - The flat mirror m_1 reflects about 90% of the incident beam b_1 towards the concave mirror m_3 as b_1', and near to center of m_3.
   - The mirror m_3 refracts about 30% and reflects 70%of the incident beam b_1', so the final beam b_3 obtain about 63% of original beam b_1. Therefore, we can recognize illumination at the output port, which gives value of logic 1.

4- b_1=logical 1 and b_2= logical 1:
   - The beams b_2 and b_1 acts exactly as mentioned in 2 and 3 respectively. The amplitude of b_1'= the amplitude of b_2'=90% of the original beams b_1 and b_2.
   - Therefore, the mirror m3 refracts about 30% and reflects 70% of both incident beams b_1' and b_2'. The amplitude of b_3=70% of b_1'+ b_2' =70%* (2*90%) =126% of original beam b_1 or b_2 where we can recognize illumination at the output port, which gives value of logic 1.

The resulting output beam for all cases has the same phase as the input beams, so there is no shift phase just a delay of one wavelength of the original beams according to use two stages of mirrors in the circuit.

5. 3. Operation Analysis:

In the study of the circuit operation we will use analytical study for different range of infrared light beams from near IR (λ = 800 nm) to (λ = 3000 nm). To work at 500 femtosecond operation time, the longest path of any beam must not exceed $3 * 10^8 * 500/ 10^{15} = 150$ µm. The total path length is measured by the distance between the input port and the flat mirrors, the distance between the flat mirrors and the concave mirror and the distance between the concave mirror and the output port.

Table 7. OR circuit behavior

b_2	b_1	b_1' after reflection from m_1	b_2' after reflection from m_2	Output (b_3)
0	0	Amplitude =0 no illumination from the input port	Amplitude =0 no illumination from the input port	Amplitude =0 no illumination at the output port
0	1	Amplitude = 90% of b_1 shifted phase by π	Amplitude =0 no illumination from the input port	Amplitude = 0.9*0.7 = 63% of b_1 same phase as b1, value =1
1	0	Amplitude =0 no illumination from the input port	Amplitude = 90% of b_2 shifted phase by π	Amplitude =0.9*0.7 = 63% of b_2 same phase as b2, value =1
1	1	Amplitude = 90% of b_1 shifted phase by π	Amplitude = 90%vof b_2 shifted phase by π	Amplitude =(0.9*0.7)*2= 126% of b_1 or b_2 same phase as b_1 and b_2, value =1

When we analyze the delay parts in the circuit, we find that only tow stages of mirrors are used in the circuit. The distance between the two flat mirrors and the concave mirror, depends on the focal length of the concave mirror. The position of the two flat mirrors must be grater than or equal to double of the focal length of the concave mirror to avoid multi reflection or unwanted interference. So the first major factor in measuring the delay time depends on the focal length of the concave mirror. The second factor is one wavelength delay according to two shift phase by π (360°). This delay is fixed and it is depending on the type of light rays used as inputs.

5. 4. The delay time for different focal lengths:

We assume that the flat mirrors are positioned such that the beam will travel double of the focal length of the concave mirror.

$$P_f = 2 \times M_f \qquad (12)$$

Where P_f : is path length between flat mirror and the concave mirror

M_f : is the concave mirror focal length

Figure 20 presents the delay time for different focal lengths.

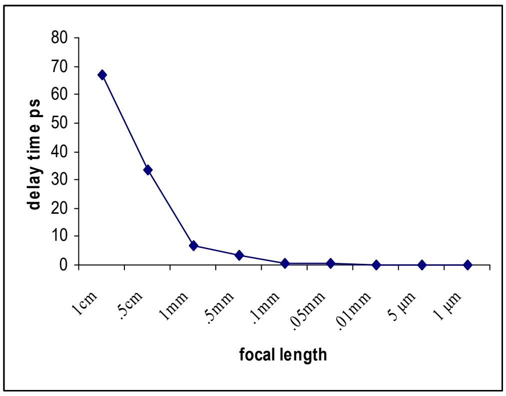

Figure 20, delay time according to different focal lengths.

According to reflection low, the angle of incidence is equal to the angle of reflection so the distance between the mirror and a parallel line to it is fixed for all points on the line, so the if we draw a line behind the concave mirror parallel to the flat mirrors, and if we assume that the input ports are in the region of this line, hence the distance between the mirror and the input port will equal the distance between the flat mirror and the center of the concave mirror.

With the assumption that the flat mirrors are positioned such that the beam will travel double of the focal length of the concave mirror so the path length of the beam from the input port to the center of the concave mirror will equal to the four time of the focal length of the concave mirror. We assume that output beam will travel double of the distance of the focal length of the concave mirror. Then the total distance that a beam must travel from the input port to the output port will equal six times the focal length of the concave mirror.

Total path length = 6 x M_f. (13)

Delay Time = Total path length /c (14)

Where c is the speed of light in vacuum. Figure 21 illustrates the total path length delay time for different focal lengths.

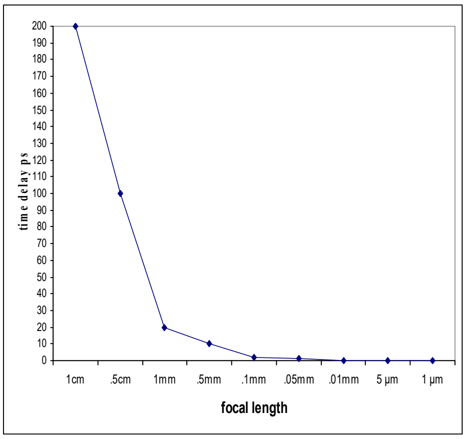

Figure 21, Total path length delay according to different focal lengths.

We have mentioned that the input pulses is affected by two delay shift phases according to the two stages of mirrors and the value of the two shifting delay is equal to λ/2 where (λ is the wave length of the input beams) that is giving us a total delay of λ which is differ for any wavelength in the light range of wave lengths. We shall demonstrate the different delay value for the range of IR wavelengths; wavelength delay is presented in figure 22.

Wave length delay = λ/c. (15)

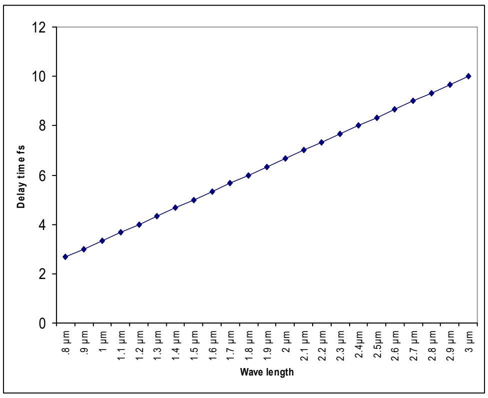

Figure 22, delay time for different wavelengths.

5. 5. Delay Analysis

5. 5. 1. Total Delay Time:

The total operation time of the circuit is represented by the summation of propagation time and frequency shifted time. It is defers from one implementation to another where it is affected by path length of propagation inside the circuit and the wavelength of the input pulses.

5. 5. 2. Bit Rate Analysis:

Since the circuit is a binary logic gate, the output will not be more than one bit at a time so its total operation time representing the time it used it to output only one bit. For instance if we use a concave mirror with focal length equal to 1 μm and the input pulse's wavelength equal to 1800 nm then the total operation time = 20.0+ 6.0 = 26 fs. The bit rate for this implementation will equal to $10^{15}/26$ = 38461538461538 bits/s which equal 34.98 Tb/s.

5. 5. 3. The Advantages of This Design:

It is all-optical circuit design, it is support all light spectral pulses.
It is faster than any other design; it is almost, has no time in operation.
Its elements are stable and they are not affected with internal or external causes of miss operation or faults. Depends on same type of light for inputs and outputs. It is not affected by previous stages problems.

5. 6. Design Enhancement

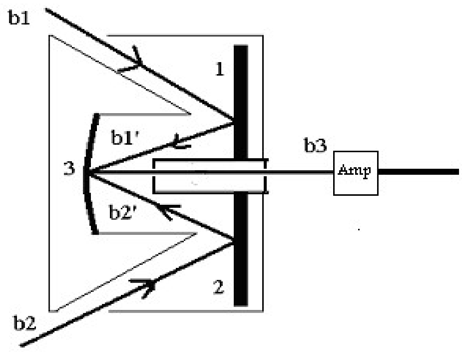

Figure23. Structure of the Enhanced proposed optical OR circuit

To ensure that the circuit can be added in a serial or parallel connections to other circuits and doesn't affect the system operation, we must insure that its outputs doesn't exceeds or less than the optical pulse logic 1. To get this:

1- We insert two vertical slits in the front of the concave mirror m3. Each slit have a narrow opaque so that it allows only maximum of 50% of the original beam rays to be passed as the output beam b3 (see figure 23).

Table 8. Enhanced OR circuit behavior

b_2	b_1	b_1' after reflection from m_1	b_2' after reflection from m_2	Output (b_3)	Final output after 200% amplification
0	0	Amplitude =0 no illumination from the input port	Amplitude =0 no illumination from the input port	Amplitude =0 no illumination at the output port	Amplitude =0 no illumination at the output port
0	1	Amplitude = 90% of b_1 shifted phase by π	Amplitude =0 no illumination from the input port	Amplitude = 50% of b_1 same phase as b1, value =1	Amplitude = 100% of b_1 same phase as b1, value =1
1	0	Amplitude =0 no illumination from the input port	Amplitude = 90% of b_2 shifted phase by π	Amplitude =50% of b_2 same phase as b2, value =1	Amplitude =100% of b_2 same phase as b2
1	1	Amplitude = 90% of b_1 shifted phase by π	Amplitude = 90%vof b_2 shifted phase by π	Amplitude 50% of b_1 or b_2 same phase as b_1 or b_2, value =1	Amplitude 100% of b_1 or b_2 same phase as b_1 or b_2,

2- An optical amplifier is attached to the circuit with 200% amplification power.

The resulting beam will equal 100% of the original input beam b1 or b2. The behavior of the circuit is presented in table 8.

5. 7. Multi-inputs OR Design:

5. 7. 1. Series/Multi-Stages Design:

The simplest design for multi-inputs gate is to divide the number of inputs N by two in series fashion until we find the last stage is less or equal 2. To demonstrate this suppose we have thee inputs, A, B and C, where N = 3 in this case. The first stage will have a single OR circuit (the division of 3 by 2 equal to integer 1 and the reminder equal to 1). In first stage we can connect AB, AC or BC. The reminder input (A, B or C) will be connected with the output of the first stage to the second OR circuit. This design is illustrated in figure 24.

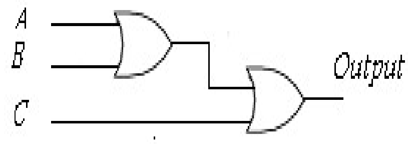

Figure 24. Three input OR structure.

In this design the Input C is reaching the second or gate faster than the output of the first one. This will leads to operational faults and leads to wrong final results. The solution for this problem is to synchronize the Input signals at every stage to grantee same time arrival for the second OR gate. This can be done by adding a third OR gate to the Input C in the first stage. This gate works only as a buffer with the same time slot as the first OR gate this synchronization is illustrated in figure 25.

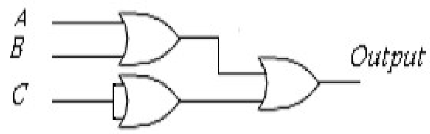

Figure 25. Three inputs synchronized OR structure.

A new problem will arise in multi-stage design which is time delay for circuit processing where delay time will equal to number of stages * time delay in the elementary circuit.

Total Delay Time = N * T (16)

Where N is number of stages, T is the delay time per stage

5. 7. 2 Single chip's Design

The optical system for Multi-inputs single chip as illustrated in figure 26; consists of two parts. Two convex lenses works as a telescope to gather the input beams as a single beam with high Illumination and its amplitude equal to the sum of all Inputs amplitudes. The second part is a two narrow parallel slits which allow only a part of the beam to pass with amplitude equal to only one input and the rest of the rays are absorbed in the outer shield. This circuit gives logic one if one or more of its N inputs equal to logic 1 otherwise its outputs will equal to logic 0.

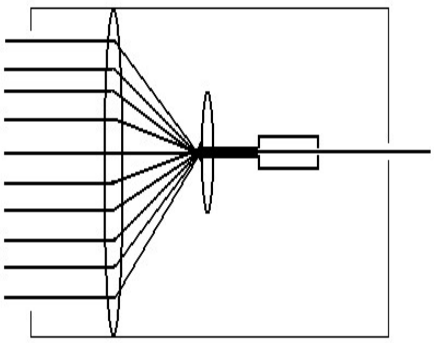

Figure26. Multi inputs single chip OR structure.

6. Conclusion & Future Work

We have presented a logical design of all optical digital NOT, OR and AND circuits. The proposed design depends on mirrors, lenses and properties of light using infrared rays as inputs. Operation and Functions of these circuits were also proved. Enhancement of design was presented and multi-inputs circuit design has been demonstrated. In future we shall:

- Try to propose a new design depends on quantum theory
- simultaneous multi wavelength processing
- Image and multimedia transmission and processing as a single pulse

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