Yield Maximization of TiO_2 Memristor-Based Memory Arrays

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***Abstract*— The missing fourth passive circuit element, the memristor, attracted a great attention when HP labs developed the first real memristor device in 2008. The memristor manufacturing is facing various challenges due to the difficulty to control its process variation, as it is fabricated at nano-scale geometry's size. Process variation result in deviating the actual electrical behavior of memristors from the desired values. This deviation results in reducing the yield especially in the memristor-based memory design. Therefore, it is very important to understand and characterize the impact of process variation on memristor performance and yield and attempt to maximize the yield of the memristor-based memory arrays.**

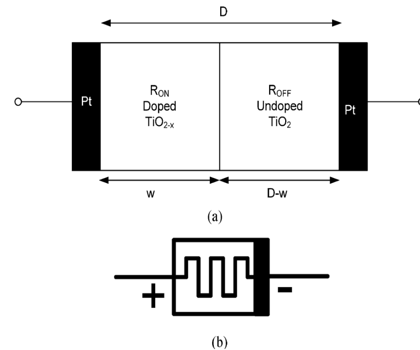

Fig. 1. (a) TiO_2 Memristor of length D, (b) TiO_2 Memristor symbol [4].

I. INTRODUCTION

A new nanometer device, memristor has drawn a significant interest from the research community. Memristor was first theoretically predicted by L.Chua in 1971 [1]. It is considered the fourth fundamental circuit element, to complete the set of passive devices that previously includes only resistor, capacitor, and inductor [2]. In 2008, the first physical realization of memristor was demonstrated by HP Lab, in which the memristive effect was achieved by moving the doping front along TiO2 thin-film device [3].

HP memristor is a thin film sandwiched between two metallic contacts (Fig. 1.a) [4]. The memristor symbol is also portrayed in (Fig. 1.b). The memristor is a very small device that can be split into two main parts: I) a high doped region with low resistance (R_{on}), and II) a low doped region with high resistance (R_{off}). Low doped region consists mostly of TiO_2; however the high doped region consists of TiO_{2-x}. The high doped region contains more oxygen vacancies which makes its resistance less than that of the low doped region. R_{on} and R_{off} notations represent the high doped and low doped regions respectively [5][6][7]. Moreover, the memristor has the ability to retain the state for a long time after the current has been switched OFF. Due to its ability to remember past charges, an intuitive utilization for it is to be used in memory design [8]. Memristor shows many promising characteristics as the next-generation data storage device [2], such as non-volatility, low power consumption, high performance, high density and excellent scalability [3] [9].

Sub-wavelength photolithography (i.e., at nano-scale devices) results in critical device parameter fluctuations, incurred by process variations, which is a critical concern affecting the device performance [3] [9]. The impact of process variations on a memristive system is more severe than a conventional digital design because of the utilization of the analog states of memristors. The process variations sources are line-edge roughness (LER), oxide thickness fluctuation (OTF), and random discrete doping (RDD) [10].

The rest of the paper is organized as follows. In Section II, Some preliminaries about the memristor device are presented. The memristor process variations model utilized in this paper is illustrated in Section III. Section IV highlights the simulation results and discussions. Finally, some conclusions in Section V.

II. PRELIMINARIES

The semiconductor thin film has a certain length *D*, and consists of two layers of titanium dioxide films. One is highly resistive pure TiO_2 (un-doped layer), and the other is filled with oxygen vacancies, which makes it highly conductive (doped layer). The state variable *w* represents the width of the doped region (TiO_{2-x} layer) the doped region has low resistance while that of the un-doped region is much higher [10]. As an external voltage bias is applied across the device, the electric field repels positively charged oxygen vacancies in the doped layer into the pure TiO_2 layer resulting the length *w*. Hence, the device's total resistivity changes. If the doped region extends to the full length, that is *w/D*=1, the total resistivity of the device is dominated by the low resistivity

region, with a value measured to be R_{on}. Likewise, when the undoped region extends to the full length *D*, *w/D=0,* the total resistance is denoted as R_{off}. The main parameter of the memristor are R_{on} and R_{off}, the device resistance is bounded between [10]:

$$R_{on} \le R(w) \le R_{off} \quad (1)$$

According to [1], the memristor has memory effect since the device maintains its resistivity even if the power goes off. According to the reported device characteristics [1][11] [12], oxygen vacancies do not move around by themselves. They become absolutely immobile until voltage is applied again. This unique characteristic makes the memristor standout from other devices such as diode. The mathematical model for memristive device resistance can be described as [10]:

$$R(w) = (R_{on}.w/D + R_{off}.(1 - w/D)) \quad (2)$$

The state of the memristor changes according to the amount of flux injection. When the memristor state is controlled by the input flux across the cell, this input flux is given by [10]:

$$\phi = \frac{\phi_D}{R_{off}^2}\left[R_{off}^2 - R_{on}^2\right] \quad (3)$$

$$\phi_D = \frac{(\beta D)^2}{2\mu_v(\beta - 1)} \quad (4)$$

Where β denoted the $R_{on} = \beta.R_{off}$ ratio, μ_v is the mobility.

In the rest of paper, without loss of generality, we use *x* and x' to represent the design value and the actual value under process variations for any given variable *x*, respectively. Very recently, a Monte-Carlo simulation method was proposed to analyze the impact of geometry variations on the electrical properties of TiO_2 thin-film memristors [8]. A 3D device structure including the geometry variation information is generated by performing a sanity check of the device characterization parameters. In the Monte-Carlo simulations, the memristor device is divided into many small filaments sandwiched between two electrodes. Within a filament *i*, the cross-section area $s_i^{'} = l_i^{'}.z_i^{'}$ and thickness $D_i^{'}$, considered as constants, whose value can be modeled by taking into account the effects of LER or OTF, respectively [13].

III. MEMRISTOR MODEL ANALYSIS

In our model, we take the memristor variations and yield analysis into account. The total memristance $M^{'}$, which is a time-varying parameter, can be uniquely defined by $R_{off}^{'}$, $R_{on}^{'}$, and $\alpha^{'}(t)$. In this section, we examine the variations of $R_{off}^{'}$, $R_{on}^{'}$, and $\alpha^{'}(t)$. Then, we will derive the corresponding process-variation aware memristance model. We summarizes the designed values of the TiO_2 memristor geometry dimensions and its electrical parameters adopted in our work. For a given TiO_2 memristor, we use $R_{off}^{'}$ and $R_{on}^{'}$ to denote its actual highest and lowest total memristances, respectively [13].

$$R_{off}^{'} = R_{off}.\eta(\mu R_{off} + \sigma R_{off}.E).(1 + \sigma_y.D_p) \quad (5)$$

$$R_{on}^{'} = R_{on}.(\mu R_{on} + \sigma R_{on}).E \quad (6)$$

Here, two independent random numbers $E \sim N(0,1)$ and $D_P \sim N(0,1)$ are introduced. *E* represents the correlation between $R_{off}^{'}$ and $R_{on}^{'}$ due to the same geometry variation sources D_P *and* σ_y represents the impact of RDD. By running extensive numerical simulations under various conditions, we found the actual $\alpha^{'}$ can be modeled as the product of the designed value α, where α =*w/D* and a coefficient η that represents the influence of process variations as [13]:

$$\alpha^{'} = \eta.\alpha \quad (7)$$

Here η can be expressed by [13]:

$$\eta = \frac{1}{(1 + \phi.\varepsilon_2 + \phi.\varepsilon_2(\omega_1.E + \omega_2.G)).(1 + \sigma_y.D_P)} \quad (8)$$

To avoid overestimating the impact of geometry variations on $\alpha^{'}$, a new random number $G \sim N(0, 1)$ is introduced to offset the impact of LER. ε_1 and ε_2 are two scalars extracted from the actual simulations performed by the device simulator.

The coefficients ω_1 and ω_2 represent the weights of *E* and *G*, where $\omega_1^2 + \omega_2^2 = 1$. By modeling $R_{on}^{'}$, $R_{off}^{'}$ and $\alpha^{'}$, the total memristance $M^{'}$ of a TiO_2 memristor can be simply calculated by [13]:

$$M^{'}(\alpha) = R_{on}^{'}.\alpha^{'} + R_{off}^{'}.(1 - \alpha^{'}) \quad (9)$$

IV. SIMULATION RESULTS AND DISCUSSIONS

We observed from our calculations that the failure percentage in the case of reading '0' is much lower than that in the case of reading '1'. As an intuitive example, the memristance (*M*) is given by:

$M(\alpha) = R_{on}\alpha + R_{off}(1 - \alpha)$ (10), α =*w/D*,

when α = 0, *M* = R_{off}. If α, due to process variation equals 0.001 (assuming R_{on}=200 Ω and R_{off}=200 kΩ), *M*= 0.001* R_{off} +0.999* R_{off} ≃199.8 kΩ with an error of 0.1%.

However, for $\alpha = 1$, $M = R_{on}$. If α, due to process variation equals 0.999, $M = 0.001 * R_{off} + 0.999 * R_{off} \cong 400\Omega$ with an error of 100%. Accordingly, we will consider only the case when $\alpha = 1$ which dominated the overall memory failure probability. Similarly, the failure percentage in the case of writing '0' is much lower than that in the case of writing '1'. Following that, the model introduced in Section III has been adopted to find the probability density function of the Memristance, M', with $\alpha = 1$.

A. WRITING YIELD OPTIMIZATION

In the case of the writing '1' operation, the input writing flux should be adjusted to change the memristor device's memristance from R_{off} to R_{on}, which is given by equation (3). In this case, all the memristor devices should have their Memristance M' less than a given threshold (normally selected to be midway between R_{on} and R_{off}, typically, $[(R_{on} + R_{off})/2]$). Since in the case of $\alpha = 1$, the ideal memristance without variations should equal R_{on}, variations result in making the memristance of some memristor devices deviates from R_{on} and becomes larger than the threshold.

The writing yield is defined as the number of memristors samples (out of 5000 samples in our simulations) that exhibit correct writing operation (i..e, their memristance is less than the mid-way threshold when variations is taken into account). In order to maximize the writing yield, the input flux is changed by changing the input voltage amplitude as well as reading duration time to achieve the maximum possible writing yield.

The following simulation results provide an important design insight to the memristor-based memory array designers as follows. If the designer ignores the variations and find only the input writing flux that changes the memristance value from R_{off} to R_{on}. This flux will not achieve the maximum writing yield. However, if the designer considers the variations, a new flux value should be used that results in maximizing the yield. Here, the writing yield is defined as the percentage of memory cells that are written correctly (i.e., the cells that are written as '1' when they are desired to store '1' with no failure). Once again, the case of writing '0' provide very small failure probability compared to the writing '1' case. Therefore, only the writing '1' case (i.e., $\alpha = 1$) is considered in this paper.

Figs. 2 and 3 portray a comparison of the writing yield for different memristor sizes when the normal input writing flux given in equation (3) is used (i.e., no writing yield maximization and the variations are not compensated) and when the optimal input writing flux is used (i.e., the writing yield is maximized and the variations are taken into account). It is obvious from Fig. 2 that increasing the device dimensions results in reducing the variations and accordingly, increase the yield. For example, when D=3nm and l=z=10nm; where D, l, and z are the memristor's dimensions; the device yield equals 89.67 % whereas when D=3nm and l=z=100nm, the device yield equals 98.63%, when variations are ignored.

Changing the flux to maximize the yield results in improving the yield for the first case (i.e., D=3nm and l=z=10nm) from 89.67% to 92.2% and in the second case (D=3nm and l=z=100nm) from 98.63% to 98.91%.

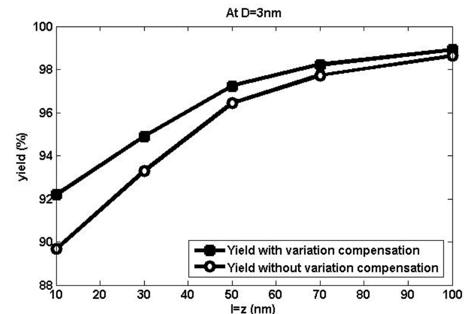

Fig.2 Yield in case D=3nm

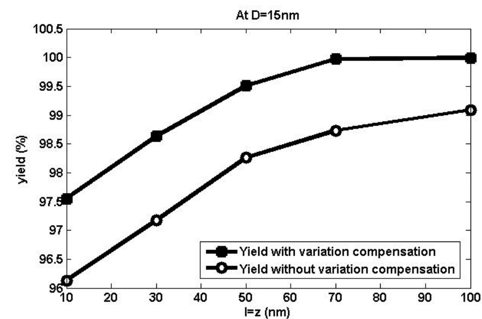

Fig.3 yield in case D=15nm

In addition, it is obvious from Figs. 2 and 3 that as the device dimensions increase, the variations decrease and the corresponding writing yield increases. For example, when D=15nm and l=z=10nm, the device yield equals 96.13% whereas when D=15nm and l=z=100nm, the device yield equals 99.09%, when variations are not compensated. However, when the optimal input writing flux is used to maximize the writing yield, the writing yield is improved for the first case (i.e., D=15nm and l=z=10nm) from 96.13% to 97.55% and in the second case (D=15nm and l=z=100nm) from 99.09% to 99.99%.

B. READING YIELD OPTIMIZATION

In the case of reading '1' which dominates the failure probability as explained earlier, the device's memristance, M',

is compared to a certain threshold which is selected to be 50% (mid-way) between R_{on} and R_{off}, typically, $[(R_{on} + R_{off})/2]$). To optimize the reading yield, this threshold has been varied to find the optimal threshold that results in maximum reading yield. The reading yield is defined in a similar way as the writing yield. In order to maximize the reading yield, the threshold is changed to achieve the maximum possible reading yield.

In Figs. 4 and 5, the reading yield achieved when the threshold is selected at 50% is plotted versus the maximum reading yield achieved when the optimal threshold values are used for different memristor device' dimensions. In Fig.4, D=3nm and l, z vary from 10nm to 100nm. When the 50% threshold is used, the reading yield equals 89.67% at l=z=10nm and equals 98.63% at l=z=100nm. However, when the optimal threshold is adopted, the reading yield equals 100% in all cases of l, z. Similar results are shown in Fig. 5 for D = 15nm.

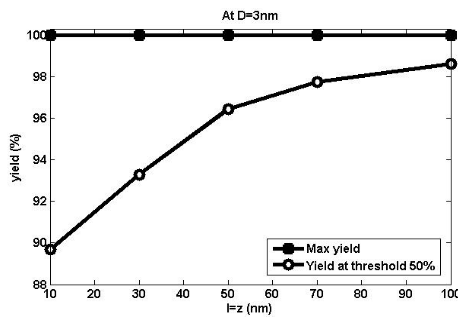

Fig.4 yield in case D=3nm

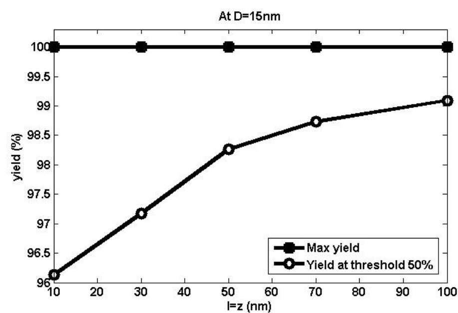

Fig.5 Max yield in case D=15nm

V. CONCLUSION

In this work, we evaluate the impact of process variations on the electrical properties of TiO_2 thin-film memristors, by conducting the analytic modeling analysis and Monte-Carlo simulations. The paper has attempted to improve the device writing and reading yields by finding the optimal writing input flux and the optimal threshold, respectively. The extension of this work is to find a closed form solution for the writing yield and the reading yield in terms of the memristor device's dimensions, threshold, input flux, ..etc. When this closed form solution exist, an optimization problem can be solved to achieve the optimal parameters that maximize the writing and the reading yields.

VI. ACKNOWLEDGMENT

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REFERENCES

[1] L. Chua. Memristor-the missing circuit element. IEEE Transaction on Circuit Theory, pages507–519, 1971.

[2]D. B. Strukov et al. The missing memristor found. In Nature, volume 453, pages 80–83, 2008.

[3] D. Niu, Y. Chen, C. Xu, and Y. Xie. Impact of process variations on emerging memristor. In Design Automation Conference (DAC), pages 877–882, 2010.

[4] Budhathoki, R.K., Sah, M.P., Adhikari, S.P., Hyongsuk Kim and Chua, L. Composite Behavior of Multiple Memristor Circuits. IEEE Transactions on Circuits and Systems I: Regular paper, vol 60, no.10, 2013.

[5] Y. Ho, G. M. Huang, and P. Li. Nonvolatile memristor memory: device characteristics and design implications. In International Conference on Computer-Aided Design, pages 485–490, 2009.

[6]Elshamy, M., H. Mostafa, and S. Said. Design Considerations/Insights for Memristor-Based Memory Arrays. IEEE International Conference on Engineering and Technology (ICET'14), Egypt, IEEE, In Press.

[7] Elshamy, M., H. Mostafa, and S. Said. New Non-Destructive Read/Write Circuit for Memristor-Based Memories. IEEE International Conference on Engineering and Technology (ICET'14), Egypt, IEEE, In Press.

[8] H. Elgabra, I. Farhat, A. Al Hosani, D. Homouz, B. Mohammad. Mathematical Modeling of a Memristor Device. International Conference on Innovations in Information Technology (IIT), pages 156–161, 2012.

[9] M. Hu, H. Li, Y. Chen, X. Wang, and R. Pino. Geometry variations analysis of tio2 thin film and spintronic memristors. In Asia and South Pacific Design Automation Conference (ASP-DAC), pages 25–30, 2011.

[10] Y. Ho, G. Huang and P. Li. Dynamical Properties and Design Analysis for Nonvolatile Memristor Memories. 724 IEEE Transactions on Circuits and Systems—I:Regular papers, vol. 58, NO. 4, APRIL 2011.

[11] Y. Ho, G. M. Huang, and P. Li. Nonvolatile memristor memory: device characteristics and design implications. In International Conference on Computer-Aided Design, pages 485–490, 2009.

[12] L. O. Chua. Device modeling via basic nonlinear circuit elements. IEEE Trans. Circuits Syst., vol. CAS-27, pages 1014–1044, Nov. 1980.

[13] M. Hu, H. Li, R. Piano. Fast Statistical Model of TiO2 Thin-Film Memristor and Design Implication. The International Conference on Computer-Aided Design, pages 345-352, 2011.