A 4-Bit 6GS/s Time-Based Analog-To-Digital Converter

Assem S. Hussein[1], Mahmoud Fawzy[1], M. Wagih Ismail[1], Mohamed Refky[1], and Hassan Mostafa[2]
[1,2]Department of Electronics and Electrical Communications Engineering Cairo University 12613, Giza, Egypt.
[2] Center for Nanoelectronics and Devices, AUC and Zewail City of Science and Technology, New Cairo 11835, Egypt.
assem.s.hussein@ieee.org; mahmoud_fawzy_93@hotmail.com;
wagih.ismail@eng.cu.edu.eg;m6amin@uwaterloo.ca;hmostafa@uwaterloo.ca

***Abstract*— This paper proposes a 4-bit 6GS/s Time-Based Analog-to-Digital Converter (TADC) to be integrated inside the Software Defined Radio (SDR) receivers. The TADC is mainly composed of two blocks which are the Voltage-to-Time Converter (VTC) and the Time-to-Digital Converter (TDC). A prototype of the proposed TADC is implemented using 65 nm technology with a sampling rate of 6GS/s. An ENOB of 3.68 is achieved for an input frequency of 1.331 GHz. The whole system consumes a total power of 21.4 mW.**

I. Introduction

Analog-to-Digital Converters (ADCs) are very important electronic modules. Any communication receiver or even any device that needs an analog interface must contain an ADC. Also it's an important part of most embedded systems applications that communicate with analog interfaces.

The target of the proposed ADC is to be integrated inside a Software Defined Radio (SDR). The SDR receivers are the main research focus these days for Ultra-Wide-Band (UWB) Fourth Generation (4G) receivers. The idea of these UWB receivers is to convert the noisy RF signal coming from the antenna to the digital domain. Consequently, all the analog processing blocks are removed. Therefore, the signal will be converted directly to the digital domain to be processed by the digital processing blocks. Processing the signal in the digital domain is ought to decrease the power tremendously while preserving high accuracy and resolution.

The Time-Based Analog-to-Digital Converter (TADC) is considered an essential block in designing software defined radio receivers because it exhibits higher speed and lower power consumption compared to the conventional ADC, especially, at scaled CMOS technologies. While CMOS technology continues to scale down very fast, conventional ADCs are facing challenging obstacles concerning accuracy, resolution and power consumption. In particular, due to supply voltage reduction, the voltage domain is becoming noisier. In addition, the relatively high threshold voltage makes the available headroom very small for any sophisticated analog architectures [1]. These challenges make the conventional ADCs incapable of providing the high speed required to adopt them at the UWB receivers front-end.

On the positive side of scaling, with decreased rising and falling times, the switching characteristics of MOS transistors offer excellent timing accuracy at high frequencies. Consequently, the TADC appears as the best solution to achieve the front-end ADCs high speed requirements.

Fig. 1 represents the block diagram of the TADC which is mainly composed of two blocks. The first is a Voltage-to-Time Converter (VTC) while the second is a Time-to-Digital Converter (TDC). The idea is based on changing the voltage signal to the time domain through the VTC to make benefit of the high timing precision in the scaled down technologies, then the time represented signal is changed to the digital domain through the TDC. There is another advantage of dividing the design into two separate blocks (VTC and TDC). This advantage is that the two blocks can be physically isolated where the low power and low noise VTC can be paced near the antenna while the TDC can be placed away from the antenna. In this way we are not in need for a high gain from the receiver amplification stages after the antenna as the VTC is close to it. On the other hand, the noisy digital TDC will be away from the input signal at the antenna and receiver side. This approach is used with the Square Kilometre Array (SKA) [2]. In the following sections, the VTC will be introduced in details. Following that the TDC block will be proposed and finally, the simulation results will be presented.

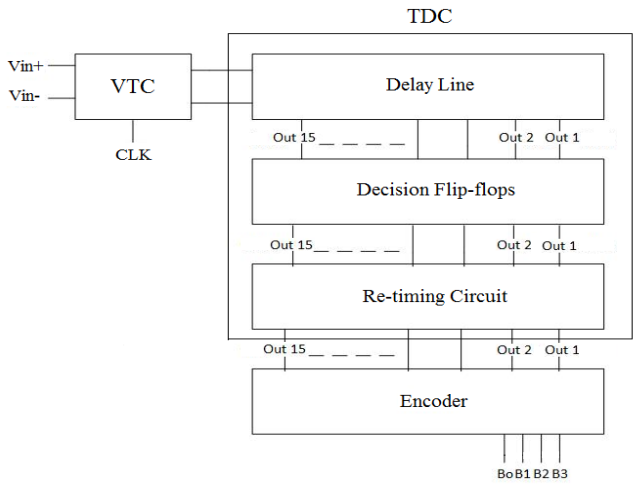

Fig. 1: TADC architecture.

II. VOLTAGE-TO-TIME CONVERTER

The VTC core circuit, shown in Fig. 2, converts the input analog signal into a corresponding pulse width that is proportional to the amplitude of the input voltage.

The VTC circuit consists of a basic inverter and a current starved inverter that controls the falling edges of the output signal. The current starved inverter (M1-M4) passes the falling edges of the signal V_{out} with a delay controlled with the input voltage.

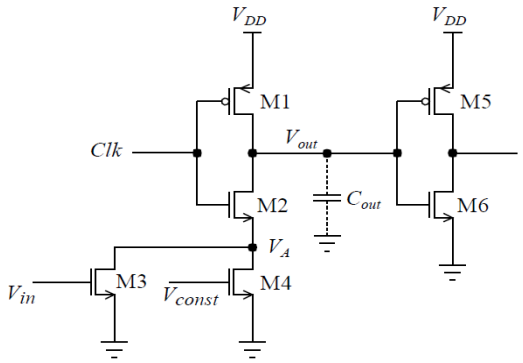

Fig. 2 The VTC core

At the rising edges of Clk, the transistors M3 and M4 are designed to enter the saturation region to make the discharging current of the capacitance (C_{out}) constant. The transistors M5 and M6 form an inverter which triggers when V_{out} reaches its threshold producing a delayed version of Clk with a controlled pulse delay.

This VTC architecture is capable of inherently sample the input signal. This inherited sample and hold function reduces the need to an external sample and hold circuit. That results in minimizing the total area and lowering power consumption.

To improve the dynamic range and the linearity of the VTC, this structure is duplicated to form the differential VTC, as shown in fig. 3, which eliminates the even harmonics from the VTC output signal.

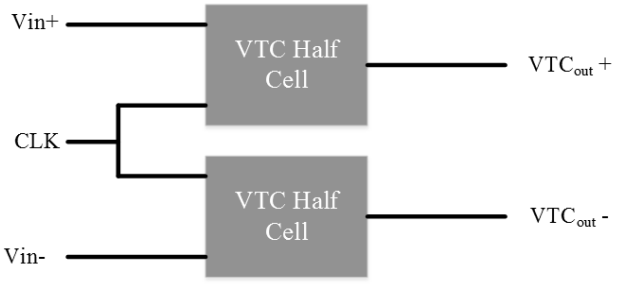

Fig. 3 The differential VTC

Fig. 4 shows the differential output delay after using two half cells to form the differential VTC.

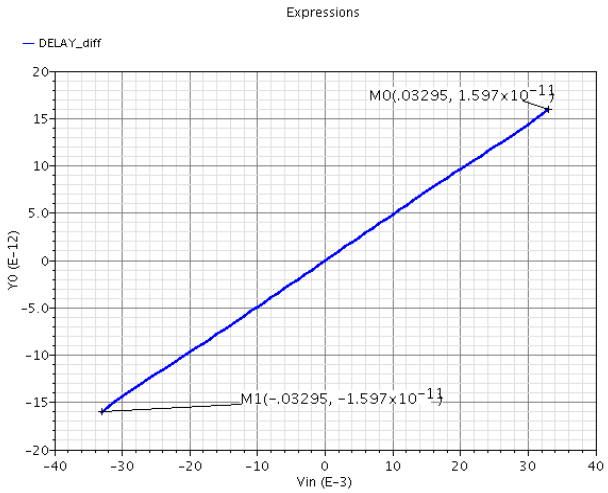

Fig. 4 The differential delay verses V_{in}

III. TIME-TO-DIGITAL CONVERTER

Generally, the TDC block is responsible for changing the time represented signals into digital codes. Depending on the location of the rising edges of the time modulated signals, it's required to output the corresponding digital codes.

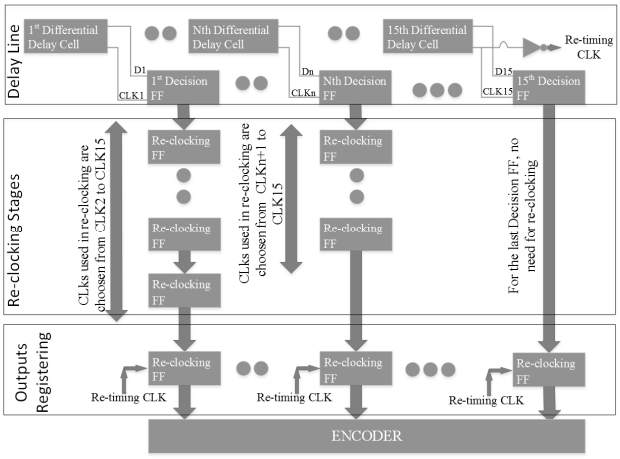

Fig. 5 Vernier Delay Line (VDL)

Fig. 5 shows the design of the proposed TDC. It's a 4-bit Vernier delay line (VDL) TDC. The TDC consists of 15 delay stages, each consisting of a tunable delay cell and a flip-flop. The first delay cell is designed to delay the negative input relative to the positive by 7tδ. All subsequent delays shift the inputs in the opposite direction; delaying the positive input relative to the negative input by 1 tδ. Consequently, the delay between the two signals sweeps through the range of -7tδ to +7tδ as the signals travel through the VDL.

After each delay, a flip-flop makes a decision on which input's rising edge occurs first, and stores the output. The flip-flop output will be '0' when its clock signal arrives before its input signal the output will be '1' when the data arrives before the clock. To achieve the correct output code, the flip flop is designed such that if the two signals are coincident on each other, the output is one.

The variable delays needed for the VDL are produced by the delay block shown in Fig. 6. The time delay of each delay cell is tuned using the two control signals V_{gp} and V_{gN}. The delay cell is mainly implemented using a normal inverter and a starved inverter. The basic CMOS inverter is formed from the 2 transistors M4 and M5 that are followed by another inverter formed from the transistors M7 and M8. The devices M3 and M6 control the amount of current passing through the inverter. Thus, the biasing voltages V_{gp} and V_{gN} are used to control the value of time delay in the rising and falling edges of the delay cell.

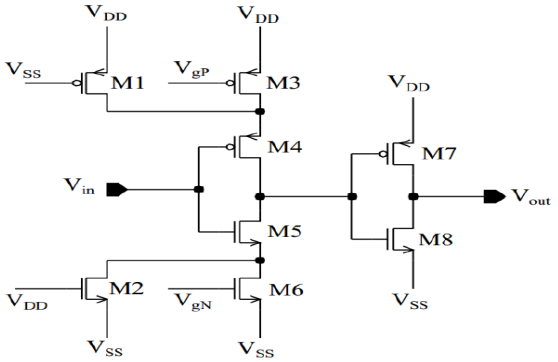

Fig. 6 The delay cell schematic

The transistors M1 and M2 are comparatively small as they have quarter the width of the remaining transistors; they are biased to ensure that a minimum amount of current is able to flow even if M3 and M6 enter the cut-off mode which is critical for automatic calibration of the ADC afterwards.

To achieve time resolution (tδ) that is smaller than the one restricted by the technology, two chains of delay cells can be used. One of these chains has a slightly higher delay than the other. As a result, the delay cell will be differentially ended. The slight difference between the two half circuit delay cells is the required time resolution tδ.

There aree three critical cases from the flip-flop point of view. The first case is when the two signals are coincident on each other; in this case the output is designed to be one. The second case is when the stop signal is preceding the start signal by tδ and here the required output is one. The last case is when the start signal is preceding the stop signal by tδ and the required output is zero. From the view of the flip-flop design, this is translated to the setup time, which is a tight restriction. The required performance was reached by the design in fig. 7.

According to the proposed Vernier delay line architecture, the output of the flip-flops will not be produced at the same time due to the delay introduced by each block. Consequently, they have to be synchronized before the encoder. One more important point is that each delay stage from the 15 delay stages produces a delay larger than tδ, i.e. the clock entering the 15th flip-flop is delayed by 15 delay stages more than the clock entering the first flip-flop. Thus, in total, the time delay

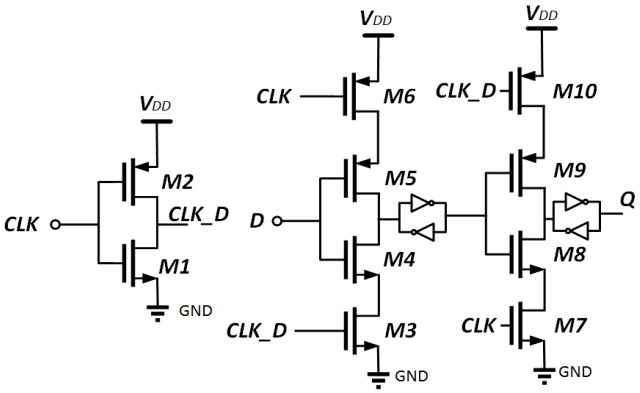

Fig. 7 The flip-flop general schematic

between the first and last flip-flop outputs exceeds the 6 GHz clock (period of ≈ 166ps), as a result, directly encoding these outputs would result in errors. We need the outputs of the decision flip flops to be ready together at the same time. Consequently, we want to save the outputs of the flip-flops, synchronize them together and at the same time receive new inputs. This is done by a pipelined re-clocking system.

As shown in fig. 5, the idea of pipelined re-clocking is based on adding a series of flip-flops after the decision flip-flop to save the output of the flip-flop in a pipelined form of successive series stages. The delayed versions of the clock in the VDL are used in these re-timing flip-flops as input clocks to them.

There are two conditions on the delay between the chosen delayed clock version and the output of the decision flip-flop to correctly decide the number of flip-flops:

1) The rising edge of the delayed clock version should be delayed enough so that the output of the flip-flop is ready.

2) The delay between the rising or falling edge of the decision flip-flop output and the re-clocking clock should be less than 165 ps (≈ 6 GHz).

The outputs of re-clocking stages which are entering the encoder are registered using the same clock and also all the outputs from the encoder are registered using one clock. This clock must make the outputs ready at a rate of 6GS/sec precisely. The falling edge of the most delayed clock version is used in the final stage of re-clocking as the falling edge is not pulse modulated in the VTC block.

After re-timing the decision flip-flops outputs, they are ready to be encoded. The VDL output consists of 15 bits forming 16 possible combinations. The final block in the TDC is the thermometer encoder which converts the 15-bit thermometer-coded output of the VDL to a 4-bit binary output. The encoder is a priority encoder in which the output bits depend on the position of the last '1' in the sequence

Using Karnaugh maps to directly map the thermometer-coded inputs to the binary outputs minimizes the amount of logic required. Using sum-of-product approach we can easily get the expression for each of the 4 outputs.

IV. Simulation Results

A prototype was designed and simulated successfully under the 65 nm technology. For the VTC block, a time delay span of 32 ps was reached which implies a TDC time resolution of 2 ps. This is equal to the VTC delay span (32 ps) divided by 2N where N = 4 bits. Also, a dynamic range of 130 mV peak-to-peak is achieved.

A. ADC Output Codes

Fig. 8 shows the characteristic curve of the TADC. The vertical axis is the quantized values of different input voltages.

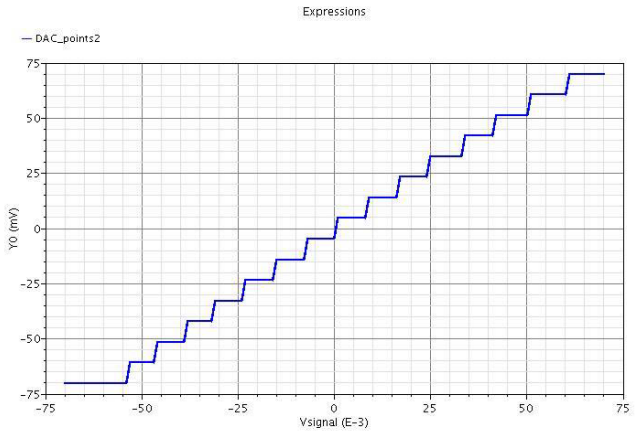

Fig. 8 Output codes VS input voltage

B. Effective Number of Bits ENOB

The ENOB was calculated at 3 different frequencies 600 MHz, 1331 MHz and 2666 MHz. The resultant ENOB is approximately 3.63, 3.68 and 3.72 respectively.

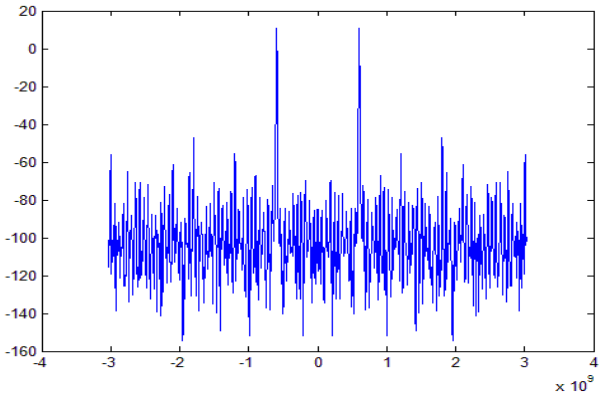

Fig. 9 The frequency domain of the output due to input frequency =600 MHz

Fig. 9 shows the frequency domain of the output due to input frequency 600 MHz. The ENOB in this case is equal to 3.63. The 3rd and 5th harmonics exist at frequencies 1800 MHz and 3000 MHz respectively. However, due to the differential structure, the 2nd and the 4th harmonics at frequencies 1200 MHz and 2400 MHz are within the range of the ordinary noise.

C. Performance Comparison

Table 1 shows the performance of the proposed TADC compared to other ADCs.

Point of Comparison	This work	[2]	[3]	[4]
CMOS Technology	65 nm	65 nm	90 nm	65 nm
Power Dissipation (mW)	21.4 mW	34.6 mW	12.1 mW	320 mW
Input Range (p-p)	130 mV (diff)	200 mV (diff)	100mV	N/A
Sampling Rate (GS/s)	6 GS/s	5 GS/s	2.5 GS/s	5 GS/s
Number of Bits	4 bits	4 bits	3 bits	6 bits

Table 1 Performance comparison of several ADCs

V. Conclusion

In this paper, we introduced a new TADC composed of a VTC and a TDC block which employs a different technique from the conventional ADC. The TADC quantizes time at predefined intervals. The main product of this work is a 4-bit, 6GS/s ADC. At an input frequency of 2666, 1331 and 600 MHz, the ENOB is approximately 3.72, 3.68 and 3.63 respectively. This TADC also introduces a new re-clocking technique that improves the whole performance.

VI. Acknowledgment

VII. This research was partially funded by Cairo University, Zewail City of Science and Technology, AUC, the STDF, Intel, Mentor Graphics, MCIT, Academy of Scientific Research and Technology (ASRT), and the Natural Sciences and Engineering Research Council of Canada (NSERC).

References

[1] Roberts, Gordon W., and Mohammad Ali-Bakhshian. "A brief introduction to time-to-digital and digital-to-time converters." *Circuits and Systems II: Express Briefs, IEEE Transactions on* 57.3 (2010): 153-157.

[2] Macpherson, Andrew R., James W. Haslett, and Leonid Belostotski. "A 5GS/s 4-bit time-based single-channel CMOS ADC for radio astronomy." *Custom Integrated Circuits Conference (CICC), 2013 IEEE*. IEEE, 2013.

[3] Macpherson, Andrew R., Kenneth A. Townsend, and James W. Haslett. "A 2.5 GS/s 3-bit time-based ADC in 90nm CMOS." *Circuits and Systems (ISCAS), 2011 IEEE International Symposium on*. IEEE, 2011.

[4] Choi, Michael, et al. "A 6-bit 5-GSample/s Nyquist A/D converter in 65nm CMOS." *VLSI Circuits, 2008 IEEE Symposium on*. IEEE, 2008.