A New Digital Locking MPPT Control for Ultra Low Power Energy Harvesting Systems

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***Abstract*—This paper presents a new control technique for maximum power delivery of solar energy harvesting systems. The new technique is based on studying the solar cell characteristics, then determining the trajectory of the maximum power across different lighting conditions. The study is based on connecting the solar cell to the power converter, and finding a relationship between the charge pump optimum frequency and the solar cell optimum voltage that delivers the maximum power of the solar cell. The goal of the control unit is to match this frequency-voltage relationship without sensing circuits and/or decision generation circuits. The solar model used maximally delivers $1.5mW$, the open circuit voltage is below $550mV$. The harvester should deliver a $1.2V$ supply voltage. The control unit consists of an 8-bit low power SAR analog-to-digital converter, exponential decoder and a digitally-controlled oscillator. The control unit power consumption is less than $120\mu W$. The power efficiency reaches 43.6% at $975\mu W$ available solar power. The technology used for simulations is Global Foundaries 65 nm CMOS.**

I. Introduction

Energy harvesting is considered a very hot topic in the power management. The applications of self-powered systems are getting larger everyday starting from wearable electronics passing through biomedical section. The applications are also expanding to environmental measurements, navigation and wireless sensor nodes. This research area dictates careful design of the harvester, since most of the available power at the transducer side has to be transferred to the load with minimum power loss. The goal of this paper is to provide a CMOS custom design of a solar energy harvester, since solar energy is the most dense power source among different energy transducers.

Solar energy harvesting techniques are based on maximum power point search of the photovoltaic cell. There are different algorithms for maintaining the cell at its maximum power capability. The most widely used techniques are the hill climbing technique [1] and perturb/observe technique. Both techniques exhibit the procedure in finding the maximum power. The idea is based on perturbing the frequency of the power converter, then a power reading is sampled. Another perturbation is done, and another power reading is also sampled. A comparison between the two samples is done, and a decision is taken to increase or decrease the frequency. This task is repeated forever as long as the harvester is powered on. The two techniques are different in the type of design. The hill climbing technique is implemented in full custom flow, whereas the perturb/observe technique is realized through FPGA flow or microcontrollers programming in the digital domain.

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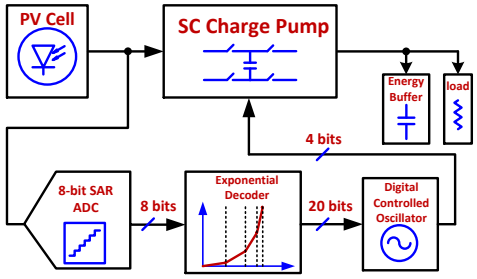

Fig. 1. The proposed block diagram of the energy harvester

This paper presents a new control technique based on the maximum power locking algorithm. Figure 1 shows the generic block diagram of the harvester. The solar cell is a compact verilog-A model [2]. The power converter is a 4-stage SC (switched capacitor) charge pump [3], each stage flying capacitor value is $500pF$. The idea is based monitoring the maximum power trajectory of the solar cell-power converter sub-system, then implements the trajectory using a mixed-signal control. The control unit is consists of three main blocks. An 8-bit analog-to-digital converter (ADC) is used to convert the solar cell voltage in to a digital word. Exponential decoder is used to decode the converted word into another coding format that takes the shape of an exponential behavior. A digital controlled oscillator is used to produce the required clock frequency needed by the charge pump to transfer the maximum power of the solar cell to the energy buffer side.

This paper is organized as follows; Section (II) presents the design of the important blocks in the system. Section (III) displays the system integration and the simulations results. Section (IV) shows the conclusion.

II. The Proposed Energy Harvester Design

In [1], the design is based on sensing the output current through a power hungry current sensor, then cascading with a decision generation circuit. This technique is consuming a lot of power in the control unit. In [4], the design is

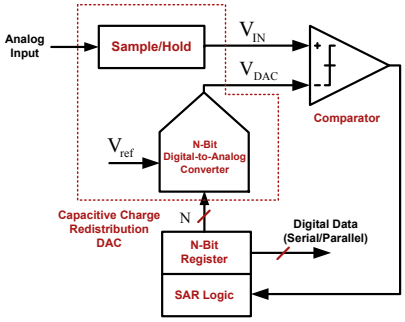

Fig. 2. Block diagram of the current sensor

based on understanding the solar cell characteristics. Th designer understands the solar cell behavior connected to th charge pump, a quadratic voltage controlled oscillator (VCC is designed to lock on the maximum power. This techniqu is poor in terms of dynamic range of the solar cell voltag accordingly it will not track efficiently across wide range c input light. In [5], an extended study of [4] has been hel the solar cell with the charge pump characteristics is derive mathematically. A compact relationship between solar ce voltage and charge pump frequency is reached. the realizatio of this relation dictates an exponential behavior between frequency and voltage. A sub-threshold VCO is designed to match the relationship. The design is very efficient in terms of power, but poor in terms of process corners since sub-threshold operation carries a lot of variations. The proposed design is based on [5], however the realization is done in digital domain rather than the custom one.

A. Analog-to-Digital Converter Design

Successive-approximation-register (SAR) analog-to-digital converters (ADCs) represent a popular ADC solution. ADCs typically provide medium-to-high-resolution, with a speed reaching 5MS/s, and a resolution ranging from 8 to 16 bits. More importantly, the SAR ADCs are capable of providing high-performance using a small amount of power, which is a prerequisite for energy harvesting systems.

The SAR ADC essentially employs a binary search algorithm. The basic architecture for the SAR ADC system is shown in Fig. 2. First, the analog input signal is sampled in the $Sample/Hold$ stage, producing a signal V_{IN}. The sample rate is a fraction of the universal clock, and depends on the resolution of SAR. V_{IN} is then held by the $Sample/Hold$ stage until the evaluation stage is finished. In the evaluation stage, the $N-Bit\ Register$ initially sets the most significant bit (MSB) to "1" (e.g., for 8-bit conversion, the n-bit register output would be "10000000"). This prompts the $N-Bit\ DAC$ to output a voltage equal to half its reference voltage ($V_{REF}/2$). After this, the DAC output (V_{DAC}) and the held input signal (V_{IN}) are evaluated by the comparator. Based on the output of the comparator, the $SAR\ Logic$ sets the output of the $N-Bit\ Register$ with purpose of making the value of V_{DAC} closer to that of V_{IN}.

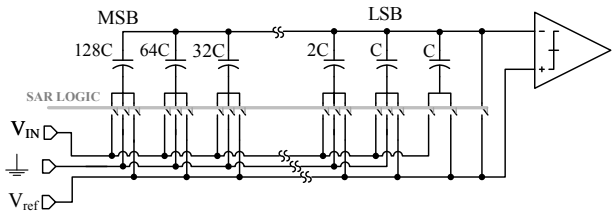

Fig. 3. Charge Redistribution Capacitive DAC architecture

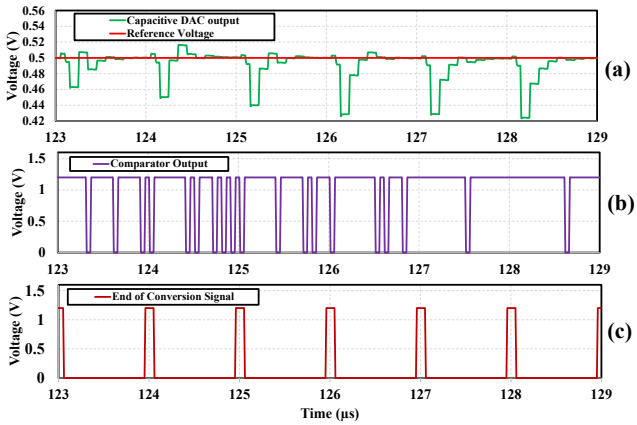

Fig. 4. Important Signals of the SAR ADC. (a)Reference Voltage, Capacitive DAC during sampling/evaluation. (b)Comparator output decision. (c)End of conversion signal

In this work, an 8-bit SAR ADC is used. The SAR system features a capacitive DAC, as shown in Fig. 3. An advantage of the capacitive DAC is that it provides an inherent track/hold function. The idea is to use weighted capacitors to describe different bits; the largest capacitor produces the largest current, and therefore corresponds to the MSB; similarly, the smallest capacitor corresponds to the LSB. Figure 4 shows the important signals of the SAR ADC, The signals shows that sampling/evaluation operation is going well for an input voltage range of $150mV$. Accordingly, the ground reference is set to $350mV$ and main reference is set to $500mV$, this is in order to guarantee a higher voltage multiplication than the energy buffer voltage ($1.2V$). Figure 5 shows the analog conversion test of the sampled data, the input analog frequency

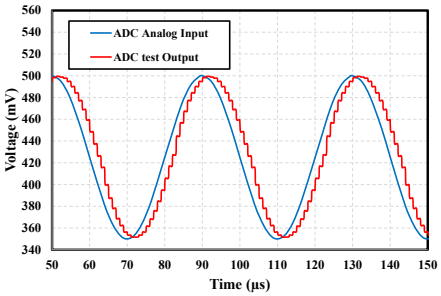

Fig. 5. ADC Test conversion of the N-bit register for an analog input sin wave

is $25KHz$ and the SAR ADC clock frequency is $10MHz$. The SAR logic control is implemented using synthesized verilog coding.

B. Exponential Decoder

Based on [3], the relationship between charge pump optimum frequency locking and the solar cell voltage has an exponential nature. The exponential relation is linearized by dividing the allowed range of V_{MPP} into different intervals were each interval has a certain slope. The following equation was used to develop a programmable MPPT controller such that the exponential behavior can be easily adjusted by changing the slopes and the size of each interval. $X0, X1, X2$ and $X3$ are used to define the start and end of each interval. The transfer function is shown in Equation(1). The input/output values are the digital equivalent of these equations.

$$F = 1(V_{in} - X_0) + 2(V_{in} - X_1) + 4(V_{in} - X_2) + 8(V_{in} - X_3) \quad (1)$$

$$\begin{aligned}(V_{in} - X_0) : 0 \rightarrow (X_1 - X_0)\\ (V_{in} - X_1) : 0 \rightarrow (X_2 - X_1)\\ (V_{in} - X_2) : 0 \rightarrow (X_3 - X_2)\\ (V_{in} - X_2) : 0 \rightarrow (X_4 - X_3)\end{aligned}$$

The function is implemented using verliog and synthesized on synopsys in order to evaluate the implementation area and power consumption. The arithmetic operations needed are addition, subtraction, and multiplication. Thus, adders, subtractors and hardwired shifters are used to realize the function. The hardwired shifters are used to replace the multipliers in order to reduce the area and power consumption. However, the multiplication can be replaced by n-bit shifting only if the multiplication constant is in the form of (2^n). Furthermore, the terms $(V_{in} - X_0), (V_{in} - X_1), (V_{in} - X_2)$ and $(V_{in} - X_3)$ are limited between zero and the size of the intervals as illustrated in the equation. Accordingly, comparators are used to identify the interval where V_{in} is located, then the multiplexers will select the appropriate result for each term. Finally, the output of the exponential function is clamped to 255 which is the value of X_4. This value is set by the number of bits needed for driving the digital controlled oscillator. Figure 6 shows the concept of the exponential decoder.

C. Digitally Controlled Oscillator

The DCO is the block used to generate the switching frequency fed to the power converter. The DCO theory of operation is based on a controllable ring oscillator, the frequency of which is controlled by both a capacitor bank for coarse tuning, and a thermometer weighted transistor banks for fine tuning. Based on the 8-bit code received from the exponential decoder the right capacitors and transistors are connected to the ring oscillator in order to generate the required frequency.

Figure 7 shows the block diagram of the DCO. five cascaded stages are used to reach a frequency range up to $10MHz$.

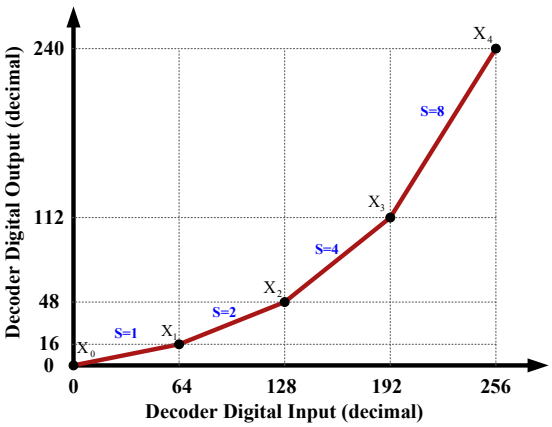

Fig. 6. Representation of the transfer function needed by the exponential decoder

The coarse tuning is done by four binary-weighted capacitors, the unit cap is equal to $0.47pF$. The fine tuning is based on driving strength transistors, the least 4 bits of the exponential decoder is translated into thermometer decoding for increasing the linearity. Figure 8 shows the detailed circuit design.

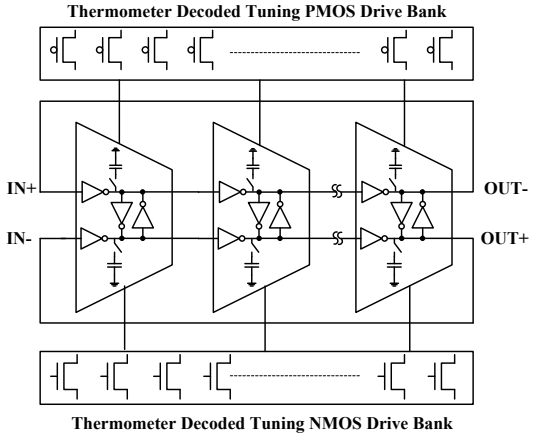

Fig. 7. Block diagram of the digital controlled oscillator

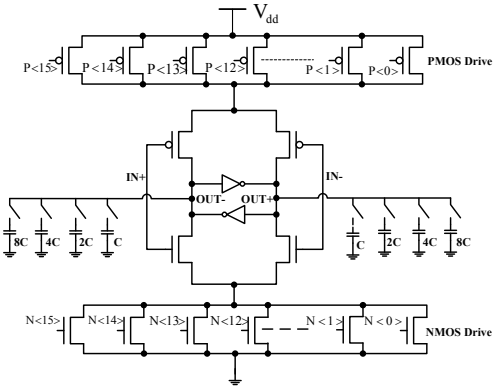

Fig. 8. Circuit design of one stage showing the tuning mechanism

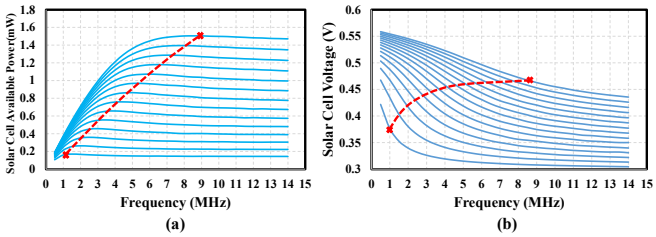

Fig. 9. Solar cell/Charge pump test simulations. (a) Solar cell power (b) Solar cell voltage ($LUX Range : 204.6 \rightarrow 1376.4$)

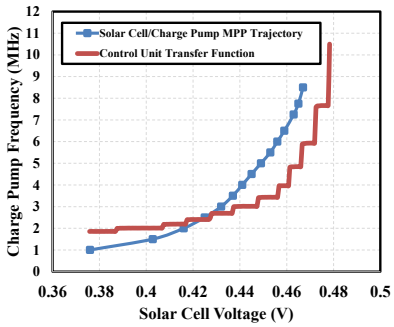

Fig. 10. Control unit V-F transfer function versus V-F trajectory of the maximum power

III. Simulation Results of The Proposed Design

First, the characteristics of the solar cell should be addressed. Figure 9(a) shows the solar cell power versus charge pump frequency under light range ($204.6LUX \rightarrow 1376.4LUX$). This simulation is done for the solar cell connected to the charge pump with a test input frequency, it can be shown that the red line represents the trajectory of the maximum power. Figure 9(b) shows the solar cell voltage versus charge pump frequency for the same light range, the maximum power trajectory is mapped to this simulation as it is going to be mapped by the control unit.

Figure 10 shows open loop simulation of both loop paths. The first curve is the solar cell maximum power trajectory needed to be tracked. The second curve shows voltage/frequency transfer function of the control unit. Based on [5], once upon closing the loop, the system should be able to track the maximum power.

Figure 11 shows the closed loop simulations for different light conditions. It can be shown that for each input light, the solar cell voltage starts at the open circuit voltage. Afterwards the feedback starts to change the frequency, then the frequency affects the voltage again. This operation is repeated several times until the feedback locks to the maximum power available at a given input light.

Table I shows the performance metrics of the harvester at different light conditions.

IV. Conclusion

A new digital maximum power locking control is addressed in this work. The idea is based on [5], where the solar

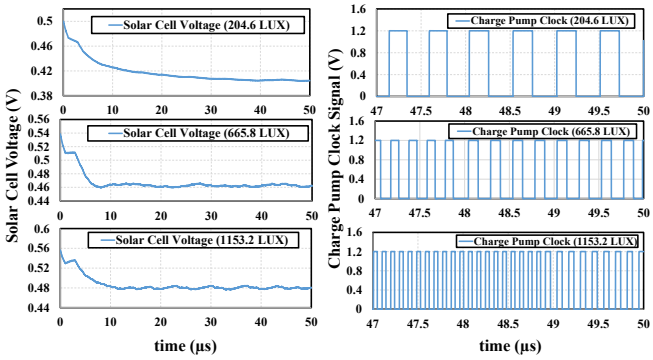

Fig. 11. Closed loop simulation results for different light conditions

TABLE I
Performance Metrics of the Energy Harvester

light	204.6 LUX	430.6 LUX	665.8 LUX	906.7 LUX	1153.2 LUX	1376.4 LUX
Solar cell power (μW)	220	463	716	975	1240	1480
Energy buffer power (μW)	47.3	180	312	425	513	605
Power Efficiency (%)	21.5	38.8	43.6	43.6	41.3	40.8
Consumed power (μW)	87.8	89.6	92	94.5	99.6	102
Charge Pump Frequency (average) (MHz)	2.14	3.07	4.38	6	9.34	10.6
Solar cell voltage (average) (mV)	405	447	462	473	479	495

cell characteristics is well understood. The control unit is designed to match the maximum power trajectory. The design of each block is highlighted. Open loop simulations are done to understand the system. Closed loop simulations are done to verify the system locking mechanism.

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