A CMOS BASED OPERATIONAL FLOATING CURRENT CONVEYOR

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***Abstract*—This paper presents a novel integrated CMOS based the operational floating current conveyor (OFCC). OFCC is a five port general purpose analog building block. The supply voltage of the proposed OFCC is 1.2V and it provides a wide bandwidth. The circuit is modeled and simulated using UMC 130nm technology kit in Cadence.**

Keywords-component; integrated, operational floating current conveyor; analog circuits; current mode device

I. INTRODUCTION

The analog signal processing circuit can be divided into two modes either voltage mode or current mode. Voltage mode circuits have the disadvantage that the gain-bandwidth product is constant. This drawback will reduce the bandwidth of the amplifier [1]. Many trials have been made to solve the limitation of the gain dependent bandwidth so this led to using current mode devices as active elements at the circuits that work at high frequencies.

There are many merits of the current mode circuits compared to the voltage mode ones; the slew rate is higher, the bandwidth is wider & the bandwidth is constant at different gains [2].

The first invented current mode device was the first generation current conveyor (CCI). The input current at the input terminal X is transferred to the output terminal Z (current tracking action) and at the same time there is a voltage following action between the two input ports Y and X, as appeared in Figure 1 [3]. The first two applications using the CCI as a primary block were wideband current measuring device and a negative impedance converter (NIC) [4].

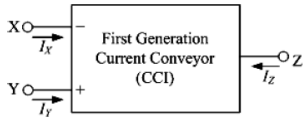

Figure 1: CCI block diagram [3]

The second-generation current conveyor (CCII) was then presented after the CCI achieved a great success. It has two models: the first one is the positive second generation current conveyor CCII+ which the current is copied with the same phase and magnitude from a low output impedance node to a high output impedance node. The second one is the negative second generation current conveyor CCII- in which the current is copied with the same magnitude but out of phase from low impedance to a high impedance node as shown in figure 2 [2].

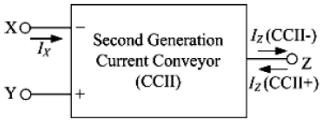

Figure 2: CCII block diagram [5]

David Nelson was the first one to design the current feedback amplifier (CFA) based on the CCII+.It was designed by using the same topology as a CCII followed by a buffer, as shown in figure 3 [6-8].

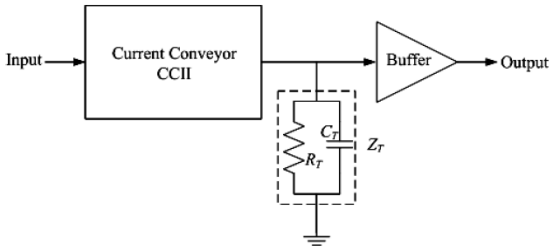

Figure 3: CFA block diagram [6]

As the CCII used to be a part of the current-feedback amplifier circuit construction; the CFA was also used as a part the operational floating conveyor OFC that was introduced by Toumazou, Payne, and Lidgey as shown in figure 4 [9].

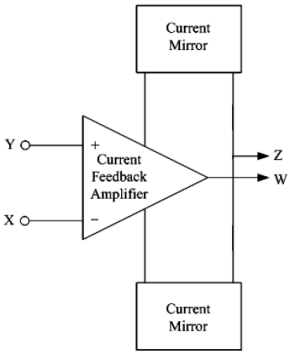

Figure 4: Block diagram of OFC [9]

Khan was the first one to design the OFCC circuit using discrete elements based on discrete BJTs and a commercial current-feedback amplifier (AD846) [10]. "Then Ghallab started using the same OFCC circuit in many applications such as a current-mode Wheatstone bridge, instrumentation amplifier, universal filter, and readout circuit for biomedical sensors and Lab-On-a-Chip (LOC) systems" [11,12].

The remaining part of this paper is arranged as follows: Section II revises the basic concept of the OFCC and its characteristics. Section III discusses the analysis of the proposed CMOS based OFCC. Section IV shows the simulation results and discussion. Section V presents an application based on OFCC. Section VI concludes the paper and presents the benefits of the proposed OFCC.

II. OFCC CIRCUIT

Figure 5 shows the OFCC has two input terminals Y & X and has three output terminals W, Z+ and Z-.

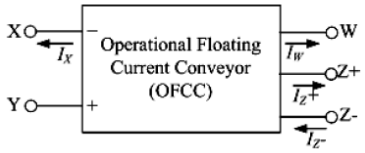

Figure 5: OFCC block diagram

X: low-impedance input current
Y: high-impedance input voltage
W: low-impedance output voltage
Z+ and Z-: high-impedance output currents with opposite polarities.

The ideal operation of the OFCC circuit can be expressed as follows:

$$\begin{bmatrix} i_y \\ v_x \\ v_w \\ i_{z+} \\ i_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & -Z_T & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ i_w \\ v_{z+} \\ v_{z-} \end{bmatrix} \quad (1)$$

There is a voltage following action between the two input terminals (V_X=V_Y) as shown in eq. (1). Also, there is a current tracking action between the OFCC output terminals W and Z. Moreover, the input current of the low input impedance terminal of the OFCC (i_X) is multiplied by the total transimpedance of the OFCC circuit (Z_T) to produce the output voltage V_W.

III. THE PROPOSED CMOS OFCC CIRCUIT

The proposed OFFC is implemented using two CCII+ [14] blocks, one noninverting transimpedance amplifier and a current steering circuit. To do the voltage folllowing at the input terminals Y and X the first CCII+ (M1- M7) is used. In addition, to do the current tracking action at the output terminals W and Z the second CCII+ (M14-M20) is used. The input current at terminal X is multiplied by the transimpedance amplifier gain (M8- M13) to generate the output voltage at terminal W. The current steering circuit (M21-M24) is used to alter the phase of the mirrored current by 180°. The steered current is mirrored by transistors M25 and M26 to produce I_{Z-}.

Figure 6 shows the proposed integrated CMOS based OFCC circuit. The following transistors are matched M1 and M2. In addition to M3, M4, M11 and M12 are matched. Also, M5, M7, M10 and M18 are matched in addition to M6, M8 and M19, M9 and M13, M16 and M17. Finally, M22, M23 and M24 are matched.

The voltage transfer gain from the terminal Y to terminal X [13]:

$$A_v = \frac{v_x}{v_y} = \frac{g_{m1}}{g_{m1} + g_{d1} + \dfrac{g_{d3}(g_{d1} + 2g_{d5})}{(g_{d5} + g_{m3})}} \quad (2)$$

g_m: the transistor transconductance
g_d: drain to source conductance
The input resistance seen at terminal X [13]:

$$r_x = \frac{(g_{d1} + 2g_{d5})}{(g_{m1} + g_{d1})(g_{m3} + g_{d5}) + g_{d3}(g_{d1} + 2g_{d5})} \quad (3)$$

The open loop transimpedance gain Z_t is expressed as [13]:

$$Z_t = \frac{g_{m12}g_{m13}g_{m14}}{(g_{d4} + g_{d7})(g_{d12} + g_{d10})(g_{m11} + g_{d13})\left(g_{m14} + g_{d14} + \dfrac{g_{d16}(g_{d14} + 2g_{d18})}{(g_{d18} + g_{m16})}\right)} \quad (4)$$

The output resistance seen at terminal Z [13]:

$$r_z = \frac{1}{g_{d17} + g_{d20}} \quad (5)$$

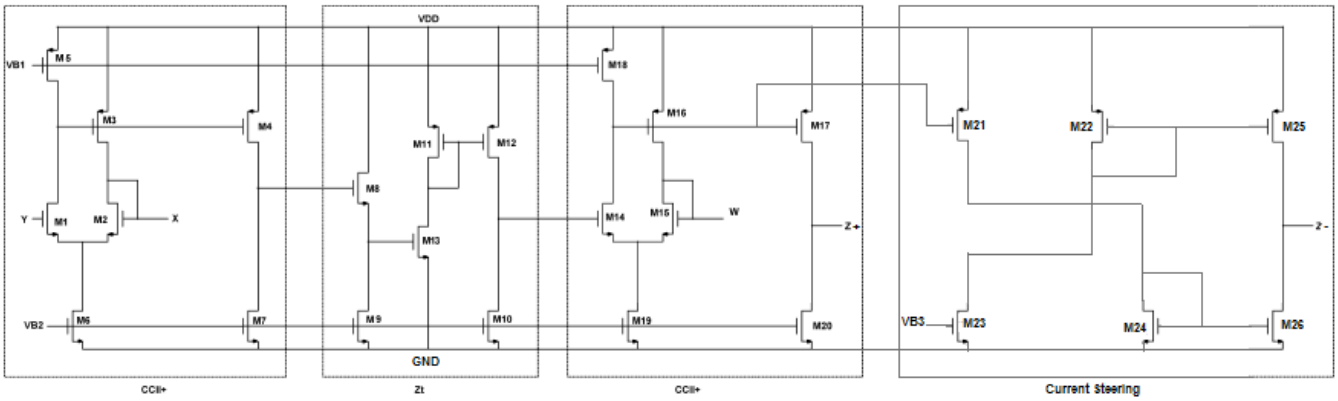

Figure 6: Schematic of the proposed OFCC circuit

IV. SIMULATION RESULTS & DISCUSION

The circuit is modeled and simulated using UMC 130nm technology kit in Cadence. The DC power supply used is 1.2 Volt.

The total DC power consumption of the OFCC circuit is 1.5mW. The input voltage tracking is shown in figure 7 with an error 0.4%. Figure 8 shows the open loop transimpedance gain between X and W (V_w/I_x). Figure 9 & figure 10 show the outputs current tracking I_{z+}/I_w with an error 0.5% and I_{z-}/I_w with an error 0.8%.

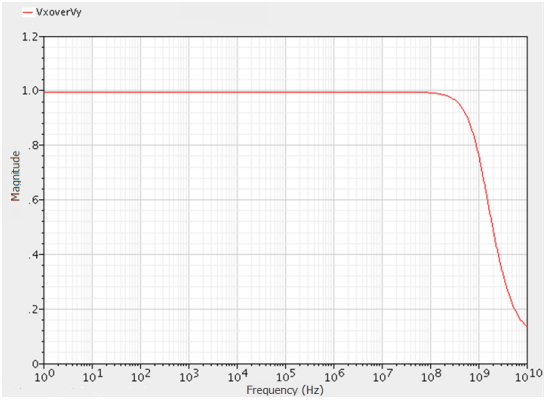

Figure 7: Input terminals voltage tracking V_x/V_y

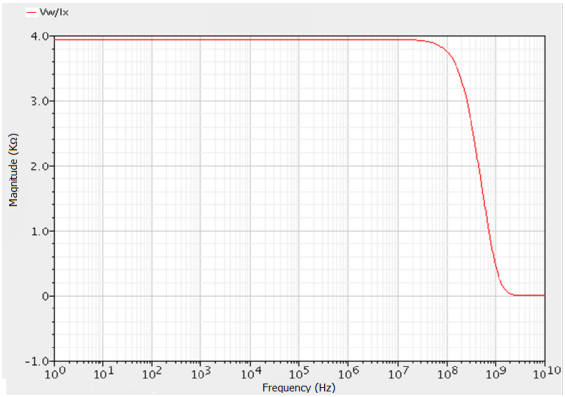

Figure 8: Open loop transimpedance gain

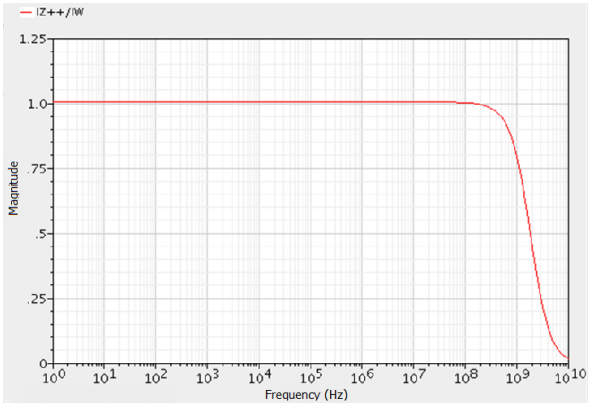

Figure 9: Output terminals current tracking Iz+/Iw

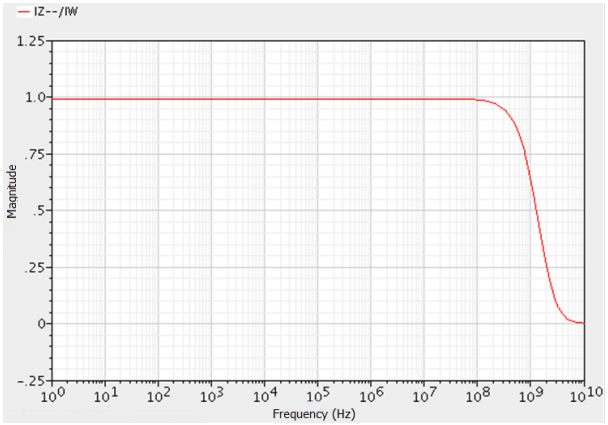

Figure 10: Output terminals current tracking Iz-/Iw

Table 1 shows a comparison in performance between the currently used and the proposed OFCC and OFC.

Table 1: Comaprison between the proposed and other OFCC & OFC circuits

OFC & OFCC Reference	Proposed	[2]	[12]
Technology	130nm	90nm	500nm
Supply	+1.2 V	+1.2 V	±1.5 V
Input voltage dynamic range (V)	500m to 900m	0 to 800m	-0.4 to 1.2
Input resistance r_x (Ω)	8.83	20	30.2
-3dB frequency (Bandwidth)	1.2GHz	30MHz	826MHz
DC open loop transimpedance gain (kΩ)	3.94	3	29.6
Power Consumption (mW)	1.5	1.1	2.4

The proposed design of the CMOS based OFCC circuit has the lowest internal resistance which is equal to 8.83Ω compared to the other two designs. Also the proposed design has the highest 3dB frequency (bandwidth) which increased by 97.5% and 30.2% compared to others [2][13], respectively. [13] shows the highest DC open loop transimpedance gain which is OFC circuit. The proposed design is higher than the OFCC circuit presented in [2]. The power consumption in the proposed design is equal to 1.5mW which is higher than [2] by 0.4mW. However, OFCC presented in [2] is designed based on 90nm CMOS technology. The proposed design has a lower power consumption compared to [13] by about 0.9mW.

V. APPLICATION BASED ON OFCC

OFCC is a flexible analog device as there is floatation in its input and output terminals. It is implemented to be utilized in a closed loop circuits with a feedback current from terminal W to terminal X. Inverting voltage amplifier, non-inverting voltage amplifier, transresistance amplifier and transconductance amplifier are examples of applications that can be designed in a closed loop.

Figure 11 shows non inverting voltage amplifier using OFCC.

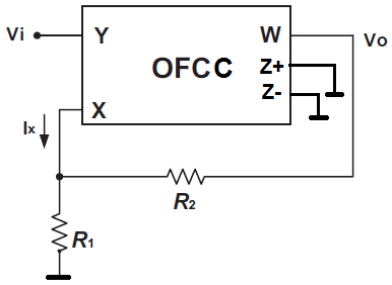

Figure 11: Non-inverting voltage amplifier

$$\text{Voltage gain } (A_v) = \frac{V_o}{V_i} = 1 + \frac{R_2}{R_1} \quad (6)$$

The non-inverting voltage amplifier is simulated using R_1=10kΩ, R_2=5kΩ and is shown in figure 12. The voltage gain is equal to 1.508 with an error 0.008. The bandwidth is greater than 100MHz.

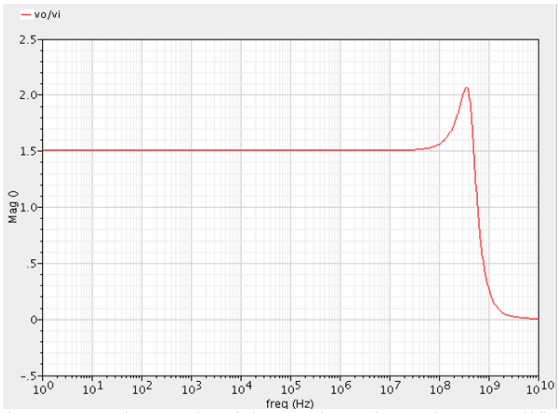

Figure 12: Voltage gain of the non-inverting voltage amplifier

VI. CONCLUSION

An integrated CMOS based OFCC has been modeled and simulated. The circuit architecture uses a low-drive CCII+ as a first gain stage, a transconductance amplifier as second gain stage, and a high-drive CCII+ & a current steering circuit as output stages. The simulation results shows that the proposed OFCC has the following advantage: it offers wide bandwidth with suitable power consumption.

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