A CMOS BASED OPERATIONAL FLOATING CURRENT CONVEYOR AND ITS APPLICATIONS

Nermine M. Edward[1,2], Yehya H. Ghallab[2,3], Hassan Mostafa[2,4], Yehea I. Ismail[1,2]

[1] *Department of Electronics and Communications Engineering, The American University in Cairo, Egypt*
[2] Center of Nanoelectronics and Devices (CND) at Zewail City of Science and Technology/AUC, Cairo, Egypt
[3] Biomedical Engineering Department, Helwan University, Cairo, Egypt
[4] *Department of Electronics and Communications Engineering, Cairo University, Giza, Egypt*
n.maher, hmoustafa, y.ismail@aucegypt.edu, yghallab@zewailcity.edu.eg

***Abstract*—This paper provides a novel integrated CMOS based operational floating current conveyor (OFCC) and its applications. The supply voltage of the intended OFCC is 1.2V and it will have a wide bandwidth.**

Keywords-component; integrated, operational floating current conveyor; analog circuits; current mode device

I. INTRODUCTION

The analog signal processing circuit can be divided using two modes either voltage mode or current mode. From the disadvantages of voltage mode circuits that the gain-bandwidth product is constant which minimizes the bandwidth of the amplifier [1]. Trials have been made to solve the drawbacks that resulted from the gain dependent bandwidth so this led to using current mode devices as active elements at the circuits that work at high frequencies.

"There are many advantages of the current mode circuits compared to the voltage mode ones; they have higher slew rate, wider bandwidth & constant bandwidth at different gains" [2].

Khan was the first one to propose the OFCC circuit utilizing discrete elements based on discrete BJTs and a commercial current-feedback amplifier (AD846) [3].

The remaining sections of this paper are arranged as follows: Section II revises the basic concept of the OFCC and its characteristics. The proposed CMOS based OFCC is presented in section III. Section IV presents applications based on OFCC. Section V is the future work.

II. OFCC CIRCUIT

The OFCC has two input terminals Y &X and has three output terminals Z-, Z+ and W as shown in figure 1.

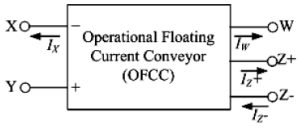

Figure 1: Block Diagram of OFCC

X: low-impedance input current
Y: high-impedance input voltage
W: low-impedance output voltage
Z+ and Z- : high-impedance output currents with opposite polarities.

The ideal operation of the OFCC circuit can be expressed as follows:

$$\begin{bmatrix} i_y \\ v_x \\ v_w \\ i_{z+} \\ i_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & -Z_T & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ i_w \\ v_{z+} \\ v_{z-} \end{bmatrix} \quad (1)$$

There is a voltage following action between the OFCC input terminals (V_X=V_Y) as shown in eq. (1). Also, there is a current following action between the OFCC output terminals W and Z. Moreover, the low impedance input current of the input terminal of the OFCC (i_X) is multiplied by the total transimpedance of the OFCC circuit (Z_T) to generate the output voltage V_W.

III. THE PROPOSED CMOS OFCC CIRCUIT

The proposed OFFC is implemented using two CCII+ [4] blocks, one noninverting transimpedance amplifier and a current steering circuit. To do the voltage following at the input terminals X and Y, the first CCII+ (M1- M7) is used. In addition, to do the current tracking action at the output terminals W and Z, the second CCII+ (M14-M20) is used. The input current at terminal X is multiplied by the transimpedance amplifier gain (M8- M13) to produce the output voltage at terminal W. The current steering circuit (M21-M24) is used to alter the phase of the mirrored current by 180°. The steered current is mirrored by transistors M25 and M26 to produce I_{Z-}.

The voltage transfer gain from the Y terminal to the X terminal [5]:

$$A_v = \frac{v_x}{v_y} = \frac{g_{m1}}{g_{m1} + g_{d1} + \dfrac{g_{d3}(g_{d1} + 2g_{d5})}{(g_{d5} + g_{m3})}} \quad (2)$$

g_m: the transistor transconductance
g_d: drain to source conductance

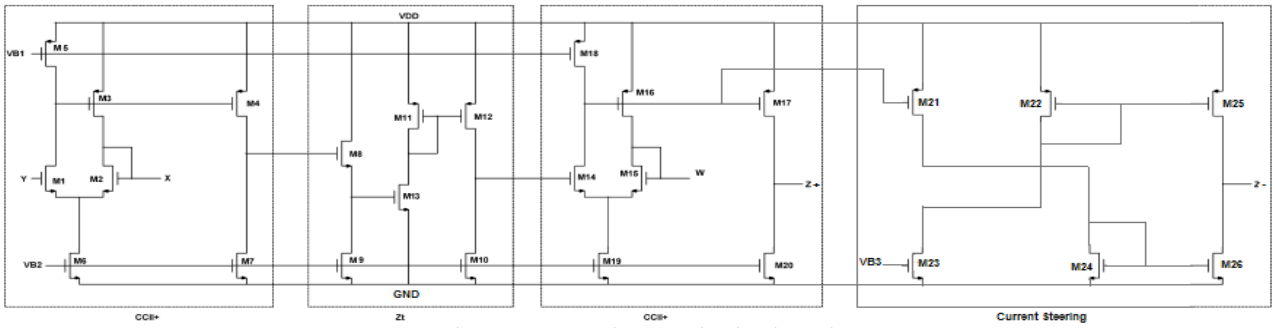

Figure 2: Proposed OFCC circuit schematic

The input resistance seen at terminal X [5]:

$$r_x = \frac{(g_{d1} + 2g_{d5})}{(g_{m1} + g_{d1})(g_{m3} + g_{d5}) + g_{d3}(g_{d1} + 2g_{d5})} \quad (3)$$

The open loop transimpedance gain Z_t [5]:

$$Z_t = \frac{g_{m12}g_{m13}g_{m14}}{(g_{d4} + g_{d7})(g_{d12} + g_{d10})(g_{m11} + g_{d13})\left(g_{m14} + g_{d14} + \frac{g_{d16}(g_{d14} + 2g_{d18})}{(g_{d18} + g_{m16})}\right)} \quad (4)$$

The output resistance at terminal Z [5]:

$$r_z = \frac{1}{g_{d17} + g_{d20}} \quad (5)$$

IV. Applications Based on OFCC

OFCC is a flexible analog device as there is floatation in its input and output terminals. It is implemented to be utilized in a closed loop circuits with a feedback current from terminal W to terminal X. Inverting voltage amplifier, non-inverting voltage amplifier, transconductance amplifier, transresistance amplifier, and current-mode instrumentation amplifier (CMIA) are examples of applications that can be designed in a closed loop.

Figure 3 shows the first application which is non-inverting voltage amplifier.

$$\text{Voltage gain } (A_v) = \frac{V_o}{V_i} = 1 + \frac{R_2}{R_1} \quad (6)$$

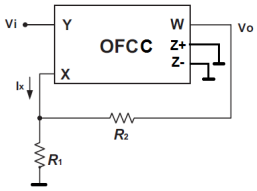

Figure 3: Non-inverting voltage amplifier using OFCC

The second application is CMIA which is shown in figure 4.

The output differential gain is given by [6]:

$$A_d(s) = \frac{v_o}{v_{in1} - v_{in2}} = \frac{2R_L}{R_G(1 + sC_ZR_L)} \quad (7)$$

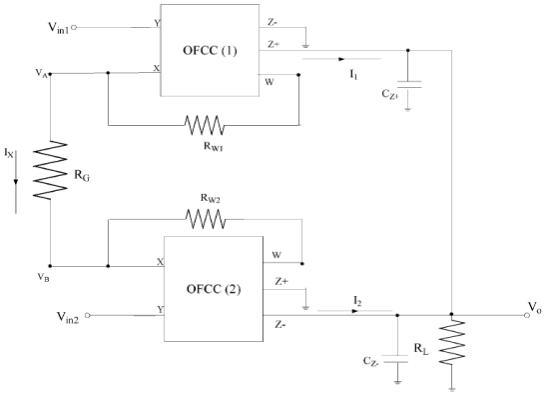

Figure 4: Proposed CMIA circuit

V. Future Work

An integrated CMOS based OFCC has been proposed. Design applications based on OFCC as non-inverting voltage amplifier and CMIA and do a comparison in performance between the currently used applications and the proposed one in terms of their bandwidth and input noise voltage.

Acknowledgement

This research was partially funded by Zewail City of Science and Technology, AUC, Cairo University, NTRA, ITIDA, SRC, ASRT, the STDF, Intel, Mentor Graphics, and MCIT.

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