Design Considerations/Insights for Memristor-Based Memory Arrays

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Abstract—To achieve high data density with low power consumption, technology migration into nano and molecular scales have been proposed. Discovery of the memristor has enabled the realization of denser nano-scale logic and memory systems. This is due to the memristor distinctive characteristics such as storing the historic state of the current passing through it, nano-scale device, and low power consumption. This work describes the design considerations of using a memristor in realization of a memory cell. Based on this analysis, a new read/write circuit is proposed and verified using a simulation tool.

Index Terms—Memristor, HP Memristor, Design considerations, Memristor-Based Memory

I. INTRODUCTION

For technology migration into the nano and molecular scales, several hybrid CMOS/nano logic and memory architectures have been recently introduced. Each of those architectures aims to achieve high device density with low power consumption. Different methodologies to displace or extend the existing CMOS technology have shed highly dense systems with low power consumption and minimum performance degradation. The announce of inventing memristors in [1] has expanded the prospect of nano-scale architectures to carry out the non-conventional logic and to increase the memory/logic density.

Previous researches in nano-scale memory design predominantly concentrate on crossbar based architectures given their regularity in structure, which makes it easier to be fabricated [2], [3]. The concerning with memory crossbar structure to make denser devices per array is due to the technology lack in CMOS technology fabrication in nano-scale. There is different array structure introduced for this purpose like crossbar array, one diode one transistor (1D1T) array, folded and un-folded crossbar architecture. These arrays consist of two sets of parallel wires crossing orthogonal to each other, with a memory device at each junction. The main difference between those structures is word to bit line ratio, how it deals with leakage current, and noise margin (NM) capabilities.

The recently found Memristor is a potential candidate for the next-generation memory because of its nano-scale and non-volatile advantages. Memristor has been recognized as the first practical implementation of the missing fourth circuit element predicted by L. Chua in 1971 [4]. In 2008, R. S. Williams introduced a two-terminal Titanium dioxide (TiO₂) nano-scale device that follows the memristive characteristics defined by L. Chua in 1971 [1]. It is stated by S. Williams that Memristors can potentially replace the CMOS transistors in future computers while occupying less chip area, consuming less power, and providing better performance [5].

Figures 1.a and 1.b show the physical structure of a Memristor device and its equivalent circuit model respectively. The device is composed of a TiO₂ thin film of length D, sandwiched between two metal contacts. There are two layers in the TiO₂ film. One layer is highly resistive TiO₂ (un-doped layer), and the other layer is filled with oxygen vacancies, which makes it highly conductive (doped layer). The state variable, w, represents the width of the doped region.

Figure 1.c displays the Memristor symbol. The orientation of the symbol follows the equivalent circuit in 1.b, where \(R_{\text{on}}\) is at the left and \(R_{\text{off}}\) is at the right. Memristor-based memories exhibit higher storage density than hard drives with access times close to those of SRAM memories. It has been declared that Memristor devices can be scaled down beyond 10nm and can achieve data storage density close to 100 Gbits/cm, which is higher than current advanced flash memory technologies [6], [7].

In this paper, design considerations on using memristor as a memory element are proposed based on device characteristics and analysis. The rest of the paper is organized as follows: Section II introduces a brief description and analysis of metal oxide memristor devices that have been invented by HP labs. Section III verifies this analysis using Cadence Spectre simulation tool, and finally some conclusions are drawn in Section IV.

II. MEMRISTOR-BASED MEMORY ELEMENT

At May 2008 HP labs announce the first physical realization of the memristor [1]. Memristor is proposed as a two terminal
device whose resistance depends on the magnitude, polarity, and the pulse width of the applied voltage.

It is fabricated as a cube of Titanium dioxide (TiO$_2$) with 3-30 nanometer thickness ($D$) sandwiched between two platinum electrodes. The Titanium dioxide cube is divided into two layers, one acting as an insulator while the other acting as a semiconductor [1]. The device is acting like a switch with a resistance ratio of 1000, which means that the ratio between the OFF state to the ON state is 1000 to 1, placed in crossbar architecture. The crossbar architecture is a fully connected net of orthogonal nano-wires, where the contact point between any two perpendicular wires represents a switch.

A. Working Principle

The mobile vacancies in the doped layer will be moved from one side to another inside the material, if a voltage is applied on the device terminal. Therefore, the material resistance increases or decreases based on the applied voltage polarity.

When an external positive bias voltage, $v$, is applied across the device, the electric field repels the positively charged oxygen vacancies in the doped layer into the undoped layer and the state length $w$ is changed [1]. Hence, the device total resistivity changes. If the doped region extends to the full length $D$ (i.e., $w/D = 1.0$), the total resistivity of the device reduces (denoted by $R_{on}$). On the other hand, when a negative bias voltage is applied, the undoped region extends to the full length $D$ (i.e., $w/D = 0$) and the total resistivity of the device grows (denoted by $R_{off}$).

Generally, the boundary between the two layers, semiconductor and insulator layer, may be considered as a moving wall, where the direction of the wall movement depends on the polarity of the applied voltage. The device can be totally described by,

$$V = R(w) \times i \tag{1}$$

$$\frac{dw}{dt} = \mu_v \times \frac{i \times R_{on}}{D} \tag{2}$$

where, $V$ is the voltage, $R(w)$ is the system resistance as a function of $w$, $i$ is the current passing through the device, $\mu_v$ is the dopant drift mobility, and $R_{on}$ is the ON resistance of the device when $w = D$. Thus, the width of the doped region ($w$) represents the state variable of the system. The non-volatile property of the system rises from the fact that, when the applied voltage is switched OFF, the total resistance value of the system (the wall position) freezes at its last value (position) before cutting off the voltage. To increase/decrease the resistance value, a positive/negative voltage is applied.

B. Design Considerations

In light of the device analysis introduced in [1], [8]–[10], the design considerations of using a memristor in the realization of a memory cell is summarized as follows:

1) Nano-scale constraints

Because of the device nano-scale, the oxygen atoms are free to move inside the device with a sensible rate, where the device resistance is changing according to this movement. On the other hand, manufacturing process fluctuations control is a key challenge. It is detailed in [11], based on the latest line edge roughness (LER) characterization method for electron beam lithography (EBL) technology from top-down scanning electron microscope (SEM) measurement that, thickness variations show significant impact on the memristive behaviours such as voltage drop and the change in the memristance value. Also, migration of the device with CMOS technology may face some issues because of the differences in the devices scales.

2) Bipolar device

Based on the previous discussions, memristor state depends on the polarity of the applied voltage and hence the memristance value of the device. Consequently, a good attention should be taken on the current direction passing through the device during the reading process, the writing process, or the idle state.

3) Device non-volatility

Memristors store the data as a resistivity. This resistance depends on the oxygen atoms movement, which is caused by the applied stimuli. Thus, if this stimuli is switched off, the oxygen atoms keep its last position. The non-volatile advantage of the device, which make the device a good candidate for memory applications, may be lost during the memory cell design. This loss is coming from designing a memory circuit based on volatile elements (i.e., Latches) beside the memristor.

4) Consumed energy and time

The main important constraints in any electronic system design are the energy consumption ($E$) and the response time ($t$). The consumed energy can be computed as in [9]:

$$E = \int i \times v(w) \ \frac{dw}{w} \tag{3}$$

From (2) and (3), it is obvious that the consumed energy ($E$) decreases exponentially as the current passing through the device ($i$) increases. Accordingly, the heat is decreased. Also, the time required to switch a device between two states ($t$) can be computed as in [9]:

$$\Delta t = \int \frac{dw}{w} \tag{4}$$

which indicate, due to (1), (2), and (4), the time decreases exponentially as the applied current increase. Figure 2 shows the relation between the applied current ($i$), the consumed energy ($E$), and the switching time ($t$). Therefore, writing logic '1' may need more voltage than writing logic '0'. This is because the nonlinear memristor I-V characteristics as portrayed in Fig. 3.

5) Memristance switching

Migration between doped region low resistance and
un-doped region high resistance represents the system resistivity, named system Memristance as,

\[ R(w) = \frac{R_0}{w_0} \left[ w_0 - \frac{\mu \rho}{A} \int_0^t I(t) \, dt \right] \]

(5)

where, \( R_0 \) and \( w_0 \) are the resistance and width of un-doped region respectively, \( \rho \) is the resistivity of the TiO\(_2\), \( A \) is the cross-section area, and \( I \) is the current passing through the device. Accordingly, Memristance is not discrete, instead it is continuous over the time.

It is important to mention that, the electrodes nano size resulted in a series resistance in the range of KOhms, while the device ON resistance is in the range of Ohms. Therefore, the series resistance is larger than the device ON resistance and hence, the device (i.e., switching material TiO\(_{2-x}\)) consumed more current to reset [12]. This consumed current results in increasing the power consumption.

6) **High density memories design**

Because of the device nano-scale, memristor has better scalability, which means more devices can be arranged in the same area that is used for the known CMOS technology, and hence more data is stored. Besides, device memristance continuity makes it possible to store multiple bits instead of one bit as in conventional memory devices.

7) **Frequency response**

There is a reverse relation between the TiO\(_2\) Memristor non-linearity and the frequency as shown in Fig. 3. Therefore, using a higher frequency input source degenerates the device non-linearity, and hence make the system design easier.

8) **Asymmetric ON/OFF switching behavior**

The time needed for OFF and ON switching are noticed to be different, as the OFF switching time is slower than the ON switching time for the same applied voltage as shown in Fig. 2. This attitude is due to the interaction of diffusion and drift on the internal electric field [10].

9) **Stimuli dependence**

Memristance value depends on the total charge injection regardless the source shape, this fact coming from the device unique signal processing criteria. The only thing matter is the net applied injection and the period of the applied stimuli.

C. **Memrestor in Memory Array**

Memristor nano-sizing and its attractive non-volatile criteria make it an appealing memory solution that might finally displace the recently applied flash memory and SRAM. As the memristor is a modest two-terminal nano device that can be used to store multiple bit, it can be used to create a crossbar memory structure with extremely high density, leading to an extra data storage solution than the known memories.

Utilizing the memristor in a crossbar memory array is not an easy task because of its accumulative property. Based on the non-idealism of the devices used in the memory array structure and its consequence (i.e., sneak paths and leakage current), memristor internal state may dramatically change and hence the stored data.

Sneak paths effect is decreased by connecting the unused rows and columns to the ground instead of left it floating as displayed in Fig.4. Grounding those rows and columns set routes for the sneaking currents to the ground instead of the memory elements. This solution will just limit the sneak paths effect not totally eliminate it because portion of the sneak current will find its direction to the ground through the memory elements. However, this solution decreases the total system resistance as this ground paths act as parallel resistances across the system and hence the equivalent system resistance decreased [13].

While grounding the arrays floating terminals does not solve the sneak paths problem, it does marginally improve the noise margin as mentioned in [13]. It is also stated in the same research that, grounding all the floating terminals will cause a huge power consumption while the sneak paths issue not totally solved.

Unfolded crossbar memory array architecture where each memristor has a separate column (displayed in Fig. 5.a) solve the problem at the expense of the memory density. It is stated in [13] the density is decreased by a factor equal to the number of rows.

Another method to solve the sneak paths problem mentioned in [13] is to use one diode with each memristor (1D1M)
Fig. 4. Memory crossbar array where the unused memristor terminals are floating.

The delay of the system because of the added capacitive loads. Also, the output swing will be decreased due to the diode threshold voltage. Using Metal Insulator Metal (MIM) diodes instead of the conventional diodes will provide a better isolation as stated in [14].

Using one transistor one memristor (1T1M) crossbar memory array architecture also discussed in [13]. It solves the sneak paths issue but it also wrecks the crossbar memory density because of the transistor micro-scale. To reduce this problem, memristors can be vertically stacked on the transistors and a mixed crossbar of nano-wires and micro-wires are used. All the previous discussed solutions will eliminate or at least reduce the sneak paths problem at the expense of another factor (i.e., power consumption, data density, or delay time). The sneak paths is highly considerable because of the fact that the crossbar architecture is consisting of two terminal memristor as the memory element. Using a three terminal memristor instead of the two terminal will dramatically reduce the sneak paths problem if it does not eliminate it.

Three terminal memristor is introduced in [15]. It comprise source electrode, drain electrode, gate electrode, and an active region. It has the same working principle of the two terminal memristor except that, it is needed to apply a sufficient voltage with the right polarity on the gate to either inject or eject dopant into or out of the undoped region from the doped region. Thus, applying voltage on the gate will electrically connect or disconnect the source and the drain to each other in a non-volatile manner. Thus, it acts as the known transistors with the advantage of memristors (i.e., nano-scale device and nonvolatile property). In addition, it may have an all-planar geometry as shown in Figure 6.a or a stacked geometry as shown in Figure 6.b.

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III. SIMULATIONS VERIFICATION

The previous analysis is verified by using Cadence Spectre simulation tools. The memristor is simulated by the Verilog-A TEAM model discussed in [16] because of its simplicity, accuracy, and time computation efficiency. For CMOS peripherals, TSMC 130nm industrial hardware-calibrated CMOS technology is used in the simulation. New proposed read/write circuit is used during this simulations as presented in Fig. 7.a. Writing circuitry is a simple circuit where the device is connected to the input source as in Fig. 7.b. As w/D varies from zero to one, Logic one state is considered if w/D = 0.6 to 1 and logic zero state is considered if w/D = 0 to 0.4 [17]. For Reading the stored data, another memristor (M2) used as a load resistance as in Fig. 7.c. The applied voltage is simply divided between M2, which placed to be in the ON state all the time, and the memory element M1. Based on the stored data, Vr may be bigger or less than VDD/2 and hence the inverter output varies. The output is considered logic zero if VO = VL = 0V, and considered logic one if VO = VH = 1V.

A. Writing Data

In this part, simulations performed for writing to or erasing data from the device. The main Memristor parameters (i.e., D, Ron, and Roff) used in the simulation are the default ones mentioned in [16]. The test is performed using different source shapes (i.e, pulse, half sin wave, and triangle input source) as displayed in Fig. 8.a and Fig 8.b.

As shown in Fig. 8 and for the same period of time, turning OFF the device needs more voltage than turning it ON (i.e., 2.35V to switch OFF the device while 1V only to switch it ON). It is clear that, the device has an asymmetry ON/OFF switching behaviour. Therefore, an adapted voltage may be used for different processes (i.e., writing or erasing data) to reduce the power consumption.
Furthermore, the memristor is a bipolar device, where its state does not depend on the applied source shape. However, it depends on the total charge injection. Also, there is an inverse relationship between the passing current and the time needed to change the device state. One more thing, after switching off the applied current, the device keeps its last state as it is a non-volatile device.

B. Testing the Device Internal State

For testing the device internal state, a small sensing voltage (1V) for a small period of time (3ns) is applied. This applied voltage disturbs one of the device states. This is because if a positive voltage is used then the switching ON state is disturbed while the switching OFF state is not affected and vice versa for using negative current.

It is stated in [17] that using a double pulse with equal duration and magnitude but with opposite polarity will neglect the effect off applying the sensing current. In fact this read pattern may eliminate the sensing current effect. This is because the asymmetry criteria of the device. In this circuit a positive sensing voltage is used. Figure 9.a and Figure 9.b display the testing results.

As shown in Fig. 9.a and Fig 9.b, the reading process is a challenge in memristor-based memory circuit design. In Fig. 9.a the internal state of the device changed for reading logic zero as w/D varies from 0 to 0.4. However, the output of the circuit still acceptable as the output pattern is big enough (i.e., w/D = 0 - 0.4). On the other hand, the device state for logic one still the same as the reading process using the same voltage polarity for writing one.

Based on the previous discussion, a refreshment circuit may be needed to remain logic zero state. Another solution is to rewrite logic zero after the reading process. The writing circuit can be triggered after reading logic zero to rewrite the device internal state. Despite its advantage maintaining the device internal state after reading logic zero, it increases the delay time of the circuit.

C. Testing The Sneak Paths problem

The proposed circuit had been used to build 4x4 memory array to test the sneak paths effect on the internal state of the un-selected devices. Sneak paths have a dramatic effect on the devices that storing logic zero as the circuit uses a positive
voltage for the reading process. The aforementioned solutions are implemented while the consumed power and the sneak paths effect are tested. The consumed power is calculated by

\[ P = \frac{1}{T} \int_0^T I \times V \]  

(6)

where, \( P \) is the consumed power, \( V \) is the applied voltage, \( I \) is the current passing through the device and \( T \) is the pulse duration.

Table I summarizes the consumed power, expected area, minimum and maximum sneak paths effect on the un-selected devices internal states. As stated in table I, 1D1M and 1T1M configuration need extra voltage than the normal voltage applied for the reading process \( (V_{\text{read}}) \) by the voltage drop on the diode \( (V_d) \) and the threshold voltage \( (V_T) \), respectively.

Sneak paths effect varies from marked impact to ignored impact based on the distance between the device under the test and other devices.

### IV. Conclusion

In this paper, the design considerations of using a memristor in the realization of a memory cell is discussed. Brief description of the memristor device is presented showing its working principles. Then design considerations and insights regarding using memristor as memory element is stated. Also the main solutions for the sneak paths problem are reviewed as well a new solution using a three terminal memristor instead of two terminal memristor is proposed.

These considerations/insights are used in designing a new memristor based memory read/write circuit. The proposed circuit is tested by a simulation tool. Also, a 4x4 memory array based on the proposed circuit is used to test the sneak paths problem. Furthermore, the reviewed solutions are implemented to test its impact on solving the sneak paths problem. Based on this discussion, reading the stored data and building the memory-array structure considered challenges in the memristor-based memory circuit design.

### ACKNOWLEDGMENT

This research was partially funded by Zewail City of Science and Technology, AUC, the STDF, Intel, Mentor Graphics, MCIT, Academy of Scientific Research and Technology (ASRT), and the Natural Sciences and Engineering Research Council of Canada (NSERC).

### REFERENCES


### TABLE I

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<th>Comparison aspect</th>
<th>Floating Array</th>
<th>Half-Grounded Array</th>
<th>Grounded Array</th>
<th>1D1M Array</th>
<th>1T1M Array</th>
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<tr>
<td>Consumed Power while Reading Logic Zero ((\mu)W)</td>
<td>35</td>
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<td>375</td>
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<td>Sneak Paths effect on the un-selected devices internal state (%)</td>
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<td>8-29</td>
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<td>Applied voltage for reading process</td>
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