Time-Based Read Circuit for Multi-Bit Memristor Memories

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***Abstract*— Memristor has attracted significant attention in various applications including single-bit and multi-bit storage. Utilizing Memristor as multi-bit memory is a promising approach to enhance the memory density for next-generation memory. Memristor offers a good alternative for memory design due to low power, high density, non-volatility, high speed, and analog behavior. This analog behavior is used to store more than one bit in a single Memristor cell. In this work, a time-based read circuit is proposed that supports the read of multi-bit storage cells. This time-based read circuit utilizes a time-based analog-to-digital converter (T-ADC) with 200 mV dynamic range to distinguish between multi-bit states of the Memristor.**

Keywords—memristor; multi-bit memory; read /write circuit.

I. INTRODUCTION

The concept of the "ideal" Memristor (concatenation of "memory resistor") was first introduced in 1971 by Professor Chua [1]. It was thus formally defined as the fourth fundamental circuit element (joining the resistor, the capacitor, and the inductor). In 1976, Chua and his student Kang introduced the fact that a 'memristive device' has a state variable (or variables), indicated by w, that describes the physical properties of the device at any time [2]. In 2008, the memristor in device form was developed by HP labs Team representing the first physical model of Memristor using Titanium Dioxide thin films material sandwiched between two metal electrodes [3]. Memristor has the ability to retain state for a long time after the power is disconnected which is referred to as a nonvolatile device [3]. Due to the memristor ability to remember past charge, an intuitive utilization for it to be used in memory design [3], [6].

The memristor state represents the stored data, for example, the low resistive state of the memristor can represent logic '0', and its high resistive state can represent logic '1'. Since Memristor can be used to store single bit value (i.e., '0' or '1') or multi-bit value (i.e., '00', '01', '10', and '11') for 2-bits value. One of the main challenge in using the Memristor as a memory cell is the design of read circuit. This is because the reading operation should be non-destructive, (i.e., the reading operation must not change the stored data) [5], [7].

Since HP developed memristor in 2008 [3], several papers have been published on a single bit [5], [7] and multi-bit memristor [6], [9], [10] memory realizations. Despite many features of memristor, memristors have several weaknesses in practice. These weaknesses come from the non-linearity characteristics which make it difficult to determine the proper pulse to achieve the desired state [6]. Therefore, it has been considered as a problem for multi-bit memory designs [6]. Many researchers have presented methods to solve this problem; some of them use analog circuit and op-amps for both read and write operations which make the circuit very complex[6], [10]. In this paper, a read/write circuit compatible with digital designs, less complex, lower delay, and low power consumption, is presented. This circuit depends on a time-based analog-to-digital converter, which eliminates the dependency on the op-amp circuits in the analog-to-digital converters (ADCs), while transferring the signal conversion process to the time domain that is processed digitally.

II. MEMRISTOR MODEL

The Memristor is firstly presented by HP lab [3], which is based on the pinched hysteresis loop exhibited by Titanium Dioxide thin films sandwiched between two metal electrodes. The total resistance of the device is the sum of the resistances of two layers; one layer has a high concentration of dopants and the other layer has a low concentration of dopants. The total resistance of Memristor is given as:

$$R = \frac{w}{D} R_{ON} + (1 - \frac{w}{D}) R_{OFF} \qquad (1)$$

Where w is the width of the doped region, D is the total length of the thin film, R_{ON} is the lowest resistance when $w = D$ and R_{OFF} is the highest resistance when $w = 0$.

III. PRELIMINARIES

A. Single bit Memristor

The region for writing and reading '0' or '1' is bounded by one threshold that is selected to be midway between R_{ON} and R_{OFF}.

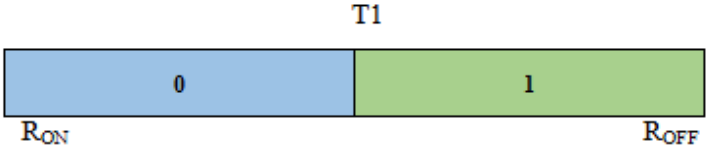

Figure 1. Memristor storing 1-bit value.

B. Multi-bit Memristor

The Memristor is utilized as a multi-bit memory. Multi-bit values such as ('00', '01', '10', '11') or ('000', '001', '010', '011',

'100', '101', '110', '111') can be stored in a single memristor cell. This allows better memory storage utilization and higher density. However, the 2 bits Memristor is divided into four equal regions, where each region is assigned a 2-bits value as shown in Figure 2. Moreover, Figure 2 shows the threshold value for these regions (i.e., T1, T2, and T3) and their mean values (i.e., M1, M2 M3 and M4), T1 = [R_{ON} +T2] / 2 , T2 = [R_{ON} +R_{OFF}] / 2, T3=[T2+R_{OFF}] / 2 , M1 = [R_{ON}+T1] / 2 , M2 = [T1+T2] / 2 , M3 =[T2+T3] / 2 and M4 = [T3+R_{OFF}] / 2 .

In order to write '00', the input charge should change the memristance value from the initial value to M1. Therefore, the input charge depends on the initial state which is assumed to be the worst case (i.e., the initial state is assumed '11' when it is required to write '00' and the required charge should change the memristance state from M4 to M1). For the read operation, the memristance value is sensed and compared to the thresholds (i.e., T1, T2, and T3) [8].

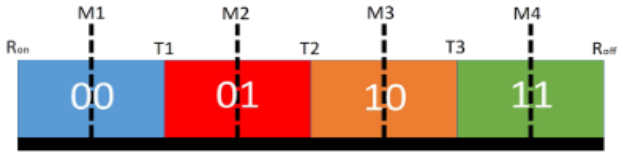

Figure 2. Multi-bit memristor storing 2-bits values [8].

IV. PROPOSED DESIGN

The proposed read design circuit deals with the memristor as single bit and multi-bit, based on simple circuit of (T-ADC) with 200 mV dynamic range.

A. Write operation

As shown in Figure 4, the write circuit depends on pulse based, where a pre-determined duration and amplitude pulse is applied to the Memristor cell (M1). This is performed by connecting S_1 to V write and S_2 to ground.

B. Read operation

The read circuit is divided into two stages. The stored data is measured and interpreted as a voltage signal. This voltage is converted into a pulse delay through a voltage-to-time converter. Then, this pulse delay is converted into a digital code through a time-to-digital converter. Figure 3 shows the proposed block diagram for reading operation.

Figure 3. Proposed block diagram for reading operation.

C. Circuit description for Read operation

Figure 4 shows, M1 is The Memristor Memory cell, R1 is a load resistor. Node X between M1 and R1 will have a unique voltage value depending on the resistive state of M1 and R1. The uniqueness of this node voltage allows the use of (T-ADC) to determine exact resistive state of memory cell M1.

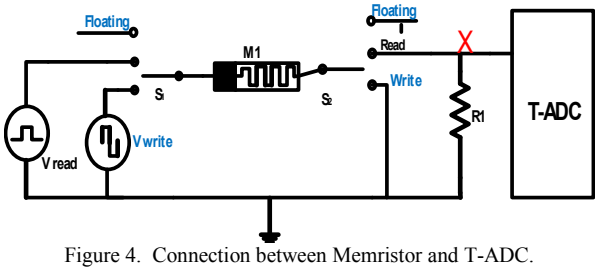

Figure 4. Connection between Memristor and T-ADC.

In the proposed circuit, the basic circuit that can be used to convert the analog voltage into a pulse delay is the starved inverter circuit [12], As shown in Figure 5. The input voltage at node 'X' controls the delay of the falling edge of the clock signal, Vclk; through the inverter (Transistors M4 and M5), by controlling the discharging current of transistor M3 [12]. For 2-bit case, there are 4 resistive states that encode the bits stored in a memory cell M1. These 4 unique resistive states generate 4 different voltage levels at node 'X', and the starved inverter converts these different voltage levels into 4 different output delays. As the cell resistance increase, the voltage level begin to decrease.

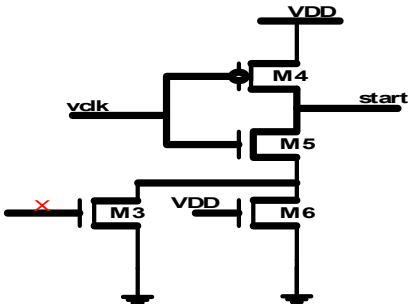

Figure 5. Starved inverter [12].

The Time to digital converter (TDC) is used to convert the output delay produced by the starved inverter into a thermometer code that is encoded into a binary code. Vernier delay line TDC consisted of 2 parallel delay chains and sense amplifier D-flip flop [13]. The delay of the buffer in the upper chain T_1 is greater than the delay of the buffer in the lower chain T_2. The stop signal is the reference signal. The signals (start, stop) travel through these delay chains until they become aligned. Sense amplifier D-flip flop determines which of the two input signals came first and produces the thermometer code. For 1-bit case, 1 flip-flop is needed, for 2-bits case, 3 flip-flops are needed. Hence we follow this formula to determine the number of flip-flops: 2^n -1; where n: represents bits number. The outputs of flip-flops in case of 2-bits are the thermometer code: q1, q2, q3. These outputs applied to an encoding circuit which converts the thermometer code into 2-bits.

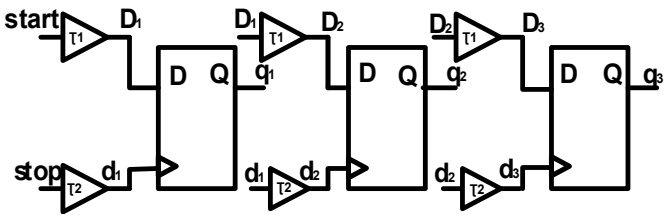

Figure 6. Vernier Line TDC [13].

V. SIMULATIONS

The proposed read/write circuit behavior is verified using cadence spectre simulation tools TSMC 130 nm technology. The TEAM Model for the memristor that is used with the proposed circuit, for more information on this model; one can refer to [4].

1) Write simulation

In these simulations, the memristor state Wn is changed from '00' to ('01','10' and '11'). The following values were used $R_{OFF} = 200$ KΩ, $R_{ON} = 100$ Ω for (M1), pulse duration: 2 ns, V write = 0.422 V, 0.950 V, 2.5 V to change the initial state of M1 to the desired states respectively.

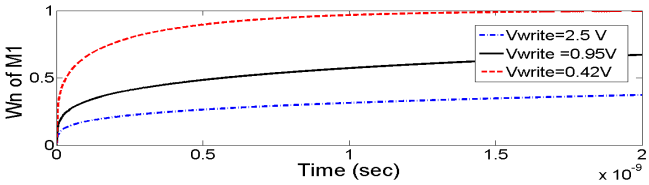

Figure 7. Writing of various values into the memory cell.

2) Read simulation

The following values were used $R_{OFF} = 200$ KΩ, $R_{ON} = 100$ Ω for M1, and R1= 600 KΩ, Read pulse magnitude = 800 mV, Read pulse duration = 1 ns. Supposed that Memristor cell stores 2-bits and required to read the stored data. The results show that outputs of a starved inverter are 4 different delays based on resistive states of Memristor cell, the output of flip-flops (Thermometer Code): q1, q2, q3, and the encoding output: out0 and out1 in each case. Moreover, the results confirm that the reading operation does not change the internal state of Memristor as shown in Figure 9, Figure 10, Figure 11, and Figure 12.

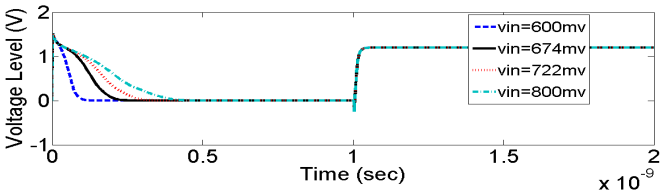

Figure 8. Output wave form of starved inverter at different input voltage in case of 2-bits.

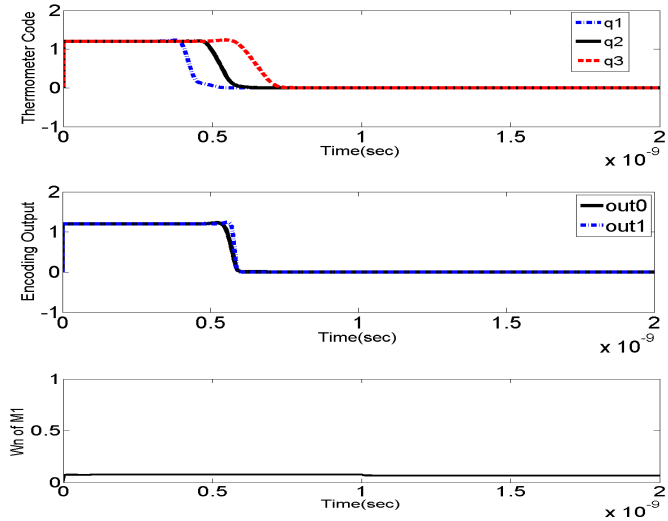

Figure 9. Reading state of M1 in case of 00.

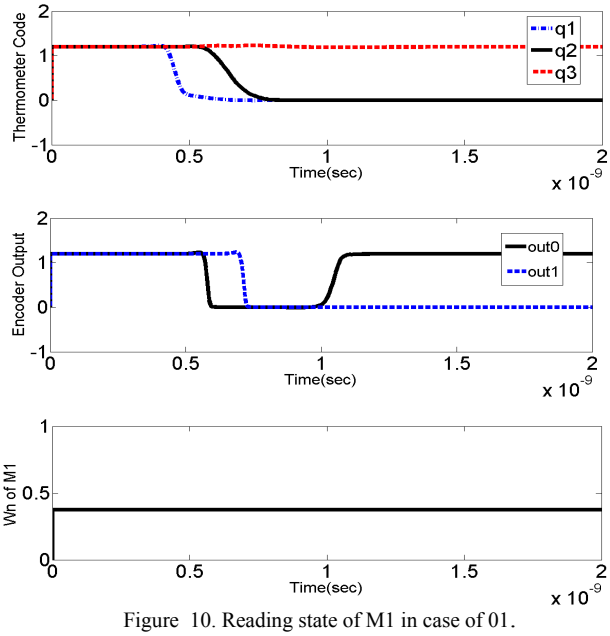

Figure 10. Reading state of M1 in case of 01.

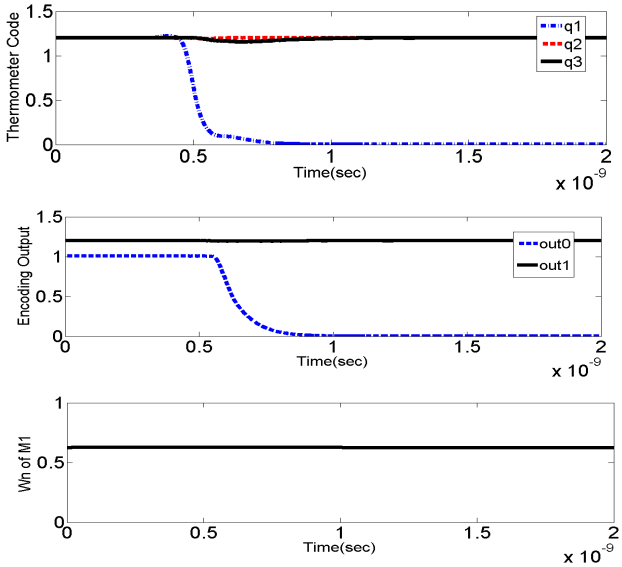

Figure 11. Reading state of M1 in case of 10.

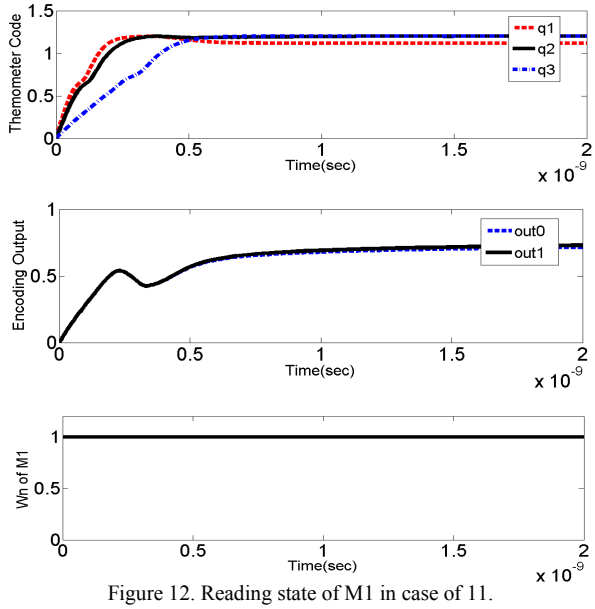

Figure 12. Reading state of M1 in case of 11.

VI. COMPARISON WITH CONVENTIONAL READ CIRCUIT

Most read methods typically include comparing the resistivity of selected memory against the reference resistor to determine the current state. The difficulty increases with the designing of multi-bit memristor memories because 2n comparators and 2n reference resistors are required per state to verify if the exact state of memristor is reached or not. In the proposed circuit, in order to verify the exact resistive state for multi-bit Memristor cell, one starved inverter is needed and the flip-flops number are determined using this formula: 2^n -1.

TABLE.1 Calculation of power and delay for 1-bit Memristor.

Comparison Aspects	**El-Shamy [7]**	**Proposed circuit**
Power for read 0 (µW)	290	5.5
Power for read 1 (µW)	260	6.5
Delay for read 0 (psec)	400	430
Delay for Read 1 (psec)	400	436

TABLE .2 Calculation of power and delay for 2-bits Memristor.

Comparison Aspects	**Read '00'**	**Read '01'**	**Read '10'**	**Read '11'**
Power (µW)	11	11.5	12.3	12.8
Delay (psec)	600	610	615	620

VII. CONCLUSION

In this paper, a read/write circuit for multi-bit Memristor-based memory cell is presented and discussed. The proposed circuit enables the storage of multi-bit in a single memory cell with low power consumption, less delay time, and transferring the signal conversion process to the time domain that is processed digitally; moreover it eliminates the dependency on the op-amp circuits in the analog-to-digital converters (ADCs).

ACKNOWLEDGEMENT

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