A Novel CMOS-based Fully Differential Operational Floating Conveyor

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***Abstract*—This paper presents the novel concept of the fully differential operational floating conveyor (FD-OFC) for the first time, to the best of the authors knowledge. A CMOS design for the proposed FD-OFC is introduced as an 8 (4x4) port general purpose analog building block. The proposed design has the advantage of low power consumption as it can operate under biasing conditions of only 1.5 V, while its wide bandwidth exceeds 100 MHz. These operating conditions recommend the proposed device to be integrated to a wide range of low power-wide high speed applications. The terminal behavior of the proposed device is mathematically modeled and its operation is simulated using the UMC 130 nm technology kit in Cadence environment.**

I. Introduction

[1] Analog circuits can be generaly classified into two broad categories. The first includes analog circiuts operating in the voltage mode, while the second category includes those operating in the current mode. Voltage mode analog circuits are often more popular and preferred in most analog signal processing applications. Unfortunately, most of these circuits rely on the conventional operational amplifier (Op-Amp), which usually exhibit a narrow bandwidth and is highly dependent on the gain via the gain bandwidth product (GBP). The fixed GBP is an inherent property of the Op-Amp itself. This limitation always stimulates a trade-off between both quantities as tailored to each particular application. This limitation has motivated the use of current as the active parameter, a concept which has lead to the development of many current-mode circuits such as the second generation current conveyor (CCII) [1]. Since then, many current mode based devices have been developed [2] to solve this problem as they provide a degenerate gain-bandwidth relationship. Moreover, current mode based device also offers the advantage of high slew rate as compared to their voltage mode based counterparts. Due to these and more advantages, research interests have been directed to the development of such devices as they are perfect candidates for a wide range of analog applications such as biomedical instrumentation and data acquisition devices.

The rest of this paper is structured as follows. In Section II, the principle of operation of the OFC is reviewed and its terminal behavior is characterized. Section III introduces the newly developed concept of the FD-OFC, its CMOS-based design and its terminal behavior is introduced based on the OFC model reviewed in Section II. The performance of the proposed FD-OFC is investigated in section IV via simulation results. The whole paper is finally concluded in Section VI.

II. Current Mode Devices : An Overview

This section overviews three of the most common types of current mode devices along with their mathematical model. These three devices are introduced through a historical development approach.

1) The second generation current conveyor (CCII): Fig. 1 depicts a simplified schematic for the inverting and non-inverting versions of the second generation current conveyor CCII+/-. The principle of operation of the CCII+ can be briefly summarized as follows. The voltage applied at terminal Y exactly appears at X with zero current at terminal Y (i.e., infinite input impedance at terminal Y) and independent voltage and current at terminal X of V_x and I_o respectively. The voltage following action at the input ports is accompanied by conveying the current I_o to the output terminal Z. This mechanism of operation can be represented using the following matrix notation as [1],[2]

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (1)$$

2) Fully differential second generation current conveyor (FDCCII): Fig. 2 depicts a simplified schematic for the FDCCII. Both inverting And non-inverting versions of the FDCCII exist (FDCCII+ and FDCCII-) [3],[4]. As its name

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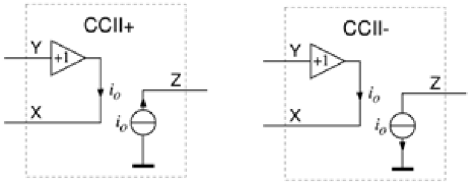

Fig. 1. Schematic representation of a typical second generation current conveyor

implies, the FDCCII is the differential form of the CCII. As shown in Fig. 2, it has six terminals (two for each terminal) such that the input and output signals at terminals fully differentially. The principle of operation of the FDCCII can be explained as follows. The differential input voltage applied at terminal Y is $V_{y1} - V_{y2}$ ideally appears as a differential voltage $V_xd = V_{x1} - V_{x2}$ at terminal X regardless of the forced current I_o to this terminal. This is the same voltage following action at the input ports as in the CCII. The currents at the individual terminals Y_1 and Y_2 refer to an infinite input impedance at terminal Y, while the currents I_{x1} and I_{x2} are conveyed to the output differential terminals Z as $I_{z1} = I_{x1}$ and $I_{z2} = I_{x2}$, respectively. The ideal operational mechanism can be expressed in matrix form as [5]

$$\begin{bmatrix} I_{y1} \\ I_{y2} \\ V_{x1} \\ V_{x2} \\ I_{z1} \\ I_{z2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & \pm 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{y1} \\ V_{y2} \\ I_{x1} \\ I_{x2} \\ V_{z1} \\ V_{z2} \end{bmatrix} \quad (2)$$

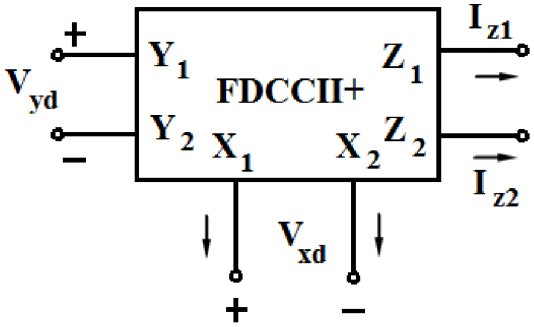

Fig. 2. Block diagram representation of a typical fully differential current conveyor

3) The Operational Floating Conveyor (OFC): The concept of the OFC, which offers more features than both the CCII and FDCCII, has been first introduced [6] based on the BJT technology and redesigned [7] using the more advanced CMOS technology. Figure 3. illustrates the operation of the OFC via its block diagram representation. As clear from this figure, the OFC is a four (2x2) terminal device. The ideal operation of the OFC can be explained as follows. The voltage applied at terminal Y appears exactly at the terminal X with V_x is independent of the input current I_x. This is the voltage following action at input ports. The current at terminal Y is ideally zero (i.e., infinite input impedance at Y). As for the output ports, the voltage at terminal W is the product of I_x and the trans-impedance Z_T while I_w is ideally conveyed to the terminal Z as I_z. This action is called the current following action at the output ports. This ideal operation of the voltage and current actions at the input and output ports respectively can be mathematically represented in matrix form as [8]

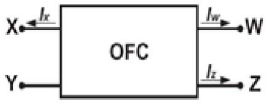

Fig. 3. Block diagram representation of a typical operational floating conveyor

$$\begin{bmatrix} V_x \\ I_y \\ V_w \\ I_z \end{bmatrix} = \mathbf{T}^{(OFC)} \begin{bmatrix} I_x \\ V_y \\ I_w \\ V_z \end{bmatrix} \quad (3)$$

where

$$\mathbf{T}^{(OFC)} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ Z_t & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix}$$

In what follows, the FDCCII is used as a basic constituting block in building a proposed differential form of the OFC as will be clear in the next section such that voltage following actions, the current following actions and the differential property of both the FDCCII and the OFC are achieved.

III. The Proposed FD-OFC

This section presents the basic concept as well as the model of the proposed FD-OFC which is an extension of the OFC circuit [4],[5] reviewed in Section II. This extension is achieved by cascading two FDCCII-'s via two trans-impedance coupling amplifiers [3], of Z_t gain each. Fig. 4 illustrates this concept via block diagram representation, while the schematic diagram representations for the FDCCII- and the trans-impedance amplier are shown in Figs. 5 and 6, respectively.

As shown in this figure, from a block diagram viewpoint, the FD-OFC has twice as much number of terminals as those in the conventional OFC which results in the operation in the fully differential mode; hence its name. Accordingly, the ideal I/O terminal behavior can be expressed in terms of a transfer matrix T of the OFC as follows.

$$\begin{bmatrix} \mathbf{V}_{xd} \\ \mathbf{I}_{yd} \\ \mathbf{V}_{wd} \\ \mathbf{I}_{zd} \end{bmatrix} = \mathbf{T}^{(FD-OFC)} \begin{bmatrix} \mathbf{I}_{xd} \\ \mathbf{V}_{yd} \\ \mathbf{I}_{wd} \\ \mathbf{V}_{zd} \end{bmatrix} \quad (4)$$

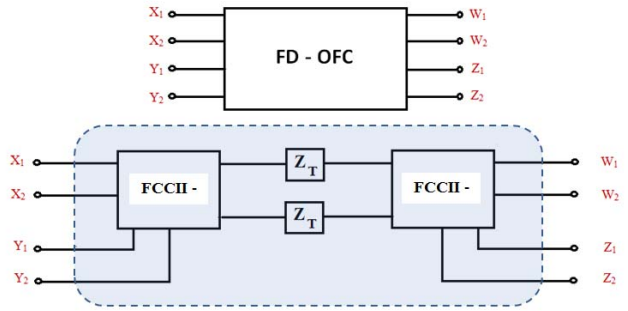

Fig. 4. Block diagram representation of the proposed FD-OFC. (a): a 4x4 port representation. (b): building blocks of the FD-OFC.

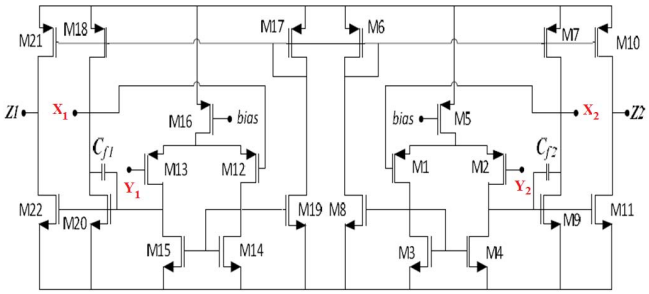

Fig. 5. Schematic diagram representation of the FDCCII-

where the (*i*,*j*) entry of the FD-OFC transfer matrix is given by $\left(\mathbf{T}^{(FD-OFC)}\right)_{ij} = \mathbf{I}_2 \otimes \left(\mathbf{T}^{(OFC)}\right)_{ij}$, $\mathbf{I}_2$ is a 2×2 identity matrix and $\otimes$ is the Kronicker product. Accordingly, the FD-OFC transfer matrix can be expanded as follows.

$$\mathbf{T}^{(FD-OFC)} = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ Z_t & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \quad (5)$$

where $\mathbf{I}_{x_d} = [I_{x_1} I_{x_2}]^T, \mathbf{I}_{y_d} = [I_{y_1} I_{y_2}]^T, \mathbf{I}_{z_d} = [I_{z_1} I_{z_2}]^T, \mathbf{I}_{w_d} = [I_{w_1} I_{w_2}]^T, \mathbf{V}_{x_d} = [I_{x_1} I_{x_2}]^T, \mathbf{V}_{y_d} = [I_{y_1} I_{y_2}]^T, \mathbf{V}_{w_d} = [I_{w_1} I_{w_2}]^T, \mathbf{V}_{z_d} = [I_{z_1} I_{z_2}]^T$ and $[.]^T$ denotes the matrix transpose operator.

IV. Simulation Results and Analysis

This section is devoted to present numerical results that validate the workability of the proposed design along with its associated structural parameters. The proposed FD-OFC circuit is simulated using the UMC 130nm CMOS-based technology kit in Cadence environment. The simulation starts by characterizing each of the MOSFET transistors involved in the constructed model as required by Cadence. Since the FDCCII- and the transimpedance amplifier are the fundamental building blocks which form the proposed device, the transistor specification of both blocks are illustrated in Table I and II, respectively. The entire circuit is simulated under 1.5 Volt biasing conditions.

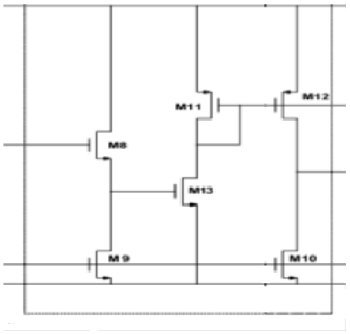

Fig. 6. Schematic diagram representation of the trans-impedance amplifier

TABLE I
TRANSISTOR ASPECT RATIO FOR THE FCCII-

Transistor Name	Transistor Aspect Ratio W/L (µm/µm)
M7-M10-M18-M21	63.7/0.39
M9-M11-M20-M22	55.9/0.39
M5-M16	20.8/0.13
M1-M2-M12-M13	11.96/0.13
M3-M4-M14-M15	5.9/0.13
M6-M17	11.18/0.13
M8-M22	7.54/0.13

TABLE II
TRANSISTOR ASPECT RATIO FOR THE Z_T CIRCUIT

Transistor Name	Transistor Aspect Ratio W/L (µm/µm)
M8	10.4/0.65
M9-M13	26/0.65
M10	5.2/0.65
M11-M12	13/0.65

Figs. 7 (a)-(f) show the frequency response (magnitude and phase) resulting from simulation the proposed FD-OFC. In all figures, it is clear that the frequency responses are essentially flat for frequencies ranging from 0 up to about 100 MHz which confirms the suitability of the proposed FD-OFC for the nominal switching speeds of analog applications. Moreover, the constancy of the frequency response in all figures validates the use of the frequency independent matrix representation in (5) for frequencies ranging from 0 up to 100 MHz.

Figs. 7 (a) and (b) plot the magnitude frequency response (in dB) and the phase response (in degrees) between the differential voltages at the X and Y terminals. Clearly these two figures confirm the voltage following action between the two terminals in the differential form as well as distortion-free transmission between the two terminals for frequencies up to 100 MHz as long as the magnitude frequency response is only concerned and up to a frequency of about 10 MHz if both the

magnitude and the phase frequency responses are considered simultaneously.

Figs. 7 (c) and (d) plot the magnitude frequency response (in dB) and the phase response (in degrees) between the differential currents at the W and Z terminals. Clearly these two figures confirm the validity of approximating a current following action between the two terminals in the differential form expect for a gain of only 0.44 dB, corresponding to a constant offset of 0.05 from an expected unity gain. The phase shift between both terminals is almost zero for frequencies ranging from 0 up to about 10 MHz. This ensures a distortionless current following action up to this frequency. The phase shift starts to increase such that a total phase offset of is achieved at a 100 MHz frequency.

Figs. 7 (e) and (f) show the magnitude frequency response (in dB) and the phase response (in degrees) between the differential voltage at terminal W and the differential current at terminal X, respectively. The open loop transimpedance gain is constant and equal to 44.5 dB for AC signals having frequencies up to 100 MHz. Again, the phase response preserves its constancy only up to one decade less than the magnitude frequency response. In general, it can be correctly concluded that the overall bandwidth of the proposed FD-OFC is about 100 MHz for applications where the magnitude frequency response is the only quantity considered. Meanwhile, the system bandwidth is limited to only 10 MHz if an almost distortion free processing is desired.

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V. Conclusion

This paper presents the novel concept of the fully differential-OFC as an extension of the conventional OFC. As a member of the analog signal processing circuits operating in the current mode, the proposed device has the fundamental advantage of independent gain and bandwidth. The proposed concept is presented in the form of a circuit design. It is shown, via simulations that the proposed concept and circuit design is perfectly suitable for low power- high speed applications as it can operate under biasing conditions as low as 1.5 volts and bandwidths as high as 100 MHz Moreover, the fully differential operation of an OFC recommends its integration in applications where a high noise rejection ratio is desired.

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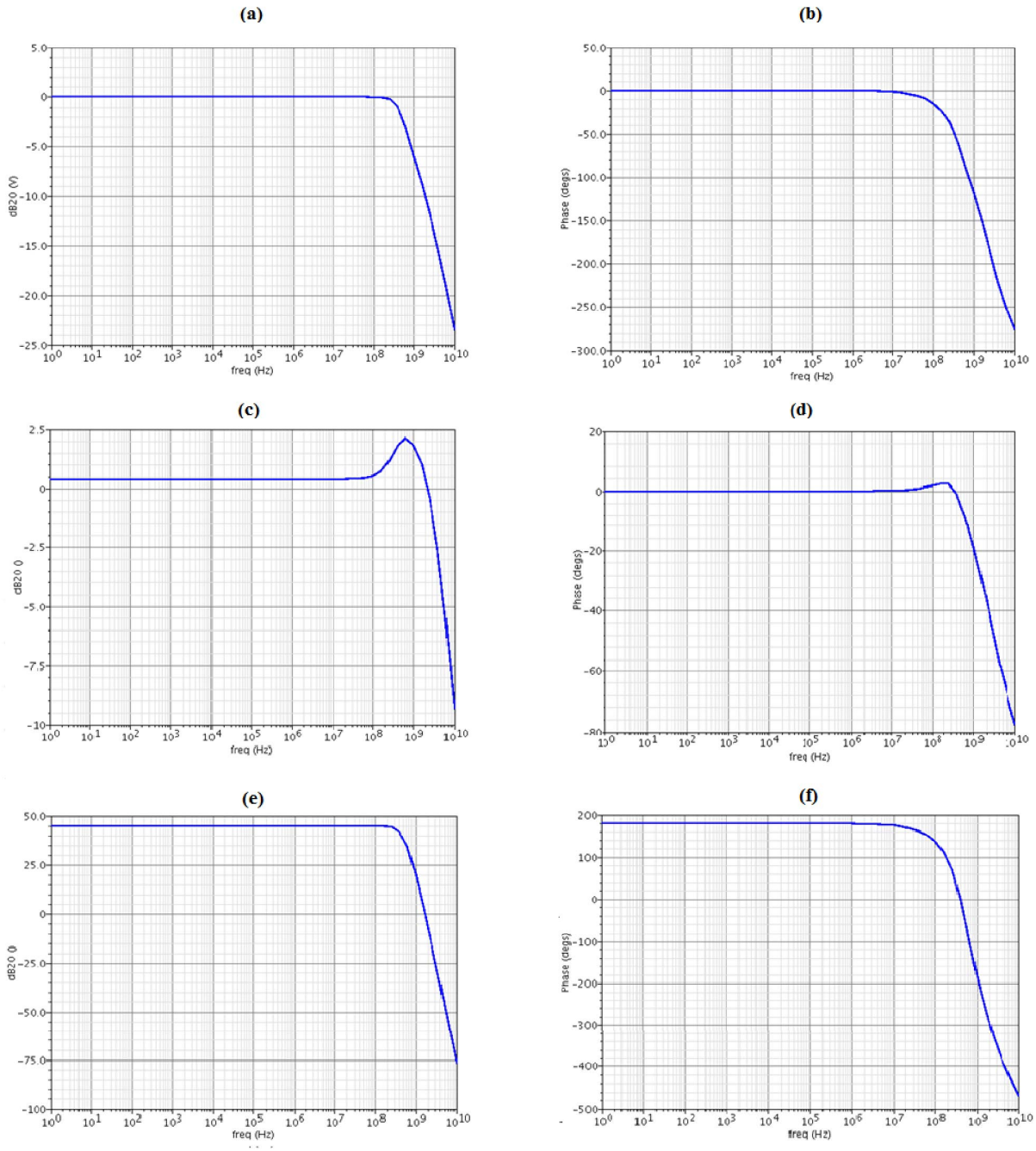

Fig. 7. Overall frequency response of the proposed FD-OFC (a): Voltage magnitude frequency response between terminals X and Y (b): Voltage phase response between terminals X and Y (c): Current magnitude frequency response between terminals W and Z (d): Current phase response between terminals X and Y (e): Magnitude frequency response of the trans-impedance gain between terminals X and W (f): Phase response of the trans-impedance gain between terminals X and W