A 200MS/s, 8-bit Time-based Analog to Digital Converter (TADC) in 65nm CMOS Technology

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***Abstract*— Time-based-Analog-to-Digital-Converter (TADC) is an important block in various applications that require higher resolution and lower power consumption compared to the conventional ADCs at scaled CMOS technologies. In time-based ADCs, the input voltage is first converted into a pulse in time by using a Voltage-to-Time Converter (VTC) circuit, and then the pulse is converted to a digital output by using a Time-to-Digital Converter (TDC) circuit. In this paper, a TADC is proposed with a VTC that achieves high linearity and large dynamic input range and a TDC that achieves a time resolution of 3.9 ps. A 200MS/s, 8-bit TADC with effective number of bits (ENOB) equals 7.6 bits is proposed.**

***Index Terms*— Nanometer CMOS technology, Voltage-to-Time Converter, Time-to-Digital Converter, Time-based Analog-to-Digital Converter.**

I. Introduction

New implementations of ADCs based on time quantization have been arose to help reducing of the drawbacks such as the reduced voltage swing and to take the advantage of the high speed circuitry brought by the VLSI scaling. One common feature in these implementations is that the signal is represented in the time domain during data cconversion. These implementations are called time-based ADCs since their resolution is determined in the time domain, that differs from the conventional ADCs. In TADCs, the input analog voltage is first converted to a delayed pulse in time by using a VTC circuit, and then the delayed pulse is converted to a digital output by using a TDC circuit.

Figure 1 shows the block diagram of the VTC circuit on which the proposed design is based. The analog input voltage, V_{in} , and the input clock, V_{CLK}, are applied to each of the two current starved inverter circuits named t_{RISE} and t_{FALL} shown in Figure 2. In the t_{RISE} circuit, the rise time of the inverter is controlled by V_{in} through transistor Pb2. Transistor Pb3 is a weak transistor used to be an alternative current path when transistor Pb2 is OFF. Similarly, In the t_{FALL} circuit, the fall time of the inverter is controlled by V_{in} through transistor Na2. Transistor Na1 is a weak transistor used to be an alternative current path when transistor Na2 is OFF. The voltage V_2 is an inverted version of the V_{CLK} with falling delay t_f which is controlled by the input voltage V_{in}. V_{CLK} is applied to an inverter delay line (i.e., odd number of CMOS inverters) equivalent to a delay Δ and then applied to the t_{RISE} circuit. The voltage V_1 is then a delayed version of V_{CLK} with rising delay t_r which is controlled by V_{in}. The voltages V_1 and V_2 are then applied to a CMOS XNOR gate to produce V_{pwm} . Vpwm contains two pulses. The first pulse width equals $\Delta + t_r - t_f$ where t_r and t_f are controlled by V_{in}. The second pulse width equals to a fixed pulse width Δ which is independent on V_{in}.

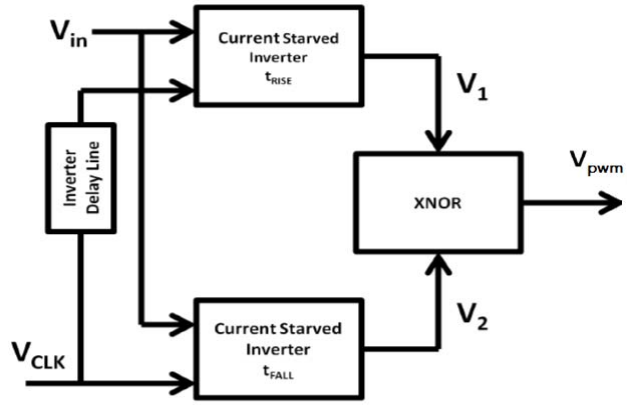


Fig. 1. Basic Idea of VTC [1].

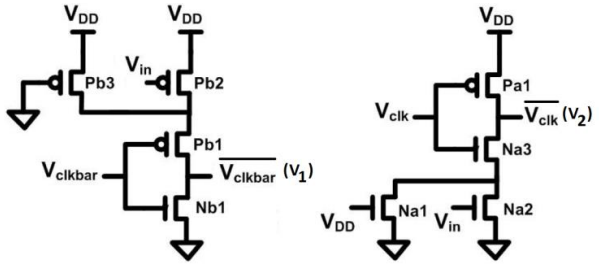


Fig. 2. (a) t_{RISE} current starved inverter and (b) t_{FALL} current starved inverter.

The basic task of TDC is to convert the time representation which corresponds to the analog input into a digital code. The conversion is done by comparing the edges to output signals generated from VTC. In this section, we will refer to the signals as LEAD (START) signal and LAG (STOP) signal. So,

the task of the TDC is to convert the time interval between a LEAD and a LAG into a digital output.

Theoretically speaking, function of the TDC can be done using a simple counter. However, high resolution required in most applications, in order of picoseconds, makes the implementation of the TDC using a simple counter very complex and impractical because of the need to unreasonably high clock counter frequency. Among all the TDC, this paper will focus on multi level vernier TDC which is based on simple flash TDC.

Figure 3 shows simple flash TDC, The LEAD signal propagates along a chain of delay elements of equal delay. The output of every delay element is connected to the input of a D-flip-flop. As shown in figure 6, when the lead signal catches up the lag signal the output of the D-flip-flop will be one.

The outputs of D-flip-flops are represented by a thermometer code which represents the time difference between the lead and the lag signals. This type of TDC uses only digital delay elements and D-flip-flops. The resolution of this TDC is given by a delay introduced by one delay element [1].

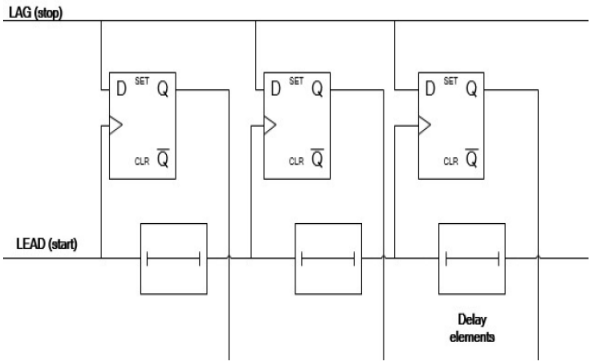


Fig. 3. Simple TDC.

The improvement of the resolution of flash TDC can be achieved by using a Vernier method. The technique is based on a Vernier principle which we use two chains of delay lines. The delay time (T_{ds}) of delay element in lower delay chain is greater than that (T_{df}) in upper delay chain. As two asynchronous signals propagate, the time interval between these two rising edge of signals will decrease in each Vernier delay element a time difference $T_R = T_{ds} - T_{df}$. Where T_R is the resolution. In each stage, LEAD and LAG signals are the inputs to D-flip-flops which indicate when the catch up occurs

II. Voltage-To-Time Converter

The design in [1] achieves highly linear dynamic range of 150mV and high sensitivity of ρ = 3.46ps/mV but in the proposed TDC a time range of 1ns is used and a resolution of 8-bit is targeted so the best sensitivity should be ρ = 3.9ps/mv ($\rho = time\_resol^n/voltage\_resol^n = (1000ps/2^8)/(dynamic\ range/2^8)$) so at least a dynamic range of 256mV is needed to be used in the design of the proposed TADC, so sizing is done to reach this dynamic range and keep the same linearity and sensitivity.

Sizing is done on PMOS transistors of t_{RISE} and t_{FALL} circuits as it enhances performance of the circuit. Also, to get best use of this circuit linearity, it is required to convert the PWM signal obtained into PPM signals.

Figure 4 shows the timing diagram of the proposed VTC. V_{PWM} is V_{pwm} but after removing second pulse of width Δ and this is done by ANDing it with V_{CLK} as shown in Figure 5.a. Then, obtaining two signals, the delay between them is changing by a step equivalent to the step in width of V_{PWM}. This is done using a D flip-flop to obtain the first signal, START, as shown in Figure 5.b. But, the START signal is delayed by a delay equivalent to the width of the V_{PWM} pulse when Vin is at the beginning of the dynamic range. This delay is added to ensure that the first delay between START and STOP signals is zero then changes by a constant step equivalent to $t_r - t_f$. STOP signal is obtained by ANDing the START signal with the inverted V_{PWM} as shown in Figure 5.c.

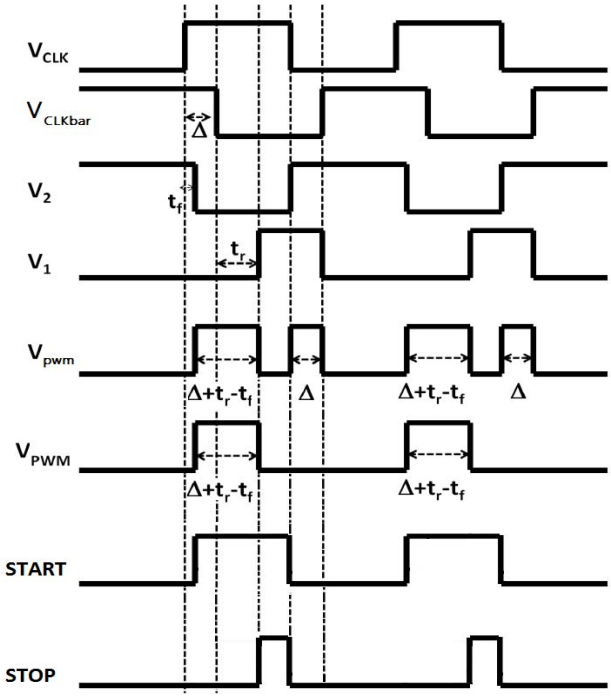
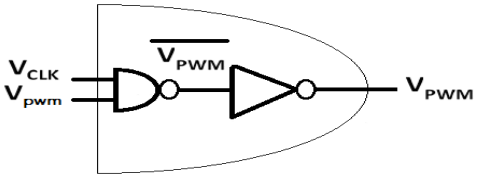
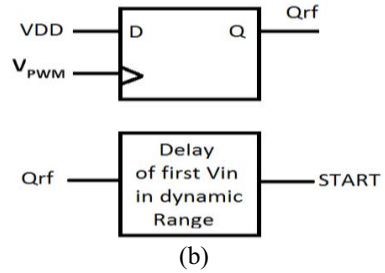


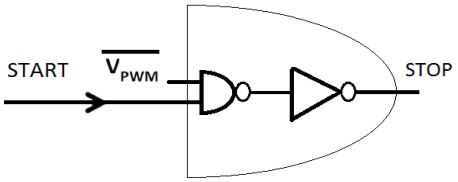
Fig. 4. Timing diagram of proposed VTC.



(a)



(b)



(c)

Fig. 5. (a) Removing second pulse Δ, (b) Obtaining START signal and (c) Obtaining STOP Pulse

III. Time-To-Digital Converter

Although the resolution of VDL can achieve the order of pico-second, VDL has the drawbacks of long conversion time and needing large number of elements. So two levels VDL technique could be used. This idea is similar to that of Vernier caliper. There are two level of measurement . The full dynamic range is divided by the number of delay elements to represent the coarse level resolution. This coarse resolution is divided by the same number of elements to represent the fine level resolution. In other words, in the coarse VDL we can achieve coarse Resolution (T_{CLK} = N), and the signals will be sent to the fine VDL by the help of an interface circuit. Fine resolution ($T_{CLK}=N^2$) can be achieved in the second VDL [1].

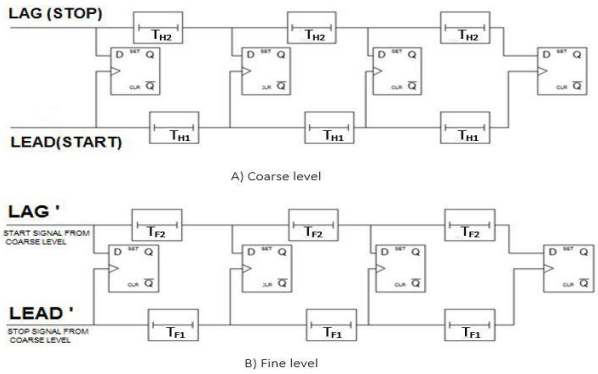


Fig. 6. Coarse level and fine levels.

Figure 6 shows the Coarse VDL and Fine VDL. In Coarse VDL, let the delay time in down line is T_{H1} delay units which is slightly greater than that of the upper line T_{H2} units The time resolution in is $T_{RCoarse} = T_{H1} - T_{H2} = T_{CLK} = N$. In Fine VDL, the two kinds of delay time are T_{F1} and T_{F2}, as in the coarse level the time resolution in Fine VDL is $T_{RFine} = T_{F1}–T_{F2} = T_{CLK} = N^2$ [2].

In the coarse level after the catch up occurs as in figure 7, the two signals will be transmitted to the fine level which will measure the difference between them with its fine resolution. The NOR gates can detect the HI/LO transition(transition between logic outputs one and zero), so NOR gates connected to the output(Q) and the output bar(Q') of each two successive D flip-flops. For example, if the LEAD signal catches up the LAG signal in the (ith) Vernier delay element then only C(i) (output of nor) will become HI (logic output 1) and so we need to send the two signals (D(i) and M(i)) to the fine level VDL [2].

Figure 7 can simply illustrates the concept of coarse and fine, we can see that the two signals propagate first with a large difference delay till catch up happens, then propagate with a small delay to determine the exact delay between them.

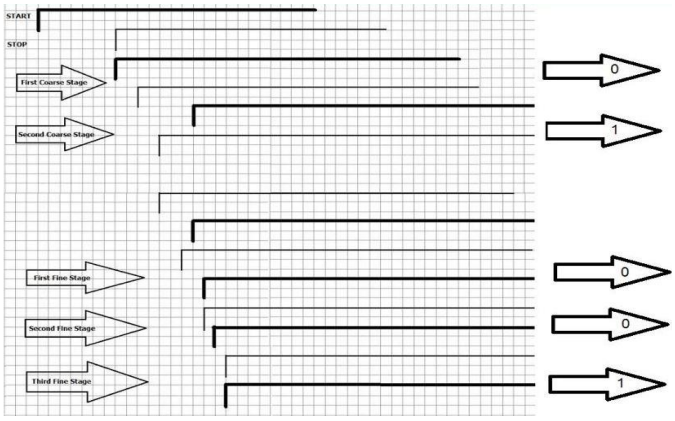


Fig. 7. Timing diagram of Multi Level VDL showing coarse and fine level.

To transmit signal from fine level to coarse level an interface circuit as shown in Figure 8 could be used. Here we connect outputs of each stage to gate of NMOS also we connect outputs of NOR gate so when a catch up occurs the two signals at the moment of catch up (at stage where catch up occurs) is transmitted to fine level.

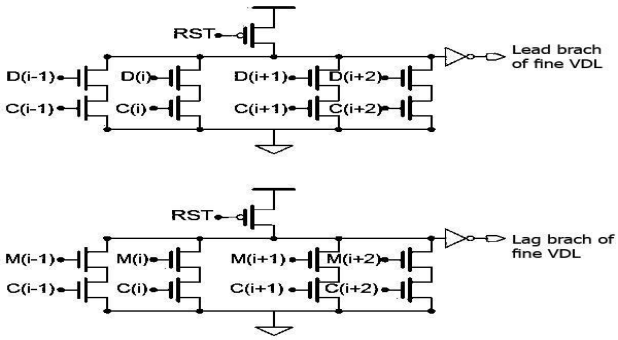


Fig. 8. Interface Circuit

IV. Read Out Circuit

READ OUT circuit is aiming to calculate the 8-bit binary output from the thermal codes outputs of the coarse and fine level. Every count (every delay element) in the coarse level represents sixteen counts in binary, and the fine level is the extra counts (the amount of excess delay) needed to be subtracted from the coarse to give the right output binary number. So we can conclude the equation represents the READ OUT circuit as follow:

BINARY O/P = 16*COARSE – FINE. (1)

Both of coarse and fine in binary. The binary outputs of the thermal to binary unit can be determined from the following equations:

$B_0 = H_1+H_3+H_5+H_7+H_9+H_{11}+H_1$ (2)

$B_1 = H_2+H_3+H_6+H_7+H_{10}+H_{11}+H_{15}$ (3)

$B2 = H_4+H_5+H_6+H_7+H_{12}+H_{13}+H_{15}$ (4)

$B3 = H_8+H_9+H_{10}+H_{11}+H_{12}+H_{13}+H_{15}$ (5)

$B_4 = H_4$ (6)

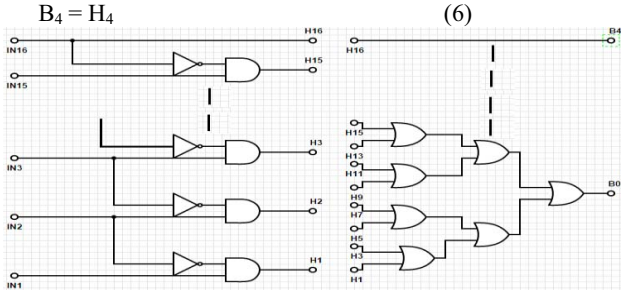


Fig. 9. Design of Thermal to Binary Unit.

We used the fat tree design for the thermal to binary unit as shown in figure 9. And we can notice that multiplying by sixteen is equivalent to shifting by four bit, so we used the 9-bit subtractor directly and entered the coarse binary shifted with four bits.

V. SIMULATION RESULTS AND DISCUSSIONS

Figure 10 illustrates the delay difference between START and STOP signals versus the input analog voltage V_{in} that changes from 384mV to 675mV providing a dynamic range of 291mV. Outside this dynamic range the linearity error is larger than 3%. The sensitivity of this VTC circuit, defined as the slope of the delay-V_{in} curve, denoted by $\rho = 3.43$ps/mV.

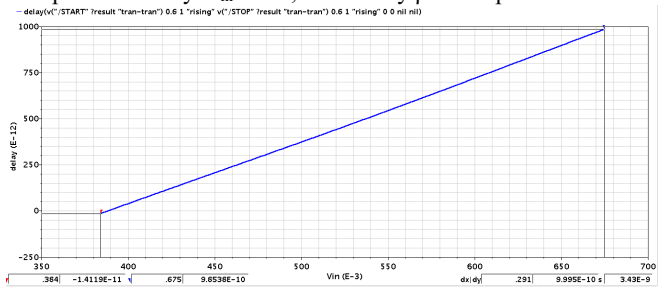


Fig. 10. Plot of delay versus V_{in}.

To calculate the ENOB we have entered a sine-wave with frequency 30 MHZ over a period of cycle, we can see in figure 11 the input signal, the signal after sample and hold and the reconstructed signal. We can see that the reconstructed signal is so close to the signal after sample and hold. We got ENOB of 7.6 bits.

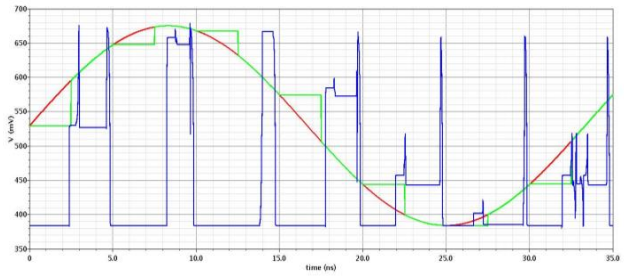


Fig. 11. Input signal, sampled Vin and digital output.

Table 1 shows the performance of the proposed TADC compared to other ADCs.

Point of comparison	This work	[3]	[4]	[5]	[6]
CMOS Technology	65 nm	180 nm	65 nm	90 nm	130nm
ENOB	7.6	5.6	5.6	8.69	6.2
Sampling Rate (GS/s)	200 MS/s	220 MS/s	500 MS/s	150 MS/s	120 MS/s
Number of Bits	8	6	6	9	8

Table 1

VI. CONCLUSIONS

The time-based ADC employs a completely different architecture from the conventional ADC and quantizes time at predefined amplitude intervals. An 8-bits 200 MS/s TADC based on highly linear VTC and two levels Vernier delay line was introduced, a dynamic range of 291mV and sensitivity of 3.43ps/mV are achieved in VTC . Also, a resolution of 3.9ps has been achieved in TDC. The proposed VTC achieved high linearity in large dynamic range and The two level VDL in TDC reduces the required number of delay elements and D-flip-flops. The two level VDL outputs are a two thermometer codes (one for the coarse and one for the fine) which converted to a binary output using the proposed READ OUT circuit over two stages. The ENOB=7.6 bits for input sine-wave frequency equals 30MHz.

VII. Acknowledgment

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