A New 16-bit Low-Power PVT-Calibrated Time-Based Differential Analog-to-Digital Converter (ADC) Circuit in CMOS 65nm Technology

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***Abstract*—Time-Based Analog-to-Digital Converter (ADC) becomes the key of the new era of scaling CMOS technology. It provides a lower power and area than conventional ADCs. These improvements urges the Time-Based ADC to overcome Software Defined Radio (SDR) receivers' challenges and to be a dominant module in designing them. Such an SDR receiver can adapt itself automatically to deal with the desired bandwidth. This permits more technologies to be built-in the same single chip. Time-Based ADC includes a Voltage-to-Time Converter (VTC) and a Time-to-Digital Converter (TDC).**

In this work, we present a novel differential VTC simulated under process-voltage-temperature (PVT) variations using TSMC 65nm CMOS technology. It is connected with a TDC algorithm implemented on MATLAB to form a complete ADC. The proposed ADC is based on a new design methodology which reports at higher input frequencies after calibration a higher Effective-Number-of-Bits (ENOB) than previously published ADC circuits in TSMC 65nm CMOS technology, with a supply voltage of 1.2V.

***Index Terms*—Nanometer CMOS technology; software defined radio; voltage-to-time converter; VTC; TDC; time-to-digital converter; PVT variations; calibration techniques; effective-number-of-bits; linearity; differential design.**

I. INTRODUCTION

Currently, the stream of scaling CMOS technology pervades all academia and industrial fields. This cutting-edge technology overcomes the main problems resulted from using conventional Analog-to-Digital Converters (ADCs) [1] in such applications. Actually, a single integrated circuit chip is proposed to have several chains of receiving and transmitting blocks for various wireless standards, due to the capacity of demands. As a result, the power consumption of the built-in electronics increases rapidly. This induces applications such as Software Defined Radio (SDR) receivers to arise [1] in which, the aimed chain could be configured and controlled.

Technology scaling of deep submicron CMOS makes the ADC design more sophisticated, as it reduces the supply voltage which results in degrading the signal-to-noise ratio due to the decreased headroom level of the signal [2]. In high frequencies, the voltage resolution of analog signals is smaller than the time resolution of the digital signals. Consequently, the ADC digital part percentage will be increased using digital CMOS technology to solve analog problems and produce high-speed ADCs.

In Time-Based ADC, by modulating the input signal edges, the analog signal amplitude is sampled and converted into a pulse in time-domain. Then this pulse is quantized into a digital output. Using a Voltage-to-Time Converter (VTC) and a Time-to-Digital Converter (TDC), the Time-Based ADC can perform this operation, respectively as shown in Fig. 1. Depending on whether the delay is applied to one or both edges of the clock pulses, the VTC is referred to as either a Pulse Width Modulator (PWM) or Pulse Position Modulator (PPM) [2].

Several ADC circuits have been introduced in the literature [1]–[3]. All previously published circuits are facing several limitations and design trade-offs. On the other hand, there are significant advantages to the differential design. First, the differential input provides a doubling to the signal amplitude resulting in a 6-dB SNR improvement. Second, the common-mode noise will be suppressed. Third, the even-order harmonic distortion components caused by the non-linearity of a single-ended ADC will be omitted. Superb results are achieved in linearity and Effective-Number-of-Bits (ENOB) at reasonable expense of extra area/ power overheads, by gathering all these advantages from the usage of lower technology nodes till this novel.

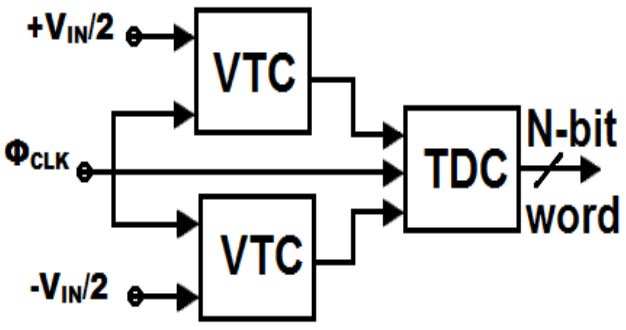

Fig. 1. The proposed time-based ADC architecture.

II. Proposed Methodology and Analysis

Each core of the proposed differential design methodology of the VTC circuit consists of 2 main blocks. The pull-up block controls PPM VTC output falling edges, while the pull-down block controls PPM VTC output rising edge resulting in a PWM VTC. For a differential design, the applied input voltage for each VTC core equals to $\pm V_{IN}/2$. The mode of operation has been discussed in [4]. Fig. 2(a) represents the pull-down block design of the single core.

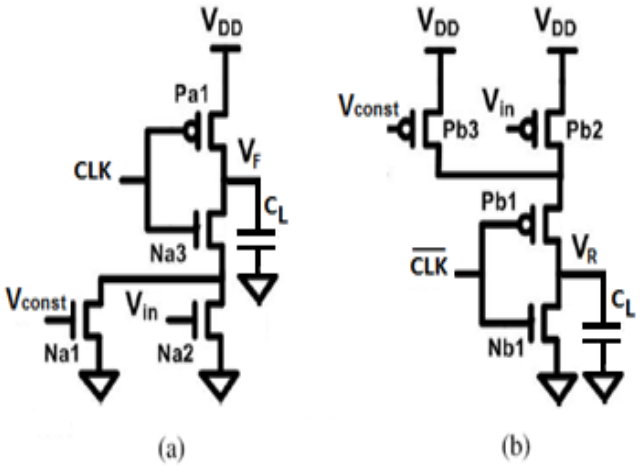

Fig. 2. Circuit schematic of the single-ended VTC. (a) Rising VTC circuit. (b) Falling VTC circuit

The Na1 transistor is used to limit the flowing current in saturation mode, in case of lower V_{IN} values. Its width should be much less than Na2 transistor, so it will have a high resistance. This makes the current flow easily through Na2 which has a higher size. Same procedure is done for the pull-up block design of the single core which is portrayed in Fig. 2(b) where the Pb2 width is greater than Pb3 width.

To have a maximum dynamic range, the single core design is based on the complementary behavior between the pull-down block and the pull-up block of a single VTC circuit. It has an inverted delayed clock using a large-sized inverter for the pull-up block. This delay helps in producing a high linear output as the output pulse equals to $\Delta + T_R - T_F$. Where Δ is the inverter delay which should be high to have a positive delay after subtracting the value of T_F; T_R is the rise delay of the pull-up block in which we minimize Pb2 width for a slow operation; and T_F is the fall delay of the pull-down block in which we increase Na2 width for a high discharging rate of the load capacitor. The XNOR gate is used to get the difference between T_R and T_F.

The following stage of the proposed VTC design is the TDC block. It is implemented using MATLAB. It takes the differential output value and generates a logic '1', if this value is greater than the average VTC output pulse width. Otherwise, we have a logic '0'. This algorithm will be repeated till we reach the final sample. A real TDC block is the main current research to suit the differential VTC output.

III. Calibration Techniques

A manual calibration technique is achieved while doing the circuit design in order to get the optimal bias conditions of the proposed design. They have been selected using a manual calibration technique by which the largest linear range can be achieved. A dynamic calibration technique is experienced by adapting the input DC voltage of each core design for specific values. Variations can be tolerated which are resulted from: corners (i.e. slow NMOS and slow PMOS, fast NMOS and fast PMOS) which change the normal carriers' mobility to be faster/slower; temperature which affects the flowing current of each transistor; and finally the supply voltage which could make NMOS/ PMOS transistors operate at deep regions (saturation/ triode) instead of normal ones. These calibration voltages can be supplied by a set of programmable digital-to-analog converters (DACs). Their implementations are also in progress. This could also result in reasonable larger power/ area expenses.

IV. Conclusion

In this work, a novel highly-linear ADC circuit is proposed which achieves the highest FOM and ENOB and the lowest area and power to date. The ingenuity of this design is emanated from the following speculations. First, the power of CMOS technology which provides a less-area low-power high-speed design is utilized. Second, this work depends on the differential mechanism which magnified the linear range and omitted the undesirable noise. Third, a new VTC design methodology which outputs a highly-linear pulse width is proposed. Then, a unique MATLAB algorithm which represents a PWM TDC functionality is implemented. Finally, a proposed calibration circuit to tolerate the PVT variations is experienced. The achieved results of the new ADC circuit are: a 4GS/s sampling speed, 13.5b ENOB, a 1.42mV dynamic-range, a 229μm^2 area, a 0.2mW power and a 8×10^{-19}J/conversion FOM. A practical programmable DAC and TDC circuit have been implementing to finalize this work that can be highly used in the SDR application.

V. ACKNOWLEDGEMENT

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