

A Comparative Analysis of Optimized Low-Power Comparators for Biomedical-ADCs

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Abstract— Comparators are essential blocks in implementing analog-to-digital converters (ADCs). An energy-efficient ADC such as successive approximation register (SAR) ADC or dual-slope ADC requires at least one comparator, where the power consumption mainly depends on the comparator design. This paper investigates various implementation techniques of low-power comparators emphasizing on their design performance metrics, and trade-offs such as sampling frequency, resolution, and power consumption. The proposed comparative analysis covers a recently published low power comparators for bio-signals monitoring and proposes a basic optimization method for these comparators. These comparators are redesigned using UMC 130nm CMOS technology for a fair comparison to present a good reference for proper choosing of a low power comparator that serves low-power bio-medical applications.

Keywords— low-power design, latched comparator, pre-amplifier, SAR ADC, Dual-Slope ADC.

I. INTRODUCTION

Bio-medical applications have significantly increased over the past few years offering a high-quality assistance to those in need. The main purpose is expressed as receiving analog signals from various parts of the human body, then processing them digitally to be able to work with them using all the latest technology in Digital Signal Processing (DSP) [1]. Thus, the need for energy-efficient analog-to-digital converters (ADCs) is emphasized as it constitutes a primary building block of such systems.

The comparator is a vital building block in the ADC design. The comparator's output is either single-ended or fully differential, depending solely on the design hierarchy. Therefore, the overall performance of an energy-efficient ADC depends on the comparator design, since it dominates many parameters such as the sampling frequency, resolution, and power consumption of the ADC. One of the proposed comparator architecture for low power ADC design is dynamic latched comparators, where a pair of back-to-back cross-coupled inverters is used to convert a small input voltage difference to a full-scale digital level in a short time. The accuracy of such comparators is dominated by the random offset voltage resulting from the device mismatches such as the internal parasitic/external load capacitance mismatches, and threshold voltage (V_{th}) [2–4]. Therefore, the offset voltage has a crucial influence on the performance of dynamic latched

comparator. To reduce the offset voltage of such comparator, a pre-amplifier is used as an input stage for the dynamic latched comparator. However, the pre-amplifier based comparators suffer from both the reduced intrinsic gain with a reduction of the drain-to-source resistance (r_{ds}) due to the continuous technology scaling and the large static power consumption for a large bandwidth [5].

This paper introduces a comparative review and analysis of different comparator architectures recently published in the literature. Also, a method is proposed to optimize the performance metrics for higher resolution, lower power consumption, and lower implementation area. The rest of the paper is organized as follows. In Section II, the design and analysis of the different comparators architectures are presented, followed by the simulation results in Section III. Finally, a conclusion is derived in Section IV.

II. COMPARATOR ARCHITECTURES

In this Section, different low power ADC architectures are discussed. Then, followed by comparator architectures which are classified based on (1) latched or not, (2) differential or single-ended, and (3) pre-amplifier based or not, to achieve the required specifications based on the application are presented.

A. SAR ADC

SAR ADC is one of the ADC architectures that benefit from the CMOS technology scaling. This feature is due to the fact that they mainly comprise digital circuits. Furthermore, other ADC architectures may need high-gain operational amplifiers that provide proper linearity as well as wide bandwidth to ensure that the linearity is maintained over the desired frequency spectrum. SAR ADCs do not require such amplifiers, not including pre-amplifiers, which means that scaling the technology does not affect this architecture undesirably like other architectures. As the required amplifiers for ADC architectures other than SAR ADC's tend to be problematic as the technology is downscaled [6].

Fig. 1 shows the typical implementation of successive approximation ADC. As evident in this figure, successive approximation ADC consists of a comparator, a DAC, and

a successive approximation register, denoted by SAR. SAR ADC is based on a binary search algorithm, and thus is more energy efficient than other ADC architectures which use a brute force approach to perform data conversion [7].

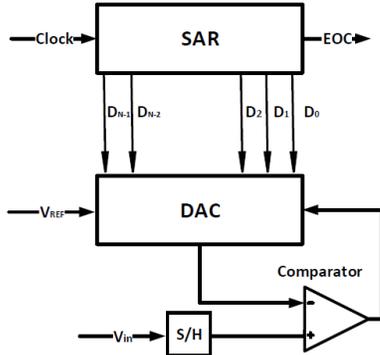


Fig. 1 SAR ADC Block Diagram

Fig. 2, shows the circuit schematic of the implemented pre-amplifier based dynamic latched comparator, where the transistors (M_4 , and M_5) are the amplifying transistors controlled by the CLK as well as M_1 . This comparator works in two different modes: 1) Pre-Charging Phase, where the output nodes (D_p , and D_n) are pre-charged to VDD. 2) Evaluation Phase: (a) If V_{in}^+ is greater than V_{in}^- , then the load capacitor at M_3 will discharge faster than that at M_2 until it reaches the threshold voltage of M_{11} causing it to turn off. Therefore, the outputs D_n is '0', and D_p is still '1'. (b) If V_{in}^- is greater than V_{in}^+ , then the load capacitor at M_2 will discharge faster than that at M_3 , until it reaches the threshold voltage of M_{10} causing it to turn off. Therefore, the outputs D_p is '0', and D_n is still '1' [8].

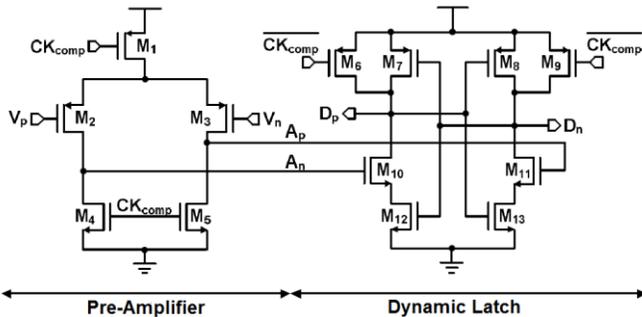


Fig. 2 Circuit Schematic of optimized comparator [8]

For the pre-amplifier design, A PMOS input pair is used, as it can operate over a wide common-mode voltage ($V_{cm,in}$) range. While the first stage voltage gain is approximately 6 on average, when the second stage takes over the amplified value, it dramatically reduces the second-stage performance requirement even though $V_{cm,in}$ is varying [9].

B. SAR ADC with Bypass Window

Fig. 3, shows the proposed SAR ADC in [10], where it proposes that a predefined window voltage would act as a means to skip some comparison steps. Hence, this reduces the switching activity and the power consumption of the ADC. The algorithm is as follows: 1) Binary weighted voltages are added

to or subtracted from the differential voltage on the two DAC's in each comparison/conversion step. 2) A pre-defined window voltage is compared to the differential voltage in each step. This window works as following: (a) If the differential voltage is smaller than the window voltage, then the control logic skips to the step that corresponds to the chosen window voltage. (b) If not, the control logic follows the aforementioned monotonic switching scheme. Moreover, the smaller the window size used; the more steps that can be bypassed, but the less likely for input to be less than the window voltage. However, this forces the designer to choose a suitable window voltage depending on the application and the input parameters. The use of an asynchronous control circuit helps reduce the power consumption as well. It is proposed to use a once-triggered DFF in the asynchronous phase generator as an extra measure to reduce the consumption. Advantages of such techniques are: (1) Skipping steps helps reduce the error accumulation, (2) Bypass window tolerates the DAC settling time, and the comparator offset voltage, and (3) It suppresses the peak DNL and INL.

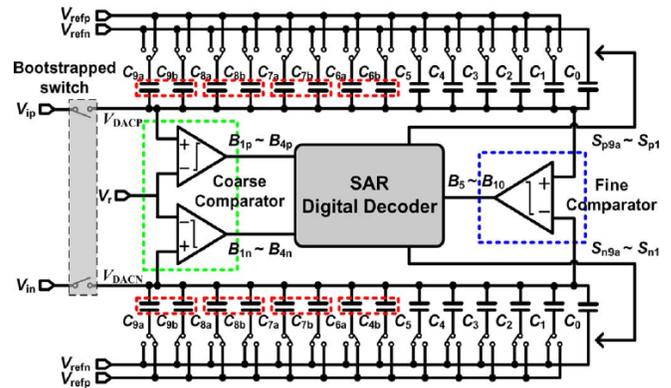


Fig. 3 SAR ADC proposed in [10]

Fig. 4 shows a schematic of the optimized pre-amplifier with an embedded regenerative latch, where the bypass window scheme uses two coarse comparators and a fine one. The three of them have the same design but with the coarse comparators having transistors with doubled W/L ratio compared to the fine one. Therefore, the fine comparator accounts for 3.4% of the consumption while the coarse comparators account for 6.8%. The used NMOS input pair tries to minimize the number of cascaded transistors as possible for low voltage operation. The comparator operation starts with a reset state when the signal Clc is low. In the reset state, the outputs are pulled down. When Clc becomes high, this is called regeneration state, where the comparator decides which input terminal has the highest voltage because when Clc is high, M_4 , M_4 , M_6 , and M_7 are off while M_3 is on. The higher input voltage drives down the drain of its input transistor faster than the drain of the other input transistor. Once, the turn-on voltage (threshold) is reached for either M_5 or M_6 , the drain of the input transistor of the lower input voltage is pulled to VDD. This makes sure that the other PMOS of M_5 or M_6 is off. The comparator latches to this configuration of on and off devices. In the end of the

evaluation state, the input terminal with the higher voltage causes its corresponding output node to rise high [10].

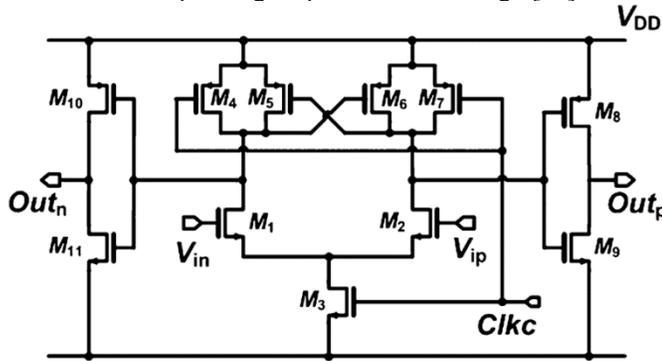


Fig. 4 Circuit Schematic of optimized comparator [10]

Comparators suffer from three non-idealities: offset, thermal noise and kickback noise. First, offset voltage can be problematic especially in the coarse comparators as they have different input loading, but this can be ignored as shown in [10]. Since the two comparators can tolerate the offset. Second, thermal noise is ignored, as the large sizing of the input pair reduces it. Finally, the kickback noise results from glitches due to the coupling of the transient change of internal nodes in the comparator. As different loading on the two input terminals can cause kickback noise to manifest as an offset.

C. Multiplying SAR ADC

For DSP of the biopotential signals, N-tap finite impulse response (FIR) filter is required. This N-tap FIR filter requires N-multipliers, so integrating the multiplication process within the ADC system has a significant influence in saving extra area as well as reducing power dissipation. As shown in Fig. 5, a multiplying SAR ADC as introduced in [11], where the implemented ADC is an 8-bit charge redistribution SAR multiplying ADC (MADC). The multiplying DAC (MDAC) utilizes a split capacitor array to minimize the overall area of the binary capacitor array. It multiplies two digital values at the expense of a small overhead of three two-input logic gates per bit. Therefore, the implemented ADC can be configured in either raw data analog-to-digital conversion or FIR filtering.

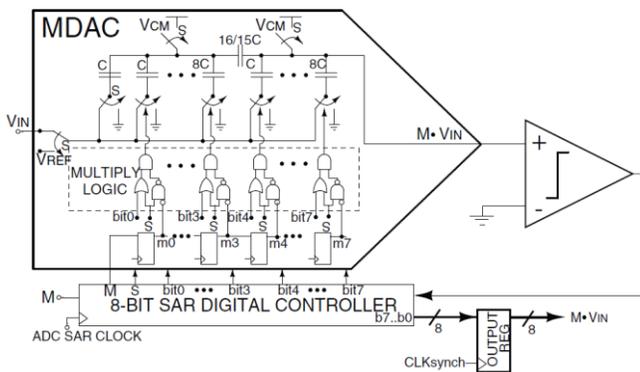


Fig. 5 Multiplied SAR ADC proposed in [11]

The comparator shown in Fig. 6 utilizes two stages with offset correction followed by a level-shifter and digital buffers. Where the preamplifier stage uses fully differential PMOS pair

with a cross-coupled load that reduces the input referred offset voltage of the comparator stage. The input pair stage is sized to make the transconductance (gm) of the input differential pair higher compared to the gm of the cross-coupled transistors, to avoid saturation of the cross-coupled transistors. After, this pre-amplifier stage, an offset correction circuit through setting threshold voltage (Vm) is placed. Finally, a level shifter stage is used to maintain rail-to-rail voltage.

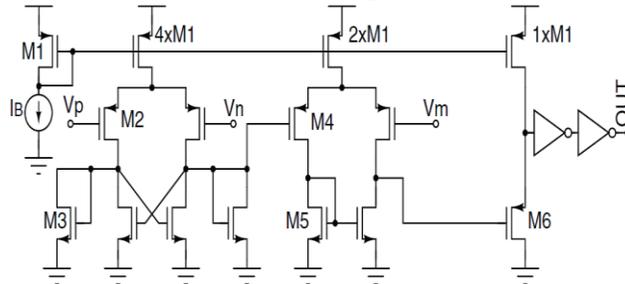


Fig. 6 Circuit Schematic of optimized comparator [11]

D. Dual-Slope ADC

As shown in Fig. 7, a simplified block diagram for dual-slope ADC. Dual-Slope ADCs are used for high accuracy and low data rate applications like digital multimeters which are also known as Avometer. It is named dual-slope ADC, as it performs conversion through two phases: During the first phase has a fixed duration $T1$ controlled by the running of a counter for 2^N clock cycles. During this period, the integrator input is connected to the analog input sample, and the integrator output starts to build up, where the integrator output can be expressed by [7]:

$$V_{out} = \frac{V_{in} \times T1}{RC}$$

While during the second phase, the input of the integrator is switched to the reference voltage V_{ref} . Therefore, the slope is fixed during this phase, unlike the first phase which has variable slopes, resulting in a variable duration $T2$ for the second phase. The integrator output starts to go down until it reaches zero, where $T2$ can be expressed by [7]:

$$T2 = \frac{V_{in} \times T1}{V_{ref}}$$

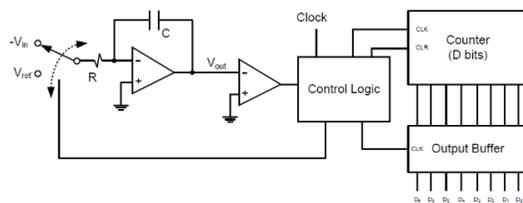


Fig. 7 Dual-Slope ADC [7]

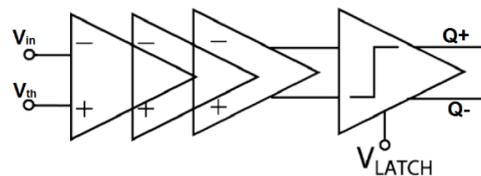


Fig. 8.a Block Diagram of the optimized comparator [11]

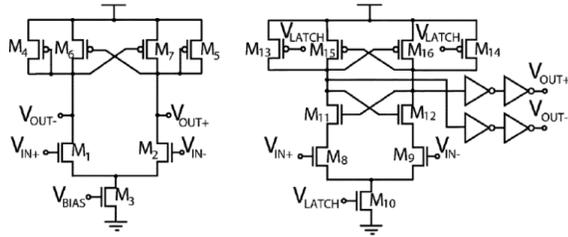


Fig. 8.b Circuit Schematic (i) one of the three identical gain stage, and (ii) Dynamic latch [11]

As explained before, the comparator shown in Fig. 8 uses a preamplifier stage that decreases the effect of offset voltage error due to device mismatch and also reduces the disturbance due to kick back noise. A cross-coupled active-load PMOS acts as a load for the input differential pair. The concept of positive feedback is used to generate negative resistance and compensate some positive resistance to enhance the DC gain. While the second of this comparator is composed of a dynamic latch that is similar to the proposed latch in subsection A.

III. SIMULATION RESULTS

In this section, all the previous comparator circuits are simulated using hardware-calibrated UMC 130 nm CMOS technology under the same environment to guarantee fair comparison as listed in Table I.

The proposed modifications are as follows:

- The different comparator architectures are optimized on gate level through setting a more accurate aspect ratio to achieve a lower power consumption.
- For [8], the comparator power consumption decreases by changing the $V_{cm,in}$ to fit the required input dynamic range. Therefore, the power consumption optimization rate is only 12 % not as high as other architectures.
- For [10], the comparator power consumption decreases by 20 % due to technology scaling as shown in Table I.
- For [11], the power consumption can't be further optimized. However, the operating frequency is doubled, while keeping the power consumption at the same level.
- For [12], optimizing the power consumption by 37 % through removing the output buffers. Since the output real-to-real voltage is obtained with no need for extra-buffers.

IV. CONCLUSION

In this paper, several architectures of low-power comparators are optimized and simulated using the same technology and the same environmental conditions to guarantee fair comparison. The comparison that serves energy-efficient ADCs for bio-medical recording shows several ADC

architectures as well as many comparator topologies whether differential or single-ended output, low speed as well as moderate speeds for different input ranges. The comparison emphasizes the effect of resizing the used comparators by optimizing the aspect ratios for reducing the power consumption. However, the operating frequency is improved, but not for all designs. This work will help comparator-based bio-signal recording systems designers to select the comparator design that meets their power budget and throughput requirements.

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REFERENCES

- [1] A. P. Chandrakasan, N. Verma, and D. C. Daly, "Ultra low-power electronics for biomedical applications," *Annu. Rev. Biomed. Eng.*, vol. 10, pp. 247–274, Aug. 2008.
- [2] J. He, S. Zhan, D. Chen, and R.L. Geiger, "Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 56, pp. 911–919, May 2009.
- [3] A. H. Hassan, M. M. Aboudina, and M. Refky, "A low-power high-speed charge-steering comparator for high-speed applications," *14th IEEE International New Circuits and Systems Conference (NEWCAS)*, pp. 1–4, 2016.
- [4] A. Nikoozadeh and B. Murmann, "An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 53, no. 12, pp. 1398–1402, Dec. 2006.
- [5] B. Murmann, P. Nikaeen, D. J. Connelly, and R. W. Dutton, "Impact of scaling on analog performance and associated modeling needs," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2160–2167, Sep. 2006.
- [6] B. R. Gregoire and U. Moon, "An over-60-dB true rail-to-rail performance using correlated level shifting and an opamp with only 30 dB loop gain," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2620–2630, Dec. 2008.
- [7] M. Amin, *Design of a Time Based Analog to Digital Converter*. Ph.D. thesis, University of Waterloo, 2012.
- [8] H. Lee, S. Park, C. Lim, and C. Kim, "A 100-nW 9.1-ENOB 20-kS/s SAR ADC for Portable Pulse Oximeter," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 62, no. 4, pp. 357–361, April 2015.
- [9] M. van Elzakker, E. van Tuijl, and G. Paul et al., "A 10-bit charger distribution ADC consuming 1.9 Wat 1MS/s," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1007–1015, May 2010.
- [10] G.-Y. Huang, S.-J. Chang, C.-C. Liu, and Y.-Z. Lin, "A 1- μ w 10-bit 200-ks/s sar adc with a bypass window for biomedical applications," *IEEE J. of Solid-State Circuits*, vol. 47, no. 11, pp. 2783–2795, 2012.
- [11] K. Abdelhalim, L. Kokarotseva, J. L. Perez Velazquez, and R. Genov, "915-MHz FSK/OOK Wireless Neural Recording SoC With 64 Mixed Signal FIR Filters," *IEEE J. of Solid-State Circuits*, pp. 2478 – 2493, July 2013.
- [12] H. Mazhab-Jafari, L. Soleymani, and R. Genov, "16-channel CMOS impedance spectroscopy DNA analyzer with dual-slope multiplying ADCs," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 5, pp. 468–478, Oct. 2012.

TABLE I
Comparison between different Comparator architectures

Design Parameter	[8]	Optimized 8	[10]	Optimized 10	[11]	Optimized 11	[12]	Optimized 12
Technology Process	110 nm	130 nm	180 nm	130 nm				
Supply Voltage	1 V	1V	0.6 V	0.6 V	1.2 V	1.2 V	1.2 V	1.2 V
Architecture	Differential	Differential	Differential	Differential	Single-Ended	Single-Ended	Differential	Differential
ADC Architecture	SAR	SAR	ByPass SAR	ByPass SAR	MSAR	MSAR	Dual Slope	Dual Slope
LSB	N/A	5 mV	N/A	0.5 mV	N/A	1 mV	N/A	1 pV
Input Clock Freq.	20 KHz	20 KHz	200 KHz	200 KHz	57 KHz	100 KHz	100 MHz	100 MHz
Comparator Power	20 nW	17.6 nW	85 nW	68 nW	1.5 μ W	1.5 μ W	19 μ W	11.9 μ W