

A Tunable Multi-band/Multi-standard Receiver Front-End Supporting LTE

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Abstract— Current wireless communication devices demand multi-band/multi-standard receiver that can access all the available services specifications. This work introduces a tunable receiver front-end for multi-band multi-standard applications. The receiver adopts a down-conversion quadrature band-pass FIR charge sampling mixer tuned via its controlling clocks. A time varying impedance matching network provides further selectivity. The architecture is simulated over three different frequencies spanning two octaves (2G, 1G and 500MHz) targeting LTE specifications. The proposed design is tested across process corners and post layout. Simulations result in Noise Figure of 7.5 to 9 dB, out-of-band IIP3 of -1.9 to -7 dBm, in-band IIP3 of -1.5 to -10 dBm and S11 <-10dB. The design is implemented using 65nm CMOS technology

I. INTRODUCTION

The number of cellular bands in mobile handset's wideband receiver front ends has grown significantly. Conventional receivers require a large number of bulky passive band select filters. Typical components such as Surface Acoustic Wave (SAW) and passive LC matching network of inductors and capacitors are inherently narrow-band and hard to tune. Filtering limits out-of-band blockers and thus relaxes linearity requirements. Eliminating the narrow-band channel select filters hence sets stringent requirements on receiver's linearity. Sampling receivers [1,2] and wide-band receivers using wide-band LNAs [9] are proposed solutions for multi-band multi-standard receivers; however they have moderate linearity and poor matching. A tunable receiver front-end is proposed in this paper. A tunable quadrature band-pass charge sampling filter forms the signal path. It down-converts the signal to intermediate frequency (IF), subsamples the signal relaxing the requirements of the analog to digital converter (ADC), and provides tunable filtering through adjusting the controlling clocks. A time varying matching network based on impedance translation technique provides a tunable matching and additional selectivity improving the receiver's linearity [3, 4]. Controlling the sampling filter and matching network driving clocks determines the frequency at which the band-pass filtering response and matching are held. This guarantees high linearity, good matching, and low noise figure at the desired frequency. The paper is organized as follows; Section II introduces the proposed architecture, Section III discusses the band-pass sampling filter. Section IV describes the time varying matching network. Section V shows the layout. Section V presents the simulation results and discusses the merits of the proposed architecture over other architectures.

II. Front End Architecture

The proposed RF receiver front-end architecture is shown in Fig.1. It is composed of two parallel paths; the band-pass filter and the matching network. The filter down-converts the signal with providing high linearity, gain and low noise figure. It is composed of a transconductance amplifier converting the input differential RF input signal to differential currents which is integrated on the sampling capacitors. A time varying matching network is used for tunable matching and selectivity enhancing the receiver's linearity. It is composed of controlled switches and base-band resistances and capacitances. According to the targeted frequency, the design's controlling clocks are adjusted.

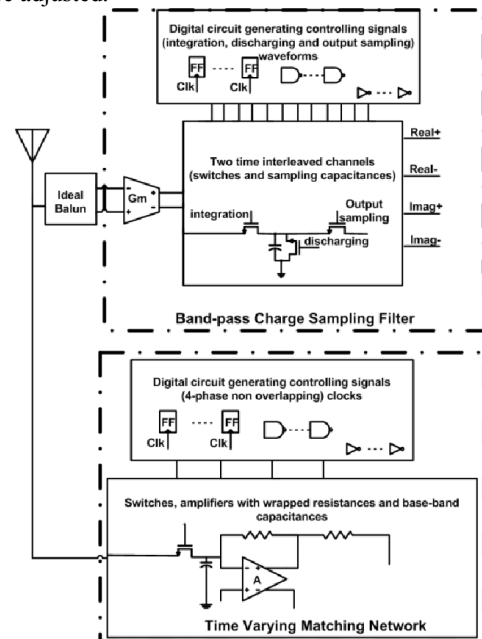


Fig.1 The proposed receiver front-end architecture

III. The Band-Pass Sampling Filter

Integrating current on a sampling capacitor on a certain time interval then sampling the resulted voltage to the output gives a sinc filtering response with notches at $(1/T_i)$. Where T_i is the integration time of one current sample. The capacitor is discharged after sampling the resulted voltage to the output.

The filter transfer function is shown in (1), where G_m is the transconductance and C_s is the sampling capacitance [5].

$$H(f) = |H_{SINC}(f)| = \frac{G_m}{C_s} \left| \frac{\sin(\pi f T_i)}{\pi f} \right| \quad (1)$$

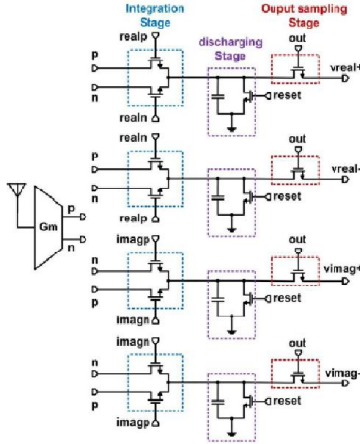


Fig.2 Band-pass charge sampling filter channel

Integrating successive sequences of $+1, +j, -1$ and $-j$ results in a quadrature band-pass filter centered at $(1/4T_i)$ with notches at $(1/NT_i)$, where N is the samples number and with a notch at $(-f_c)$ for image rejection [5,6]. This is done by integrating two successive sequence of $+1, 0, -1$ and 0 on real channel and $0, +1, 0$ and -1 on imaginary channels. In addition to the samples integration time (NT_i) , time should be considered for the sampling-to-output and discharging phases, this sets constraints on the minimum sampling time. So two time-interleaved channels are used to place the filter's notches at multiples of the sampling frequency for optimal anti-aliasing filtering effect.

The final time-interleaved filter is shown in Fig.2. The RF input voltage is converted to current by the transconductor then it is integrated on the sampling capacitances. The controlling signals for 2GHz frequency, where T_i is 125 ps are shown in Fig.3a and 3b. Here, 8 current samples are integrated on the sampling capacitance in the integration phase then sampled to the output. By adjusting the integration time (T_i) , the band-pass filter center frequency is maintained at the desired frequency. The resulting band-pass filter down-converts the signal to IF frequency. The integration of several current samples decreases the sampling frequency of the following ADC to $(1/8T_i)$. The charge sampler provides conversion gain (CG) shown in (2), where G_m is the tranconductance and C_s is the sampling capacitance.

$$CG = \left(8 \frac{2\sqrt{2}G_m T_i}{\pi C_s} \right) \quad (2)$$

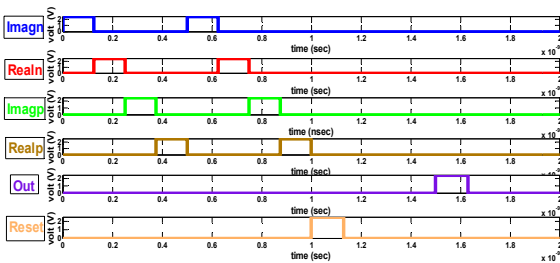


Fig.3a the controlling clocks of the filter first channel

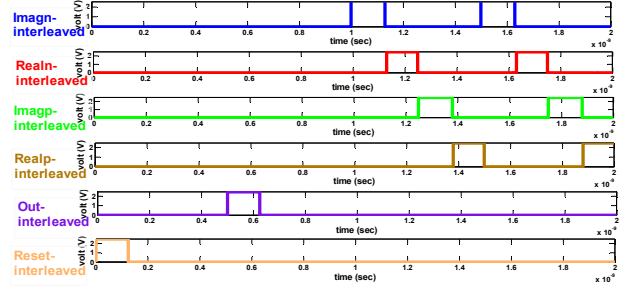


Fig.3b controlling clocks of the filter second interleaved channel

A. Transconductance amplifier

The transconductor is the main contributor in the receiver's gain, NF and linearity. It should supply sufficient integrated current on the targeted frequency range (500MHz-3GHz) for a proper gain according to the desired NF and linearity. It should have high output resistance and low output capacitance to force the current to pass in the integration switches. A low-noise folded cascode transconductor as shown in Fig.4 is used for its high linearity and high output resistance. It consumes 7.5mA.

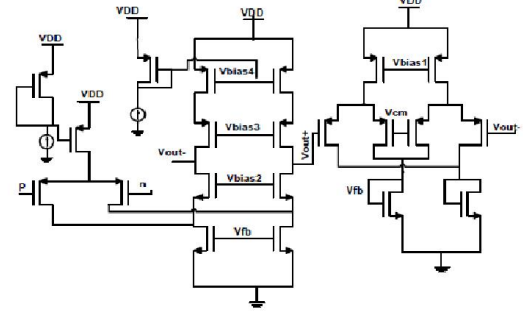


Fig.4 The schematic of the used folded trans-conductor

B. The switches

They are implemented using I/O 2.5V devices for a better linearity and lower switching resistance to force the current to pass in the integration switches. Their W/L is chosen to give a proper low switching resistance with low drain and source capacitance.

IV. Time varying matching network

The matching network idea shown in Fig.5 is based on impedance translation technique [7]. The effect of the resistances and capacitances in the base-band side is translated to the RF side through passive switches. Four-25% duty cycle non-overlapping clocks control these switches. Only one switch is closed at a time and the input voltage is sampled during LO pulse time on the capacitance C_I . The voltage sampled on the base-band capacitance is up-converted to the RF side due to the bi-directional nature of the passive switches. The reciprocal nature of the switches leads to harmonic re-radiation. By virtue of this mechanism, the base-band voltage is remixed with the local oscillator harmonics and re-radiated to the antenna. This reduces the power of the desired signal; these losses can be represented by a resistance in shunt with the base-band resistance.

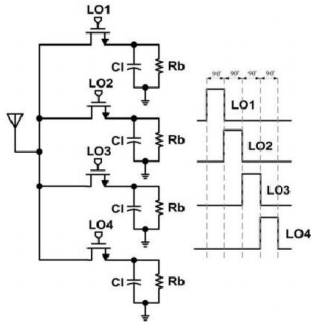


Fig.5 The idea of the time variant matching network

The final input impedance seen by the antenna is represented by a switch resistance in series with a parallel combination of a scaled version of the base-band resistance and the shunt resistance capturing harmonic re-radiation. The base-band resistance is implemented using a resistor wrapped around an amplifier with gain (A) [8]; this configuration decreases the base-band noise contribution. The existence of the capacitance (C1) with the antenna parasitics slightly shifts the S11 notch from the LO frequency. Cross-crossed feed-back resistors (Rfc) are connected from the output of I-channel of the amplifier to the input of Q-channels for the impedance complex part matching [8]. Fig.6 shows the final matching network accounting for real and imaginary parts matching.

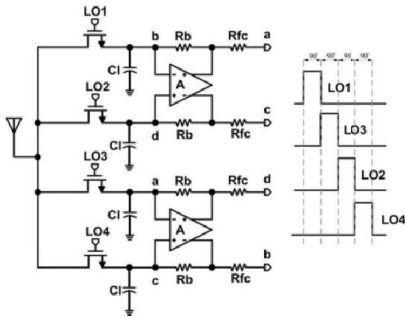


Fig.6 The final time varying matching network

V. Layout

The layout of the whole architecture is shown in Fig.7, it occupies area of 0.45 mm^2 ($870 \mu\text{m} \times 540 \mu\text{m}$). For the transconductor, the design is differential so matching is very important. That's why large width transistors are divided to many fingers and they are inter-digitated. The area of the transconductor is ($116 \mu\text{m} \times 45 \mu\text{m}$). The area of the integration, sampling-to-output, discharging switches and the sampling capacitances is ($307 \mu\text{m} \times 75 \mu\text{m}$). The area of the matching network is ($715 \mu\text{m} \times 217 \mu\text{m}$).

VI. SIMULATION RESULTS

The proposed design is tested over three different frequencies 2G, 1G and 500MHz to prove its programmability through achieving LTE requirements (700MHz- 2.4GHz). The design achieves NF of 7 to 9 dB, out-of-band IIP3 of -1.9 to -5.6 dBm, in-band IIP3 of -1.5 to -5.7 dBm and S11 <-10 dB. It is also tested across process corners and post layout. Post layout results for 1GHz and 2GHz are shown in the following

figures. Fig.8 shows the NF for 1GHz and 2GHz frequencies. NF is due to the addition of the noise of the charge sampler and the matching network; however it is dominated by that of the charge sampler. NF ranges from 7.5 to 9dB at the targeted IF frequency (10MHz).

Linearity specifications are controlled by the transconductor and are enhanced through the matching network selectivity. Fig.9 shows out-of-band IIP3 of -4 to -7 dBm across the tested frequencies. Fig.10 shows in-band IIP3 of -7 to -10 dBm. S11 is <-10 dB as shown in Fig.11 indicating a good matching at the tested frequencies. The proposed architecture pre and post layout results are compared with previous published designs in table I. This work provides programmable front-end that can support multi-frequencies. However, designs [1,10] based on sampling receivers are targeting single frequency. In addition, this work has better linearity due to further selectivity of the time varying matching network also it has better matching and lower power consumption. Wide-band receiver [9] using wide-band LNA has worse linearity and poor matching when compared to this work.

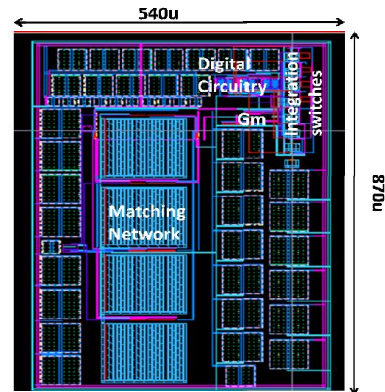


Fig.7 The design layout

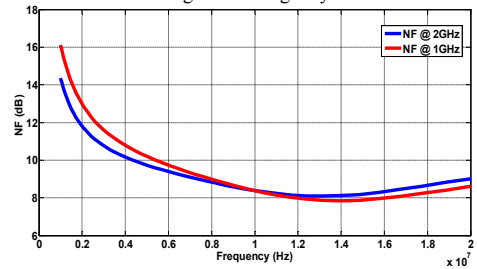


Fig.8 Post layout Noise figure for 1G and 2GHz

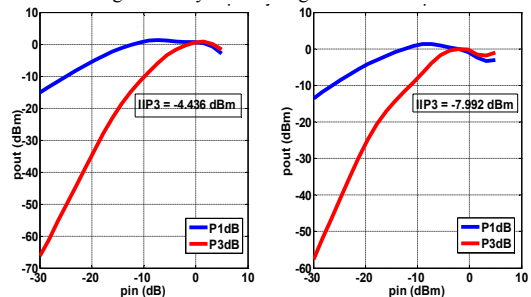


Fig.9 Post layout Out-of-band IIP3 for 2GHz and 1GHz

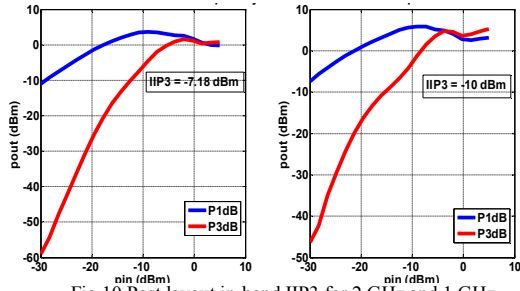


Fig.10 Post layout in-band IIP3 for 2 GHz and 1 GHz

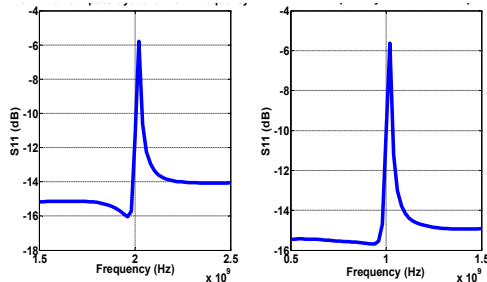


Fig.11 Post layout S11 at 2GHz and 1GHz

The design achieves maximum NF of 9dB, minimum out-of-band and in-band IIP3 of -9 dBm and -12 dBm respectively and minimum S11 of -9 dB when tested across process corners

Table I Performance Metrics Comparison with Existing Designs

Design	Schematic Results	Post layout Results	[1]	[9]	[10]	LTE specs
Frequency (GHz)	0.5→2	1→2	1	0.5-3	2.3	0.7 – 2.7
Gain (dB)	23→28	-	20.2	35	30	-
NF (dB)	7.5→9	7.5→9	7.5	4.5	6	9
Out-of-band P1dB (dBm)	-12→-16	-15→-18	-	-	-14.5	-
Out-of-band IIP3 (dBm)	-1.9→-5.6	-4.4→-7.7	-	-6	-6.6	-10
In-band p1dB (dBm)	-13.5→-18	-16→-20	-14	-	-	-
In-band IIP3 (dBm)	-1.4→-5.7	-7→-10	-5.4	-10	-	-21
S11 (dB)	<-10	-9→-11.5	-8	-	-	-
Power (mW)	9(Analog) + 3(Digital)	10(Analog) + 4(Digital)	18.2(A) + 16.8(D)	28	26.7	40
CMOS Technology (nm)	65	65	65	65	180	

VII. ACKNOWLEDGEMENT

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VIII. Conclusion

The aim of this work is to implement a programmable receiver front-end controlled by adjusting the controlling clocks of the receiver's blocks to be able to receive different frequency bands. By controlling the clocks of the charge sampler (the integration pulse width) and the clocks of the

time varying matching network, the receiver is able to receive a certain frequency band.

This architecture solves the problem of moderate linearity and poor matching in sampling receivers and wide-band receivers.

The receiver achieves better linearity than the other wide-band designs; as in this design the receiver's linearity is controlled by the transistor which is designed with high linearity and is more enhanced by the time varying matching network selectivity.

This design has better matching than other designs. Matching is based on a programmable matching network instead of a wide-band one. Good matching can be held at multi-bands.

By adjusting the number of integrated samples (N), the sampling capacitance (C_s), the receiver's gain is controlled consequently the receiver's noise and linearity.

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