Direct-Elevator: A Modified Routing Algorithm for 3D-NoCs

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***Abstract*—In this paper, a Three-Dimensional (3D) flexible routing algorithm is proposed for generic 3D Network-on-Chip (NoC). The proposed approach, Direct-Elevator, is based on the Elevator-First Algorithm which is independent of the network topology, number of interconnects and placement of interconnects. Direct-Elevator is tailored for 3D-NoC structures, offering a lower communication latency than its predecessor.**

The proposed approach paves the route for finding the optimal configuration of 3D network topology and different hard and soft router implementations for 3D-NoC based Field Programmable Gate Arrays (FPGA).

***Index Terms*—3D technology, NoC, 3D Routing Algorithm, 3D NoC.**

I. Introduction

Three-Dimensional technology which groups multiple chips vertically into a single chip with a die-to-die interconnection, provides wide capabilities for system integration [1]. The 3D-integration offers a promising solution with a significant reduction in the power consumption and delay. It also allows the designer to combine different technologies in one fabrication process [2]. Meanwhile, the new 3D trend introduces new challenges such as different interconnect modeling, thermal management, power delivery, cooling techniques, noise anaylsis and fabrication process comp-atibility [3], [4]. On the other hand, Network-on-Chips (NoCs) offer flexibility, re-usability, and reliability in designing networks which can communicate with many intellectual properties (IPs) through efficient communication protocols [5].

The 3D-NoCs combine the benefits provided by the 3D integration technology and NoCs which results in a significant enhancement in the network performance [6]. As the 2D routing algorithms are not applicable in the third dimension, new 3D routing mechanisms are provided to communicate between the different tiers in the 3D-NoCs. The Through-Silicon Via (TSV) interconnection model which is one of the 3D interconnect approaches, offers the highest density of interconnect of all the other interconnecting approaches, but with a high fabrication cost in return [2]. The performance of 3D-NoCs depends on the number and location of the TSVs. Thus, a routing algorithm which guarantees the flexibility in choosing the number and placement of TSVs is a powerful algorithm [7]. The Elevator-First routing algorithm proposed in [7], is also independent of the dimensions of each tier and the 2D planar topologies. This independence of the shape and size of each tier builds up hierarchical structures of 3D-NoCs. Such flexibility helps to perform variety of future experimental evaluations for the hierarchical structures of the 3D-NoCs. Through these evaluations, a deep analysis can be performed to define the optimal solution for the combination of the network topologies [8], switching techniques and also the count of the TSVs provided in the 3D-NoC.

The paper is organized as follows. In section II, various routing mechanisms for 3D-NoCs are presented. In section III, the Elevator-First algorithm and the Direct-Elevator algorithm are compared to illustrate the differences and the analogy behind each of them. In section IV, the performance analysis between the two algorithms is demonstrated to show the results under various test cases. Section V provides the conclusion of this work.

II. Related Work

Providing new routing mechanisms that can maintain reliability and flexibility offered by 3D-NoCs, is a very challenging research field. Variety of studies adapt new routing schemes for 3D-NoCs. Authors in [9] proposed two routing algorithms for irregular topologies which can be implemented with two different approaches. These algorithms use look up tables for routing the messages over the NoC. In [10], another routing algorithm was proposed, in which virtual channels are used to provide a deadlock free mechanism for irregular networks. This mechanism utilizes compact routing tables to minimize the overhead of the look up tables. The authors in [11] proposed a deadlock and livelock free algorithm. The routing mechanism depends on splitting the network into layers. In [12], a routing algorithm was proposed with lower power consumption and system latency. Other routing schemes are provided for mesh topology only since it is the most popular topology used in the 3D-NoCs [13], [14].

Some studies focus on how to reduce the number of the TSVs to improve the performance. Authors in [8] proposed different 3D topologies in which the number of TSVs is less than other adopted routing algorithms. Mainly, the important aspects that the 3D routing algorithms investigate in are: the number and placement of TSVs in the NoC, the usability of the algorithm for irregular networks, and deadlock and livelock freedom. The authors in [7] provided a routing scheme

called Elevator-First having no constraints on the number or placement of TSVs. The Elevator-First scheme is efficient with irregular networks and it is deadlock and livelock free by using two virtual channels. The study is extended in [15] to provide the implementation of the 3D-router that supports the Elevator-First algorithm. The area overhead of the 3D-router implemented is 8% more than the standard 3D-NoC router with same buffer capacity.

III. The Direct-Elevator Routing Algorithm

The Direct-Elevator algorithm benefits from the advantages and flexibility of the Elevator-First algorithm while optimizing its communication latency. Both distributed algorithms operate on vertically partially connected stacks of 2D topologies.

In the Elevator-First algorithm, adjacent stages are connected through elevator nodes. In order to move a packet from one stage to another, the packet has to go through the elevator node first; hence the algorithm's name. The routing algorithm's logic is distributed over multiple nodes in any tier. To get a better understanding of the algorithm, let's follow a packet path from the source node S1 to the target node D3 shown in Fig.1. Any source issues a packet to destination, it checks whether the destination exists on its tier, accordingly it routes the packet to the destination or the elevator. In case of S1, the destination is on a different tier, hence the packet is forwarded to the elevator E1. Additional information is added to the packet in a temporary header: the elevator's address, a T flag indicating whether the elevator is the final destination and another U flag indicating if the packet will go up or down to the target tier. When the packet reaches the intermediate tier, M acts as the new source and repeats the steps followed by S1. In this scheme, a packet cannot go directly from stage 1 to stage 3; it has to go through multiple nodes in stage 2. The Direct-Elevator algorithm is based on the hypothesis that having smarter elevator nodes connecting the stages will have a positive impact on the communication latency. Those elevator nodes would be able to decide whether the target node exists in their tier or not, then route the packet accordingly.

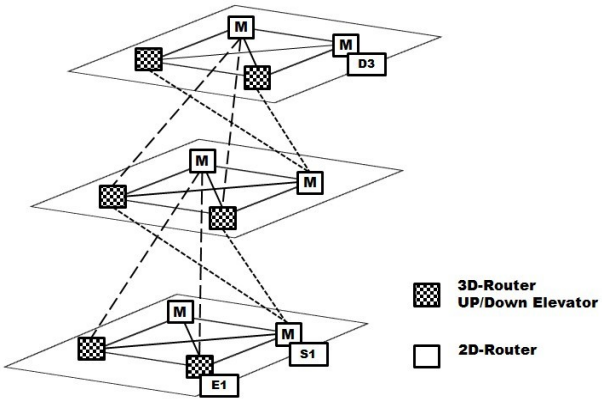

Fig. 1: Elevator-First Algorithm

An example for the Direct-Elevator algorithm is shown in Fig.2. When the source node S1 issues a packet to the target node D3. First S1 adds the elevator address to the temporary header then sets the two flags T and U. The 3D elevator E1 receives the packet and checks the flags then sends the packet to E2. Therefore, E2 resets T flag and checks if the destination node in the same tier or not. If not, it forwards the packet to E3. Otherwise, it routes the packet to D3.

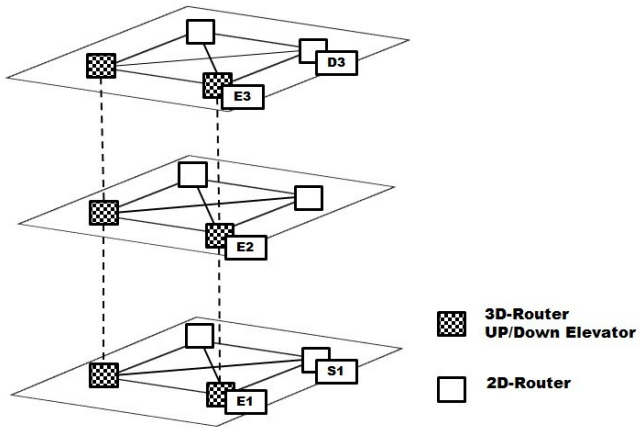

Fig. 2: Direct-Elevator Algorithm

The Direct-Elevator algorithm saves the processing time of adding and removing the 3D elevator address into the temporary header in every tier. So, regardless to where the destination tier is, the adding and removing process of the temporary header is done once.

IV. Performance Analysis and Results

A number of experiments were conducted in order to compare the performance of the Elevator-First and the Direct-Elevator algorithms. Both algorithms are implemented in the same environment to guarantee an efficient and reliable performance evaluation and fair comparison. The two algorithms have been implemented and compiled using C programming language and GNU Compiler Collection (GCC) under Cygwin.

Each experiment measures the throughput of the network in the following cases:

1) Random packet transmission.
2) Transmission over the network's worst path.

The throughput is defined as the number of successful received packets per second, while the worst path is defined as the longest path between two nodes in the NoC.

For each experiment setup the effect of changing the network load, the vertical complexity and the tier complexity on the throughput is measured by varying the number of transmitted packets, the number of tiers and the number of routers per tier, respectively.

A. Network Load

The network load is measured by evaluating the throughput across a range of transmitted packets randomly and over the network's worst path. In these simulations, the number of tiers and the number of routers per each tier is equal to four.
Fig.3 shows the throughput of the two algorithms over a transmitted random packets range which varies from 50,000 to 200,000.

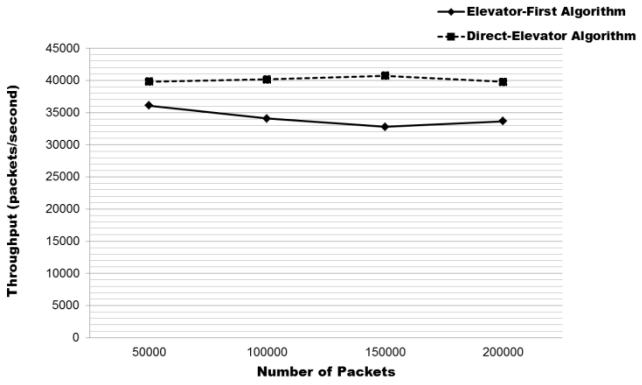

Fig. 3: Throughput Vs. Packets (random test case)

Fig.4 shows the two throughputs over a transmitted packets range over the worst network path which varies from 50,000 to 200,000.

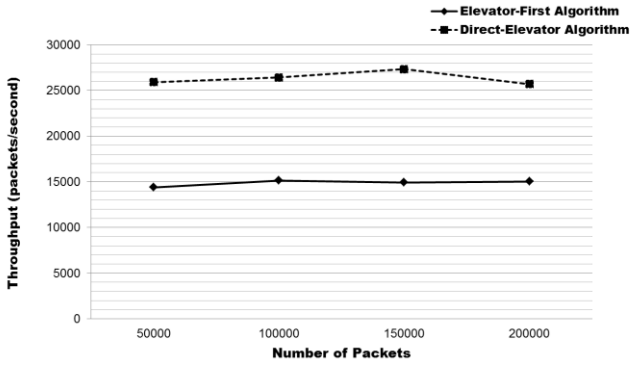

Fig. 4: Throughput Vs. Packets (worst path test case)

In Fig.3 and Fig.4, the throughput of the two algorithms changes slightly over the range of transmitted random or worst path packets. This behavior indicates that tuning the number of packets has no significant effect on the throughput and reflects the performance stability of the two algorithms.

B. Vertical Complexity

The vertical complexity measures the effect of changing the number of tiers in the NoC on the throughput.
Fig.5 shows the throughput of the two algorithms over a range of tiers in the NoC which varies from 3 to 6. In these simulations, the random transmitted packets and routers per tier are 100,000 and 4, respectively.
The throughput of the two algorithms decreases over the range of tiers as increasing the number of tiers results in new longer vertical paths in the 3D-NoC.

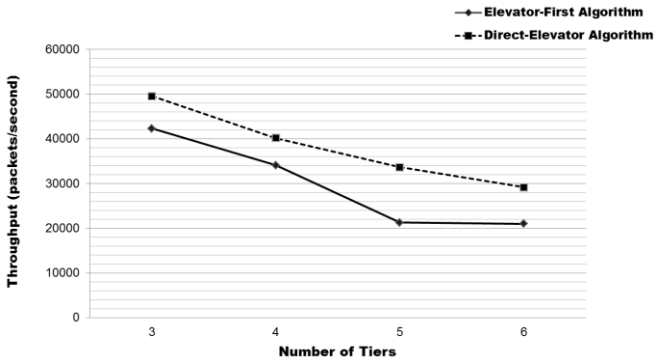

Fig. 5: Throughput Vs. Tiers (random test case)

Fig.6 shows the two throughputs over a range of tiers in the NoC which varies from 3 to 6. Here, the worst path transmitted packets and routers per tier are 100,000 and 4, respectively. The throughput of the two algorithms decreases more than the throughput shown in Fig.5 because in this case the packets are forced to follow the worst path in the 3D-NoC.

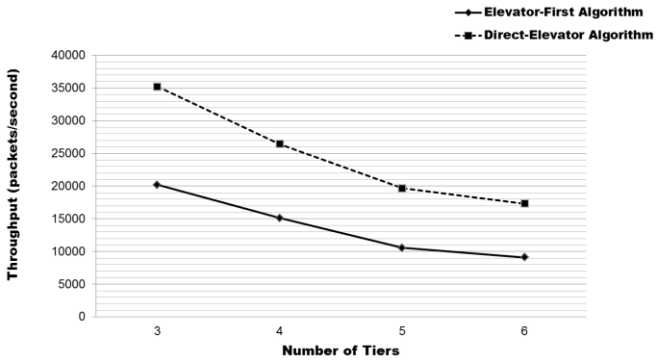

Fig. 6: Throughput Vs. Tiers (worst path test case)

C. Tier Complexity

The tier complexity measures the effect of changing the number of routers per tier in the NoC on the throughput. That can be studied on regular distributed or hierarchical distributed NoCs.

1) Regular Distributed NoC: A regular distributed NoC has the same number of routers in each tier.
Fig.7 shows the two throughputs over a range of routers in the tiers of NoC which varies from 4 to 32. In these simulations, the random transmitted packets and the number of tiers are 100,000 and 4, respectively.
Fig.8 shows the two throughputs over a range of routers per all the NoC tiers which varies from 4 to 32. Here, the worst path transmitted packets and the number of tiers are 100,000 and 4, respectively.

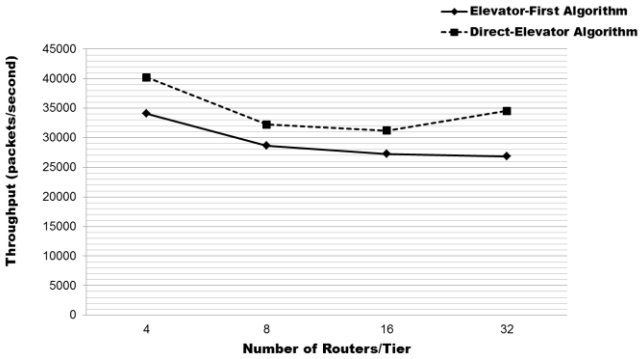

Fig. 7: Throughput Vs. Routers/Tier (random test case)

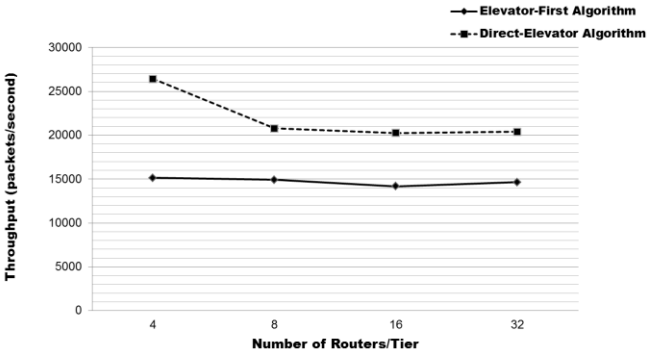

Fig. 8: Throughput Vs. Routers/Tier (worst path test case)

2) Hierarchical Distributed NoC: In the hierarchical structure of a four layered NoC, The routers are distributed as 4 routers in the first layer, 8 routers in the second layer, 16 routers in the third layer and 32 routers in the fourth layer. In the case of transmitting a random sequence of 100,000 packets, the Direct-Elevator algorithm's throughput is higher than the Elevator-First algorithm's throughput by 5.3%. while in the case of transmitting the packets over the network's worst path,the throughput increase is greater than the random packets test case throughput increase by 40%.

V. Conclusion

The experimental evaluations of the Direct-Elevator algorithm show that the throughput of the algorithm is better than the throughput of the Elevator-First algorithm in different 3D-NoCs structures. The Direct-Elevator algorithm saves the processing time taken by the Elevator-First algorithm in the successive operation of adding and removing the elevator address while transmitting the message over the 3D-NoC tiers. The time utilization is better in the case of transmitting packets over the worst path in different combination of tiers per 3D-NoC, transmitted packets and routers per tier. Also, The number and placement of up and down elevators can be adjusted according to the traffic of each application. The Direct-Elevator combines the powerful features of the Elevator-First algorithm, but with better time utilization.

VI. Future Work

The performance evaluation between the Elevator-First and Direct-Elevator algorithms has been performed from the algorithmic throughput prospective. Future evaluations need to be performed to study the differences between the two algorithms for the area and power aspects.

VII. Acknowledgement

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