

A Tunable Receiver Architecture Utilizing Time-Varying Matching Network for A Universal Receiver

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Abstract— This paper presents a digitally controlled RF charge sampling receiver font-end architecture for multiband multi standard RF receivers. A time-varying matching network is proposed instead of traditional ones. The receiver operates in charge domain to produce a band pass Sinc filter centered at the desired local oscillator frequency. A time varying matching network provides tunable matching and selectivity to support multi-bands. This receiver architecture targets LTE band (0.7- 2.7) GHz making use of its programmability. Based on a verilogA model, the receiver conversion gain is 33 dB at 2 GHz; the resulting noise figure is 7.3dB, and P1dB and IIP3 of -10dBm are 0 dBm respectively.

I. INTRODUCTION

High linearity receivers are becoming highly important for multi-band multi- standard receivers and software defined radio applications as there is no band pass selective filter preceding the receiver’s front end, also power matching should be held at many frequency bands. It is typical that a SAW filter precedes the LNA in conventional receivers as shown in Fig.2. SAW filters provide high narrow-band selectivity indeed. However, they are hard to tune to support multi- band applications. Moreover it adds around 1 dB of loss which degrades the noise figure by the same amount. The receiver’s matching network is difficult to be tuned using passive elements.

A straight wideband matching using a 50 ohm resistor shown in Fig.1 increases the receiver’s noise figure with 3 dB due to the reducing the power reaching the receiver. Therefore, noise cancelling frontends became important[1], [2]. Additionally there is no selectivity achieved using 50 ohm as it matches power at all frequencies degrading the receiver’s linearity.

The objective here is to make a tunable high linear receiver front end with tunable matching network and a tunable selective filter more enhancing the receiver’s linearity. RF charge sampling receivers are useful for wideband operation [5] & [6]. However they still need passive components which are hard to tune. In this paper a new charge sampling receiver front end is proposed with a discrete FIR Sinc bandpass filtering sub sampling effect fulfilling the mixing effect and giving gain to the signal. The center frequency of this response is set at the desired local oscillator frequency through adjusting the controlling clocks of the charge sampler. The filter response has notches at frequencies determined by the number of taps of the filter. Multi-band matching is achieved by a time varying matching

network. The rest of this paper is organized as follows: section II discusses the proposed architecture. Section III represents the simulation results; finally a comparison between the proposed architecture and literature architectures is highlighted to show the competence of the new architecture.

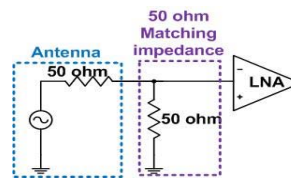


Fig.1 Wideband matching using 50 ohm resistance

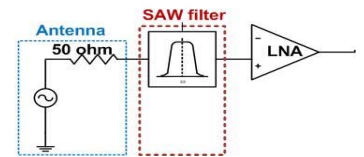


Fig.2 SAW filter preceding the LNA for band selectivity

II. RECEIVER FRONTEND ARCHITECTURE

In the proposed RF sampling receiver architecture, the front end is a quadrature bandpass charge sampling filter. The filter encompasses N-tap complex bandpass finite impulse response (FIR) circuitry. By adjusting the number of taps and the integration time of each sample through adjusting the controlling clocks, the receiver is able to support a certain frequency band. A time varying matching network allows multi-band matching. The block diagram of the proposed architecture is shown in Fig.3.

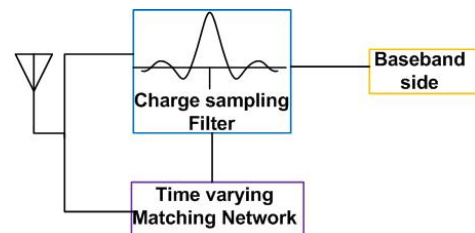


Fig.3 The block diagram of the proposed architecture

A. Time varying Matching Network

The concept of the proposed time-varying matching network is illustrated in Fig.4 [7]. It encompasses passive switches loaded by a baseband resistance (R_b) and a baseband capacitance (C_l). Four-90°-phase-shifted-25%-duty cycle- non overlapping clocks drive these switches. During operation only one switch is closed at a time and the input voltage is sampled during LO pulse time

on the capacitance C_I giving rise to a corresponding voltage on the baseband side. Due to the bidirectional nature of passive mixers, the baseband voltage on the capacitance is up-converted to the RF side at LO pulse time.

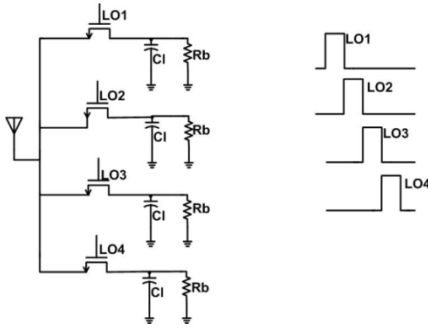


Fig.4 The idea of time varying matching network

Harmonic re-radiation due to the reciprocal switches should be taken into consideration. By virtue of this mechanism, the baseband voltage is remixed with harmonics of the local oscillator and hence reradiated to the antenna. This is more pronounced with our matching network since there is no reverse isolation of a block preceding the network. Harmonics re-radiation reduces the power of the desired signal; such losses can be represented by a resistance in shunt with the baseband resistance. As the number of these harmonics increases, the shunt resistance decreases and becomes more impactful. Finally the input impedance is represented by a switch resistance in series with the combination of a scaled version of the baseband resistance and the shunt resistance capturing harmonics re-radiation. Here the baseband resistance is implemented by using a resistor which is wrapped around an amplifier (A) [8]; this decreases the contribution of the noise generated from the baseband resistance. In essence, the baseband side consists of a resistance in parallel with a capacitance. The presence of this capacitance (C_I) with the parasitic components of the antenna creates a S11 notch that is slightly shifted from the LO. Cross-coupled feedback resistors (R_{fc}) are connected from output of I channel of the amplifier to input of Q channels in order to match the complex part of the impedance [8]. Such feedback represents 90° phase shift seen at the antenna port as complex impedance. The final matching network accounting for matching of real and complex parts of the impedance is shown in Fig.5.

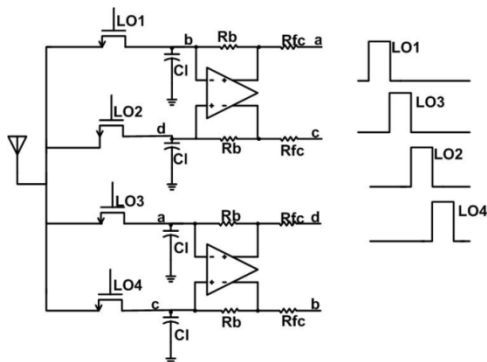


Fig.5 Final time varying matching network

B. Quadrature band pass charge domain sampling filter

The front end quadrature bandpass charge domain sampling filter is depicted in Fig.6. The control signals for 2GHz band are shown in Fig.7. A transconductor G_m converts the input RF voltage signal into current that is integrated on a sampling capacitance for an interval of time. The voltage on the capacitance is sampled at the output, producing a Sinc function response. The response shows notches at multiples of $(1/T_i)$ as represented by (1) [9], [10], where T_i is the current sample integration time.

$$H(f) = |H_{SINC}(f)| = \frac{G_m}{C_s} \left| \frac{\sin(\pi f T_i)}{\pi f} \right| \quad (1)$$

The integration of several input current samples gives discrete time Sinc FIR filtering effect as is given by (2) [9, 10]. Notches exist at integer multiples of $\frac{1}{NT_f}$. T_f is the time between two successive integrated samples (the sampling time of the FIR filter), N is the number of integrated samples and C_s is the sampling capacitance.

$$H_{tot}(f) = \frac{V_{out}(f)}{V_{in}(f)} = \frac{G_m}{C_s} \cdot \frac{1 - e^{-j2\pi f T_i}}{j2\pi f} \cdot \sum_{K=0}^{N-1} h_K \cdot z^{-K} \Big|_{z=e^{j2\pi f T_f}} \quad (2)$$

For an optimal anti-aliasing filtering effect, the sampling time T_s should be equal to $(N \cdot T_f)$, this places the notches of Sinc response on top of multiples of sampling frequency (f_s). In addition to the integration period of the samples ($N \cdot T_f$), there is time for output read out and discharging of the sampling capacitance setting constraints on the minimum sampling time (T_s). The output sampling frequency can be increased by using time interleaved sampling operation.

Complex band pass filtering image rejection is realized by transferring the low pass discrete first order Sinc response to the required center frequency $f_c = (1/(4 \cdot T_f))$. This comes through multiplying the impulse response by $e^{jn\pi/2}$ resulting in complex FIR coefficients $[+1, +j, -1, -j]$ which is equivalent to $[+1, 0, -1, 0]$ for real channel and $[0, +1, 0, -1]$ for imaginary channel [9],[10]. The (-1) is implemented by the cross coupling of inverted and non-inverted current signal paths.

Integration of several current samples causes decimation and down conversion, decreasing the sampling frequency of the next block the Analog to digital converter to $(1/(N \cdot T_f))$. Here the reciprocal of the sampling frequency of the FIR filter (T_f) is equal to the integration time (T_i). The center frequency and the bandwidth of the charge domain bandpass filter changes by changing the integration time of the current sample. The bandwidth is inversely proportional to the integration time and number of taps of the filter. The conversion gain of the sampler is given by (3).

$$\text{Conversion gain} = \frac{2\sqrt{2} \cdot N \cdot G_m \cdot T_f}{\pi \cdot C_s} \quad (3)$$

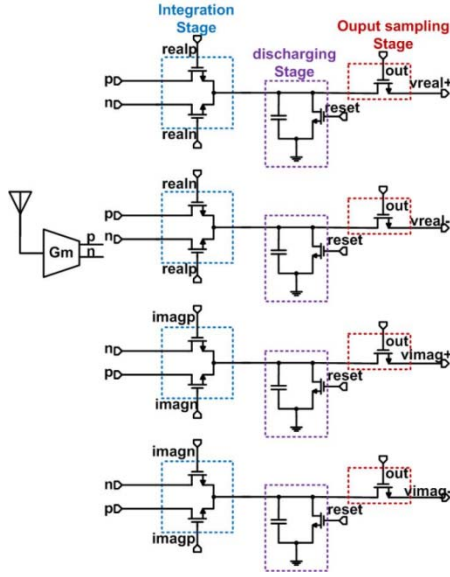


Fig.6 One channel of the quadrature bandpass charge domain sampling filter

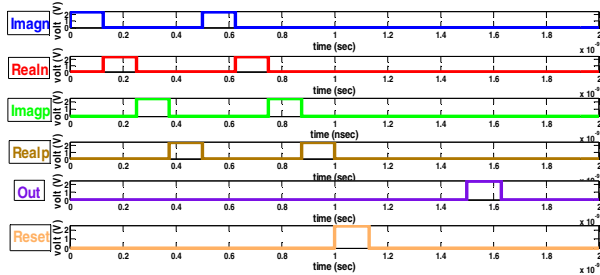


Fig.3a the controlling clocks of the filter first channel

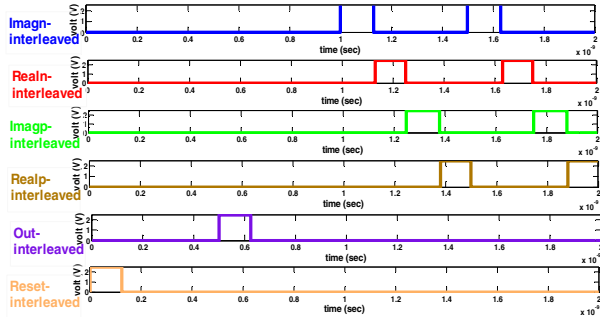


Fig.3b controlling clocks of the filter second interleaved channel

III. Simulation results

A typical receiver with input frequency located at 2GHz is examined to check the receiver's functionality targeting LTE specifications. The charge sampler model parameters are shown in Table.I The time varying matching network model parameters are as shown; the switch resistances of 20Ω and the noise current of each switch of 8.284×10^{-22} . The baseband resistance is set to 25k a, and the amplifier zero frequency gain to be 40 dB with noise of 3.314×10^{-19} , baseband capacitance (C1) to be 10pF and Rfc is set to 65K. The tunable matching of the receiver is tested and S11 for 2GHz in put is shown in Fig.8 indicating good matching. The center frequency of the sinc filter response is

controlled by changing the integration time and the width of the pass band and the location of the notches is controlled by the number of integrated current samples. Fig.9 shows the conversion gain is 57 dB at 2GHz by choosing G_m to be 50mS, $T_f = T_r = 125$ psec, $N=8$ and $c_s = 62.5$ fF. The Sinc function response with notches at multiples of FIR filter sampling frequency improves the in-band and out of band linearity of the receiver. Linearity is more enhanced by the time varying matching network selectivity. Linearity of the receiver is tested through measuring its IIP3 and P1dB; IIP3 is tested for two input signals at 2.1GHz and 2.12GHz achieving IIP3 of -1.7 dBm as shown in Fig.10. 1-dB compression point (P1dB) is -10 dBm for input frequency of 2.1GHz as shown in Fig.11. The placement of the notches of the FIR sinc filter at multiples of the output sampling frequency enhances the noise figure by suppressing of the noise folding at multiples of the sampling frequency. The DSB NF of the receiver is 7.3 dB as shown in Fig.12. The results obtained are compared with other architectures supporting wideband frequencies in table II.

Table.I Charge Sampler model parameters

Block	G_m (S)	Output current noise (A^2/Hz)	ON resistance (Ω)	OFF resistance (Ω)	IIP3 (dBm)
Transconductor	50m	3.3136×10^{-22}	-	-	-8
Integration switches	-	3.3136×10^{-22}	50	1G	-10
Discharging switches	-	1.3807×10^{-22}	120	10G	25
Sampling to output switches	-	2.549×10^{-22}	65	1G	0

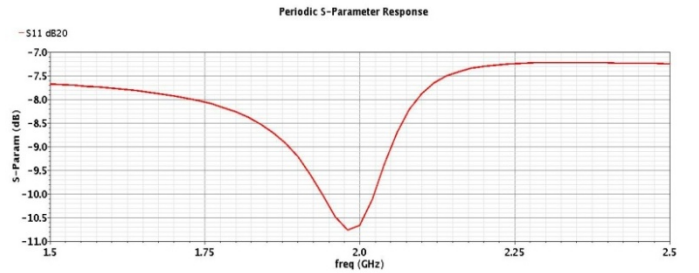


Fig.8 S11 of the time varying matching network

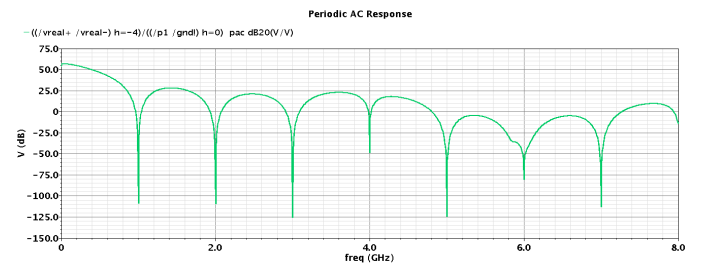


Fig.9 Conversion gain of the band pass charge sampling filter

CONCLUSION

In this paper, a reconfigurable sampling receiver design with a multi-band matching network for a multiband multi-standard and software defined radio receivers is presented. The filtering response of the discrete time band-pass filter can be changed flexibly by changing the controlling LO signal and usage of a time varying matching network. Good matching and the translated band-pass filter response can be held over a multi-band of frequencies.

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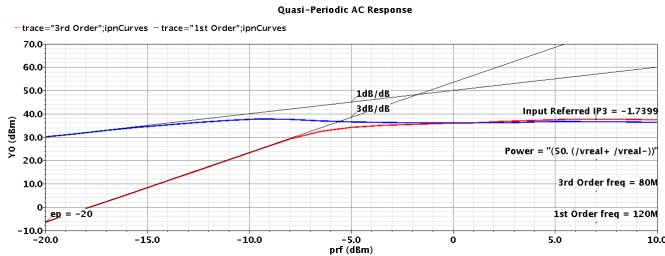


Fig. 10 IIP3 for inputs at 2.1GHz and 2.12GHz

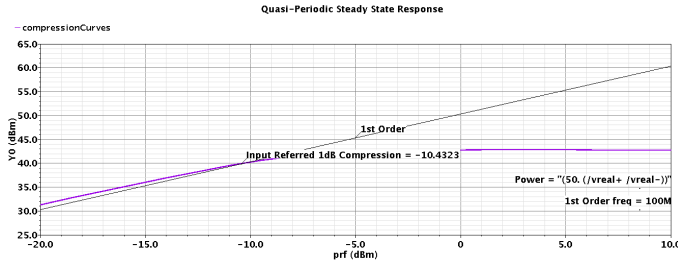


Fig. 11 P1dB for an input of 2.1GHz frequency

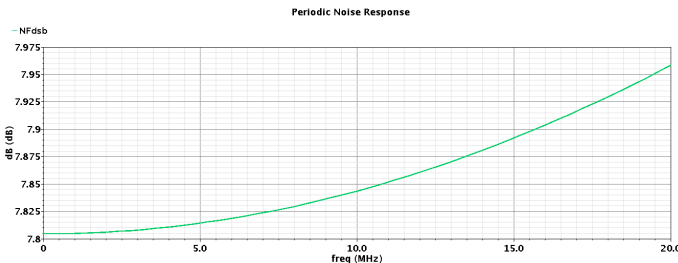


Fig.12 Noise Figure at 2GHz

Table II Results summary of the proposed receiver architecture

Architecture	Frequency (GHz)	Conversion gain (dB)	P1dB (dBm)	IIP3 (dBm)	DSB NF (dB)
[5]	1	20.2	-2.8	6.7	7.3
[11]	2.3 (BW=30MHz)	30	-14.5	-6.6	6
[12]	0.5 - 6.0	12.6	-7.5	3.2	6
[13]	0.7 - 2.6	31	-7	2	11-12
LTE specifications	0.7→2.7	-	-20	-10	9
This work	0.7 - 2.7	57 at 2 GHz	-10.5	-1.8	7.8

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