Insights for Utilizing the Memristor as a Multi-bit Based Memory

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Abstract— **The memristor, known as the fourth basic two-terminal circuit element, has attracted many research interests since HP labs were able to develop the device based on what L. Chua predicted theoretically. The memristor is a potential contender for the next-generation memory due to its distinctive characters, such as non-volatility, non-linearity, low-power consumption, good scalability and its ability to store multi-bit values. These electrical characteristics of memristors are mainly determined by the material characteristic and the fabrication process. However, the manufacturing of memristors is facing various challenges due to the difficulty of controlling its process variation, as it is fabricated at nano-scale geometry's size. These process variations lead to deviation in results from the theoretical results which lead to reduction in the reading yield. In this paper, we present the multi-bit memristor and we investigate the effect of the memristor size and the process variations effect on the multi-bit memristor and how we can maximize the reading yield.**

I. INTRODUCTION

Memristor was first theoretically predicted by L.Chua in 1971 [1]. It is considered the fourth fundamental circuit element, to complete the set of passive devices that previously included only resistor, capacitor, and inductor. In 2008, the first physical realization of memristor was demonstrated by HP Lab, in which the memristive effect was achieved by moving the doping front along TiO_2 thin-film device [3].

The memristor developed by HP labs is a TiO_2 thin film of length D, with two metal contacts at each end as shown in (Fig.1) [4]. The memristor can be split into two main parts: I) a high doped region with low resistance (R_{on}), and II) a low doped region with high resistance (R_{off}). Low doped region consists mostly of TiO_2; however the high doped region consists of TiO_{2-x}. The high doped region contains more oxygen vacancies which makes its resistance less than that of the low doped region. (R_{on}) and (R_{off}) notations represent the high doped and low doped regions respectively [6]. Moreover, the memristor has the ability to retain the state for a long time after the current has been switched OFF which means it is a non-volatile device.

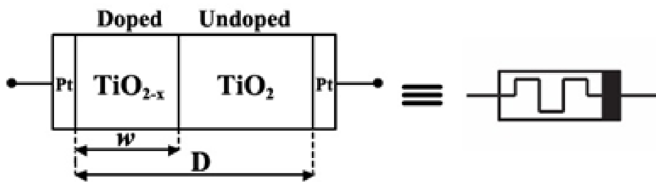

Fig. 1. TiO_2 Memristor of length D and the corresponding Memristor symbol [4].

Due to its ability to remember past charges, an intuitive utilization for it is to be used in memory design [6]. Memristor shows many promising characteristics as the next-generation data storage device [2], such as non-volatility, low power consumption, high performance, high density and excellent scalability [2] [7]. Manufacturing the memristor devices at nano-scale faces many problems which results in critical device parameter fluctuations, incurred by process variations, which is a critical concern affecting the device performance [2] [7]. The process variations sources are line-edge roughness (LER), oxide thickness fluctuation (OTF), and random discrete doping (RDD) [8].

In this paper we attempt to use the memristor as a multi-bit memory and give some insights on the effect of the process variations and dimensions on the reading yield, and how to maximize it through our method of threshold optimization.

II. PRELIMINARIES

A. Yield Concept

The process variations cause the actual results to deviate from its actual results thus we used the yield concept to give us an accurate description of the actual results in storing a value, the yield is the probability of writing a value and reading the same value. We can calculate the yield by calculating the probability of failure, which is the error in reading a different value than the written one, for example in (Fig. 2) is the yield for writing and reading '0' which is denoted by (Y_0=1- $f_{1/0}$) where Y_0 is the probability of writing '0' and reading '0', $f_{1/0}$ is the probability of writing '0' and reading '1'.

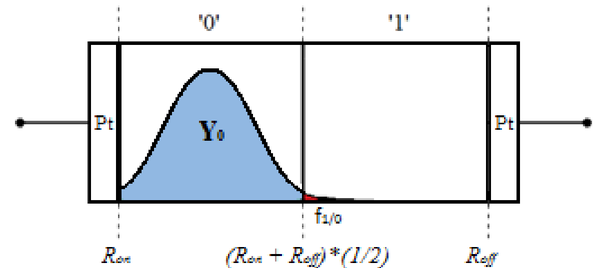

Fig. 2. Yield of Y_0

B. Multi-bit Memristor

The multi-bit memristor memory we can store multi-bit values such as ('00', '01', '10', '11') or ('000', '001', '010', '011', '100', '101', '110', '111') which allows for much better memory storage, however, the storing capacity is limited by the process variations. The multi-bit memristor is divided into four

regions, the first regions, for writing and reading '00', is bounded between R_{on} and the first threshold $(R_{on} + R_{off})*(1/4)$, the second region, for writing and reading '01', is bounded between the first threshold and the second threshold $(R_{on} + R_{off})*(1/2)$, the third regions for writing and reading '10' is bounded between the second threshold and the third threshold $(R_{on} + R_{off})*(3/4)$, the fourth regions for writing and reading '11' is bounded between the first threshold to R_{off}.

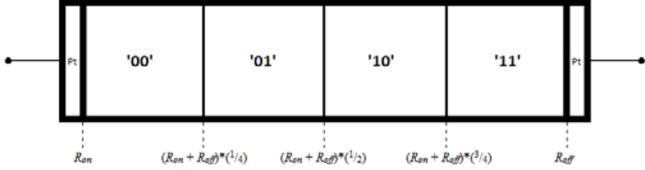

Fig. 3. Multi-bit Memristor storing 2 bit values

III. MEMRISTOR MODEL ANALYSIS

As an external voltage bias is applied across the device, the electric field repels positively charged oxygen vacancies in the doped layer into the pure TiO_2 layer thus changing the length w which is the width of the doped region (TiO_{2-x} layer). Hence, the device's total resistivity changes. If the doped region extends to the full length, that is w/D=1, the total resistivity of the device is dominated by the low resistivity region, with a value measured to be R_{on}. Likewise, when the undoped region extends to the full length D, $w/D=0$, the total resistance is denoted as R_{off}. The main parameters of the memristor are R_{on} and R_{off}, the device resistance is bounded between [8]:

$$R_{on} \leq R(w) \leq R_{off} \tag{1}$$

According to [1][9][10], the memristor has memory effect since the device maintains its resistivity even if the power goes off. The mathematical model for memristive device resistance can be described as [8]:

$$R(w) = (R_{on}.w/D + R_{off}.(1 - w/D)) \tag{2}$$

The state of the memristor changes according to the amount of flux injection. When the memristor state is controlled by the input flux across the cell, this input flux is given by:

$$\phi = \frac{\phi_D}{R_{off}^2}\left[R_{off}^2 - R_{on}^2\right] \tag{3}$$

$$\phi_D = \frac{(\beta D)^2}{2\mu_v(\beta - 1)} \tag{4}$$

Where β denoted the $R_{on} = \beta.\ R_{off}$ ratio, μ_v is the mobility. In the rest of paper, x and x' are used to represent the design value and the actual value under process variations for any given variable x, respectively [10].

For a given TiO_2 memristor, R'_{off} and R'_{on} are used to denote its actual highest and lowest total memristances, respectively [10].

$$R'_{off} = R_{off}.\eta(\mu R_{off} + \sigma R_{off}.E).(1 + \sigma_y.D) \tag{5}$$

$$R'_{on} = R_{on}.(\mu R_{on} + \sigma R_{on}).E \tag{6}$$

Here, two independent random numbers $E \sim N(0,1)$ and $D \sim N(0,1)$ are introduced. E represents the correlation between R'_{off} and R'_{on} due to the same geometry variation sources, D and σ_y represent the impact of RDD. It was found that the actual α', can be modeled as the product of the designed value α, where α=w/D and a coefficient η that represents the influence of process variations as [10]:

$$\alpha' = \eta.\alpha \tag{7}$$

Here η can be expressed by [10]:

$$\eta = \frac{1}{(1 + \phi.\varepsilon_2 + \phi.\varepsilon_2(\omega_1.E + \omega_2.G)).(1 + \sigma_y.D)} \tag{8}$$

To avoid overestimating the impact of geometry variations on α', a new random number $G \sim N(0,\ 1)$ is introduced to offset the impact of LER. ε_1 and ε_2 are two scalars extracted from the actual simulations performed by the device simulator. The coefficients w_1 and w_2 represent the weights of E and G, where $w_1^2+w_2^2=1$. By modeling R'_{on}, R'_{off} and α', the total memristance M' of a TiO2 memristor can be simply calculated by:

$$M'(\alpha) = R'_{on}.\alpha' + R'_{off}.(1 - \alpha') \tag{9}$$

IV. SIMULATION RESULTS AND DISCUSSIONS

A. Effect of the process variation on the read yield

The process variations effect is different on each region due to change in resistance as the memristance (M) is given by:

$$M(\alpha) = R_{on}\alpha + R_{off}(1 - \alpha) \tag{10}$$

As an example of how the process variations affect the yield we will assume the values (R_{on} =100 Ω and R_{off} =100 KΩ.), when α = 0, M = R_{off} .If α, due to process variation equals 0.001, M= 0.001* R_{on} +0.999* R_{off} ≃99.9 KΩ with an error of 0.1%. However, for α = 1, M = R_{on}. If α, due to process variation equals 0.999, M= 0.999* R_{on} +0.001* R_{off} ≅ 200 Ω with an error of 100 %. That's why the failure percentage in the case of reading '0' is much lower than that in the case of reading '1'.

A.1. Single bit threshold yield

The region for writing and reading '0' is bounded between Ron to the threshold that is selected to be midway between R_{on} and R_{off}, typically, $(R_{on} + R_{off}) / 2$ [5].

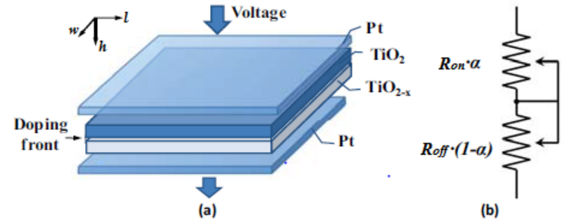

Fig. 4. TiO2 thin-film memristor. (a) Structure, and (b) equivalent circuit. [10].

In Table 1 is the reading yield for a memristor with dimensions (h=3 nm, w=l=30 nm and w=l=100 nm), and it's shown how the reading yield Y_0 is lower than Y_1.

Table 1
Single-bit yield for memristor with height 3 nm

Memristor dimensions	Yield	
	Y_0	Y_1
w = l = 30 nm	0.9331	1.0000
w = l = 100 nm	0.9863	1.0000

A.2. Multi bit threshold yield

In the multi–bit memristor the effect of the process variations on the yield are much more apparent due to the fact we are storing more values, which leads to closer regions so the probability of failure is much higher. In Fig.6 is the yield for the different regions for a memristor with dimensions (w=l=100nm and h=10nm), from the figure we can observe how the yield for the multi-bit is much lower than the yield of the single-bit.

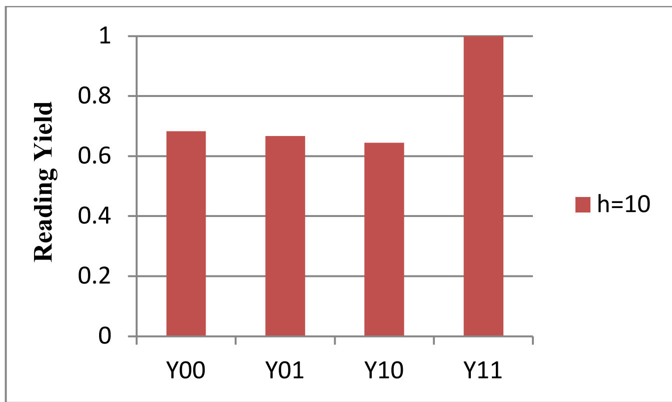

Fig. 5. Multi-bit Yield in case of (w=l=100nm and h=10nm)

B. Effect of the memristor dimensions on the read yield

We attempted to study the effect of varying the memristor dimensions on the reading yield. Thus we compared the yield of different sized memristors and we found that the yield and the size of the memristor are directly proportional, a comparison between memristors with different height (h) but with same width and length (w = l =100nm) for the single-bit memristor is shown in Fig.4 and a comparison between memristors with different height (h) but with same width and length (w=l=100nm) for the multi-bit memristor is shown in Fig.5.

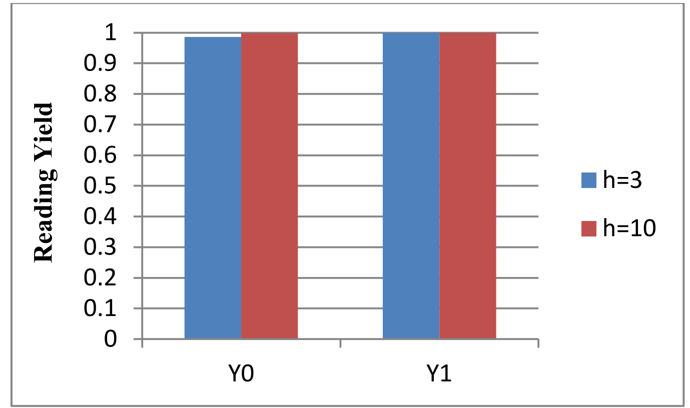

Fig. 6. Single-bit Reading Yield in case of (w=l=100nm)

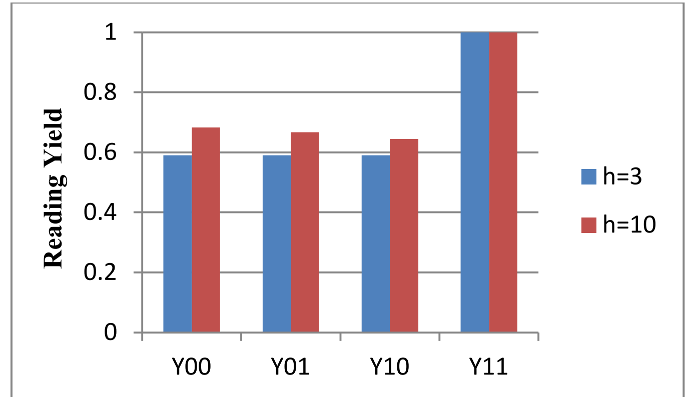

Fig. 7. Multi-bit Reading Yield in case of (w=l=100nm)

C. Yield optimization

Since that process variations effect is different on each region, due to change in resistance, means that choosing to divide the memristor into equal regions, to store the values, wasn't the best decision. In order to maximize the yield we attempted to vary the regions threshold finding the optimal regions for each value that results in maximum reading yield. Taking into consideration the fact that optimizing the region for one value changes the adjacent regions which could lead to lower yield, we calculated the overall yield, denoted by $Y_{overall}$, so that we find the optimal yield for a specific region that leads to a total increase of all the reading yields.

C.1. Single-bit

To optimize the reading yield, the threshold of the single-bit memristor that is $[(R_{on} + R_{off}) / 2]$ has been varied to find the optimal threshold that results in maximum reading yield, the overall yield for the single-bit memristor is ($Y_{overall} = Y_0 * Y_1$). A comparison between the fixed and the optimized threshold overall yield is given in Table 2 for a memristor with height (h=10nm) and with different width and length. As shown in Table 2, optimizing the threshold gives better overall reading yield resulting in 100% yield in some cases, which means there is no probability of failure after optimizing the regions' threshold.

Table 2
Comparison between fixed and optimized threshold overall yield

Memristor dimensions h=10 nm	Overall Yield	
	Fixed threshold	Optimized threshold
w = l = 50 nm	0. 9924	1.0000
w = l = 100 nm	0. 9980	1.0000

C.2. Multi-bit

In order to verify the method of optimizing the regions threshold, we calculated the overall yield ($Y_{overall} = Y_{00} * Y_{01} * Y_{10} * Y_{11}$) for fixed threshold, then we varied the thresholds of each region to find the optimal region for each value and calculated the overall yield for the optimized threshold. The results from the optimized threshold regions shows clearly the enhancement in the overall yield compared to the results from the fixed threshold region, as shown in Table 3 and Table 4 are a comparison between the overall yield for the fixed and optimized threshold for memristors with h=3 nm and h=10 nm respectively with different dimensions.

Table 3
Comparison between fixed and optimized threshold overall yield for the multi-bit memristor with height 3 nm

Memristor dimensions h=3 nm	Overall Yield	
	Fixed threshold	Optimized threshold
w = l = 50 nm	0. 0469	0. 8813
w = l = 70 nm	0. 0631	0. 9167
w = l = 100 nm	0. 0842	0. 9425

Table 4
Comparison between fixed and optimized threshold overall yield for the multi-bit memristor with height 10 nm

Memristor dimensions h=10 nm	Overall Yield	
	Fixed threshold	Optimized threshold
w = l = 50 nm	0.1474	0. 9072
w = l = 70 nm	0.2304	0. 9412
w = l = 100 nm	0.2929	0. 9543

V. CONCLUSION

In this paper, the design of the multi-bit memristor-based memory is proposed. Also, we observed the effect of changing the memristor size and the process variations on the single-bit and the multi-bit memristor memory reading yield. The "Fast Statistical Model of TiO_2 Thin-Film Memristor" had been used for the memristor device simulations, which was done using MATLAB. The paper proposed a method on how to improve the reading yield through optimizing the regions threshold. Simulation results showed that optimization enhances the overall yield from 0.2304 to 0.9412 in some cases. The extension of this work is to try to increase the memory storage of the memristor by using it as a memory for higher multi-bit data.

VI. ACKNOWLEDGMENT

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REFERENCES

[1] L. Chua. Memristor-the missing circuit element. IEEE Transaction on Circuit Theory, pages507–519, 1971.
[2] D. Niu, Y. Chen, C. Xu, and Y. Xie. Impact of process variations on emerging memristor. In Design Automation Conference (DAC), pages 877–882, 2010.
[3] Budhathoki, R.K., Sah, M.P., Adhikari, S.P., Hyongsuk Kim and Chua, L. Composite Behavior of Multiple Memristor Circuits. IEEE Transactions on Circuits and Systems I: Regular paper, vol 60, no.10, 2013.
[4] Y. Ho, G. M. Huang, and P. Li. Nonvolatile memristor memory: device characteristics and design implications. In International Conference on Computer-Aided Design, pages 485–490, 2009..
[5] Abdallah, M. and H. Mostafa. Yield Maximization of Memristor-Based Memory Arrays. IEEE, International Conference on Microelectronics (ICM'14), Doha, Qatar (In Press)
[6] H. Elgabra, I. Farhat, A. Al Hosani, D. Homouz, B. Mohammad. Mathematical Modeling of a Memristor Device. International Conference on Innovations in Information Technology (IIT), pages 156–161, 2012.
[7] M. Hu, H. Li, Y. Chen, X. Wang, and R. Pino. Geometry variations analysis of TiO_2 thin film and spintronic memristors. In Asia and South Pacific Design Automation Conference (ASP-DAC), pages 25–30, 2011.
[8] Y. Ho, G. Huang and P. Li. Dynamical Properties and Design Analysis for Nonvolatile Memristor Memories. 724 IEEE Transactions on Circuits and Systems—I:Regular papers, vol. 58, NO. 4, APRIL 2011.
[9] Y. Ho, G. M. Huang, and P. Li. Nonvolatile memristor memory: device characteristics and design implications. In International Conference on Computer-Aided Design, pages 485–490, 2009.
[10] M. Hu, H. Li, R. Piano. Fast Statistical Model of TiO_2 Thin-Film Memristor and Design Implication. The International Conference on Computer-Aided Design, pages 345-352, 2011.