Area-Efficient Read/Write Circuit for Spintronic Memristor Based Memories

Sherif F. Nafea[1], Ahmed A.S. Dessouki[2], S. El-Rabaie[3], Basem E. Elnaghi [1], Yehea Ismail[4], Hassan Mostafa [4,5]

[1] Electrical Engineering Dept., Faculty of Engineering, Ismailia, Suez Canal Univ., Egypt.

[2] Electrical Engineering Dept., Faculty of Engineering, Port Said, Port Said Univ., Egypt.

[3] Electronics and Electrical Communications Dept., Faculty of Electronic Engineering, Menoufia University, Menouf, Egypt.

[4]Center for Nanoelectronics and Devices, AUC and Zewail City of Science and Technology, New Cairo 11835, Egypt.

[5]Electronics and Communications Engineering Department, Cairo University., Egypt.

Emails: sheriff_kamel@eng.suez.edu.eg, dessouki2000@yahoo.com, srabie1@yahoo.com, hmostafa@uwaterloo.ca

Abstract **Memory circuits occupy substantial area percentage of recent . In addition, the continuous scaling of CMOS technology faces increasing technological difficulties. Thus, there is a need for alternative technologies that can offer larger memory densities and better performance. Spintronic memristor offers a good alternative for memory design due to its inherent non-volatility, good scalability, and radiation hardness. In this paper, a read/write circuit for spintronic memristor-based memories is proposed. The proposed read/write circuit achieves a significant reduction in the occupied area. The read disturbance of the circuit is investigated to calculate the maximum allowed number of reading cycles before a refreshment operation is needed.**

Keywords ***Spintronic memristor; Read/Write Circuits; thermal fluctuations; memory design; read disturbance.***

I. INTRODUCTION

The memristor device was first proposed by Prof. Chua as the fourth fundamental element beside resistors, inductors, and capacitors [1]. This element completes the missing link between magnetic flux (-) and electric charge (q). The memristor was not practically realized until 2008 when HP Labs announced the physical realization of a solid-state memristor element using a TiO_2 strip sandwiched between two Platinum electrodes [2]. Since then, the memristor gained a wide research interest. Memristor devices have some distinguished properties that benefit greatly in the field of memory design. Memristors offer excellent scalability as its memory cell occupies about $4F^2$ [3]. Memristors also have an inherent non-volatile property as it can hold its last state after being unplugged from the power source.

A. Spintronic Memristor

Beside the HP memristor, many devices have been submitted as physical realizations of memristors. One of these types is the spintronic memristor, which is the main focus of this paper [4]. Fig. 1 shows the structure of the domain-wall spintronic memristor. The device consists of two ferromagnetic layers; the pinned layer (PL), and the free layer (FL). The pinned layer has a fixed magnetization direction and it is used as a reference layer. The free layer is allowed to change its magnetization direction using the spin-transfer torque effect [5]. The free layer is divided into two parts, one with a parallel magnetization direction to the PL and the other with antiparallel magnetization direction separated by the µGRPDLQ ZDOO¶. The ¶domain ±wall position

(a)

(b)

Fig. 1 A spintronic memristor based on magnetic-domain-wall motion: (a) Structure. (b) Equivalent circuit.

represents WKH -µVWUDLWDEHOH¶ RI WKH PHPULV, which can be moved by passing a driving current through the memristor.

Spintronic memristor memory cells benefit from the advantages of MRAM cells such as radiation hardness and mature memory technology. On the other hand, spintronic memristors are affected by the thermal fluctuations. Including the thermal fluctuations effect during the modeling of spintronic memristors and consequently during the design of memory circuits is important to investigate the circuit reliability and the possible disturbance in the saved data during the read operation.

B. Spintronic Memristor Modeling

The modeling of memristors consists of two main equations. The first equation is the current-voltage relationship, and the second equation relates the memristance of the device to the domain wall position, which is usually, depends on the current passing through the memristor. In this section, we discuss two modeling approaches; Wang [4] model and the TFA model [6].

1) Wang Model:

Fig.1 E VKRZV WKH PHPULVWRU¶V HTX Wang model. Similar to most memristor models, it assumed that the domain-wall divides the memristor into two resistors for the parallel and the antiparallel parts. The parallel part has a lower resistivity state and the antiparallel part has a higher resistivity state. The values of the resistance per unit length of the spintronic memristor at the low-resistance and the high-resistance states are r_L and r_H respectively. The memristance of a spintronic memristor can be calculated as follows:

/ :T; L Nä S E Nä & F S; (1)

where w is the position of the domain wall, and D is the length of the device. Note that the domain-wall thickness ¨w is assumed very small and thus ignored. When applying a driving

current, the domain-wall motion velocity (v) is proportional to the effective current density (J_{eff}) and thus can be written as follows:

$$v = \frac{dw}{dt} = \beta J_{eff} \tag{2}$$

where β is the domain-wall velocity coefficient. The effective current density J_{eff} only affects the domain-wall position if it is greater than a specific critical value J_{cr} as provided in (3).

$$J_{eff} = \begin{cases} J, & J \geq J_{cr} \\ 0, & J < J_{cr} \end{cases} \tag{3}$$

According to (3), currents lower than the critical value do not affect the memristor state, and thus if the current used in the reading operation of memory cells is lower than this critical value, there will be no disturbance in the stored data. However, this model did not include the effect of thermal fluctuation, which is important for all Magnetic Tunneling Junction (MTJ)-based structures. Thus, some unexpected disturbances to the stored data might occur and it cannot be observed using this model.

2) Thermal-Fluctuations Aware (TFA) Model

The TFA spintronic memristor model modified the Wang model in order to include the thermal fluctuations effect [6].The thermal fluctuations might cause undesirable disturbance to the stored data in spintronic memristor memories during the read operation. In the TFA model, the value of J_{eff} is modified to include the thermal fluctuations effect as provided in (4).

$$J_{eff} = \begin{cases} J - \frac{[illegible]}{t_P}, & J \geq J_{cr} \\ 0, & J < J_{cr} \end{cases} \tag{4}$$

where t_P is the duration time until memristor's state is switched. For a given design parameter $P_{failure}$, t_P equals:

$$t_P = \tau_0 e^{\Delta} \ln\left(\frac{1}{1-P_{failure}}\right) \tag{5}$$

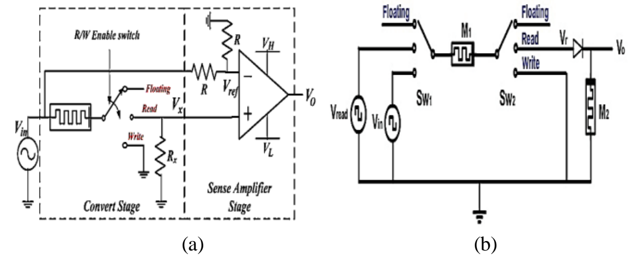
where $P_{failure}$ represents the probability of switching the data stored in the memristor.

The TFA model provides a better understanding of the spintronic memristors behavior, and it can be used to define the maximum allowable successive read cycles before the stored data in the spintronic memristor is disturbed. Thus, all the analyses provided in this paper use the TFA model.

In this paper, a thermal-fluctuations aware (TFA) model is used to investigate the read/write operations of spintronic memristor memories. The proposed read/write circuit is introduced and compared with two well-known read/write circuits. The read disturbance, which occurs due to the pulse mismatch of the read signal, is studied in order to calculate the required refreshment frequency.

II. READ/WRITE CIRCUITS OF MEMRISTOR MEMORIES

The read/write circuit of spintronic memristor memories requires a careful design to avoid data disturbance during the read operation. Spintronic memristors have a small OFF state resistance R_{OFF} - denoted here by R_H - and a small ON/OFF resistance ratios, which increases the possibility of read disturbance and reduces the sensed voltage difference. It is required to design a read/write circuit that can achieve larger sensed voltage difference, lower read operation data disturbance, and smaller occupied area.



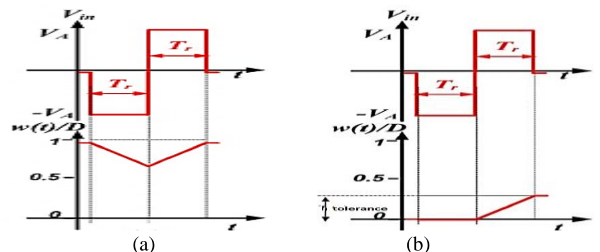
(a) (b)

Fig. 2 Two possible Read/Write circuits realizations (a) Yenpo R/W circuit[7] (b) El-Shamy R/W circuit [8].

Fig. 2 shows two realizations of read/write circuits proposed by Yenpo et al. [7] and El-Shamy et al. [8]. For both R/W circuits, the write operation is achieved simply by applying a DC write voltage for enough time T_{WRITE} to ensure full switching.

For the R/W circuits shown in Fig. 2.a, the read operation is achieved by applying the read pulse shown in Fig. 3. The read pulse consists of two opposite polarities pulses with the same amplitude and width in order to compensate the read disturbance of each other. However, in the case of pulse widths mismatch, a small read disturbance occurs which means that this circuit needs a periodic refreshment after a specific number of reading cycles. The reading operation is achieved by comparing the voltage V_X which is a voltage divider between the memristor's resistance and $R_X = (R_H + R_L)/2$, with a reference voltage $V_{ref} = V_{read}/2$. The main disadvantage of this circuit is the large area required to fabricate the resistors.

The second R/W circuit is shown in Fig. 2.b. This circuit was originally proposed for solid-state memristor in order to avoid the date disturbance of Yenpo R/W circuit. Note that this circuit is equivalent to the convert stage only. However, due to the small R_H of spintronic memristors compared to solid-state memristors, this advantage cannot be achieved in case of spintronic memristors as will be shown in the simulation results.



(a) (b)

Fig. 3 Read pulse when reading a logic ‘ ’ [7].

III. PROPOSED READ/WRITE CIRCUIT

Fig. 4 shows the proposed R/W circuit. In this circuit, the resistor R_X of Yenpo circuit is replaced by two parallel memristors (M_2, M_3) and they are kept in the OFF state. Thus, the equivalent resistance of M_2 and M_3 equals ($R_H/2$). Despite that, this value is slightly lower than R_X, it can give similar operation without any problems. Similarly, the two resistors of the sense stage are also replaced by two memristors (M_4 and M_5). This circuit works in the same manner of Yenpo R/W circuit. During floating and write operation, memristors (M_2, M_3, M_4, and M_5) are connected to a voltage (V_{DD}) to prevent accumulated mismatches that occur in the read operation. Memristor M_1 represents the memory cell, and it still affected by the read pulse mismatch like in Yenpo R/W circuit. The main advantage of this circuit is the great

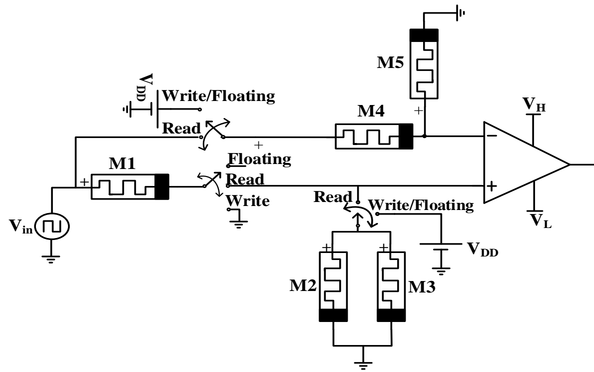


Fig. 4 Proposed Read/Write Circuit.

reduction in the circuit¶V area, as the memristor¶ area is much smaller than its equivalent resistor.

A. Simulation results

Memristor parameters are taken from [9]. The ON/OFF ratio is adjusted to 5, which is the largest ratio achieved in spintronic PHPULVWRUV XS WR WKH DXWKRU¶V N [10]. The memristor dimensions are (D=200nm, z=10nm, h=70A). The thermal stability factor ¨=50.

Fig. 5 shows the equivalent circuit of the R/W circuit during the write operation. The write operation is simply achieved by DSSO\LQJ D SRVLWLYH SXOVH RI 9 H RI -1 9 WR ZULWH Fig. 6 shows the simulation results of the write operation.

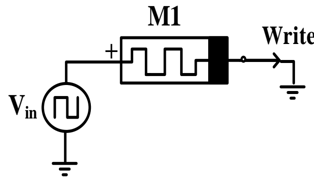


Fig. 5 Equivalent R/W Circuit during the write operation.

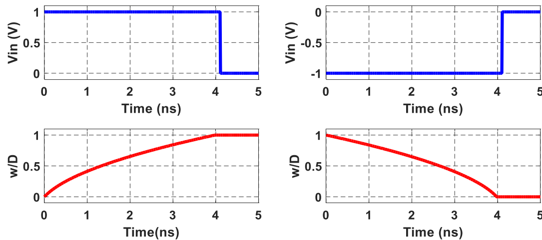


Fig. 6 Write operation D /RJLF µ ¶ Z ' E /RJLF µ ¶

Fig. 7 shows the equivalent R/W circuit during the read operation. The simulation results of the read operation for one cycle is shown in Fig. 8. In the case of w/D=1, the negative pulse compensates the positive pulse disturbance. If w/D=0, the first negative pulse cannot reduce w/D as it is at minimum limit. However, this disturbance is not accumulative as the next read cycle w/D>0 and thus next negative and positive pulses compensate each other. The data out is sensed during the positive reading pulse, thus the output is valid after the rising edge of the reading pulse as shown in Fig. 8.b. Fig. 9 shows the memristor¶V state and the data out for successive reading pulses. As shown in the figure, there is no data disturbance as long as there is no pulse match in the reading voltage signal.

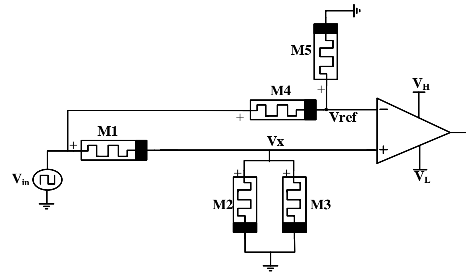


Fig. 7 Equivalent R/W circuit during Read operation.

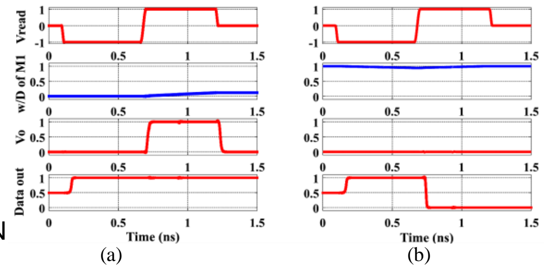


Fig. 8 Read operation one cycle D /RJLF µ ¶ Z ' E /RJLF µ

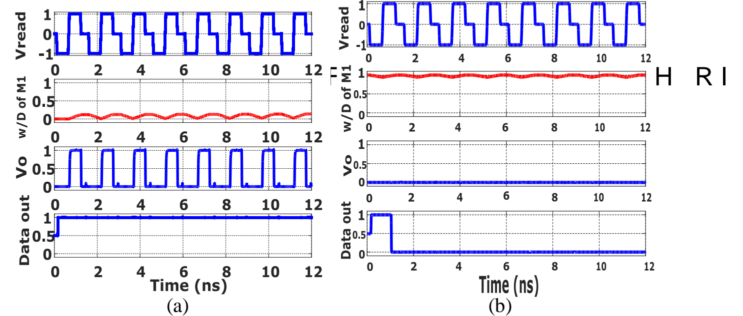


Fig. 9 Read operation successive cycles D /RJLF µ ¶ E /RJLF µ ¶

B. Read disturbance

The read disturbance is an important concern, as it defines the maximum allowed successive read cycles after which the data must be refreshed. Assume that the allowable margin for ORJLF ¶ w/D: 0 to 0.4 DQG IRU ORJLF ¶ w/D: 0.6 to 1. The effect of the reading pulse mismatch is similar in the Yenpo and the proposed R/W circuits.

Fig. 10 shows the simulation results of successive reading cycles using El-6KDPL\ 5 : FLUFXLW DQG UHDG contrast with the results of this circuit using solid-state memristors, the stored data is disturbed after only 40 cycles. The high resistance state R_H of solid-state memristors is about 200 . Ÿ, and the voltage drop of the forward biased diode is about 0.7 V. The read current I_{READ} passes through memristors M_1 and M_2, where M_2 is kept always at R_H. In the worst case, if M1 resistance equals R_L Ÿ, the current I_{READ} becomes:

Ė ¾ 0 ½ L Ï Ã ¶ ² µ ? Ï µ / Ë1 N 4.7 / 6 4 4 5 4 L säwä # (6)

This is a small value and thus no disturbance occurs in solid-state memristor. On the other hand, for the spintronic memristor; R_L . Ÿ DQG 5 . Ÿ I_{READ} N 0.3/6K = 50 µA. This current is more than 30 times of the equivalent one in the solid-state memristor, which causes the significant read disturbance as

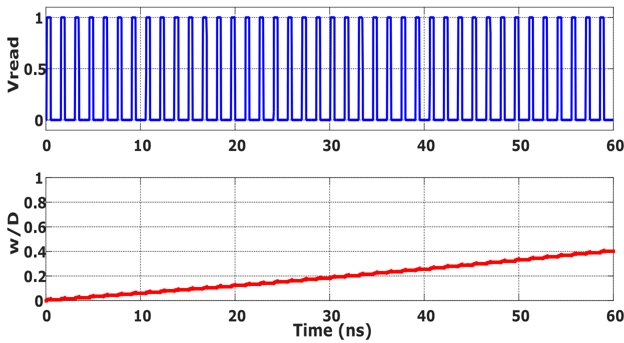


Fig. 10 Read disturbance in El-Shamy R/W Circuit.

shown in Fig.11. Note that this technique uses a positive read pulse only, which means that there are no disturbance in ORJLF µ ¶ VXFFHVVLYH UHDGLQJ

Fig. 11 shows the read disturbance in the proposed circuit for a 10% pulse mismatch. The data is lost after 60 cycles. The logic µ ¶ LV QRW shown here also because the memristor becomes in the higher resistance state, which reduces the read disturbance. 7KXV UHDGLQJ ORJLF µ ¶ LV WKH ZRUVW-case condition.

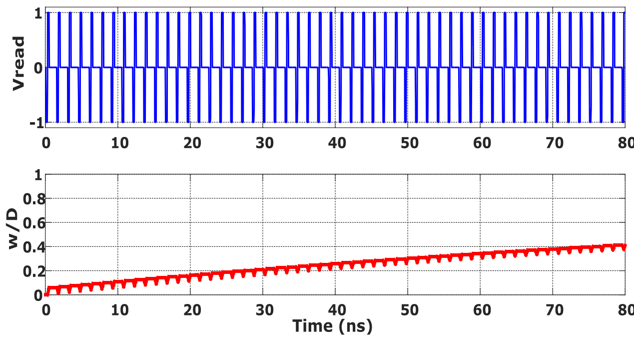


Fig. 11 Read disturbance in the proposed R/W circuit for a 10% pulse mismatch.

Table 1 concludes the comparison between the three R/W techniques. The sense amplifier stage for El-Shamy is assumed the same as in Yenpo R/W circuit. The write power is the same in the three R/W, because they are identical in the write operation. The comparator used in El-Shamy R/W circuit is twice the area of the compactor used in the other two techniques because the sensed voltage difference in El-Shamy is small. The small ON/OFF ratio provided a voltage difference of 60 mV (175 mV for Logic µ ¶ DQG P9 IRU ORJLF µ ¶ 7KH UHVLVWRUV XVHG in the sense stage should be reduced as possible to reduce their area. However, the tolerance of the N-Diffusion resistor should be observed. For this design, 5 . Ÿ is chosen. The convert stage area of the proposed circuit is 1:10^5 of Yenpo R/W and 1:500 of El-Shamy R/W circuits.

IV. Conclusion

In this work, a read/write circuit for memristor memories is proposed. The proposed circuit showed a significant reduction in the read/write FLUFXLW¶V area. The accumulative mismatches occur during successive read cycles is investigated to calculate the required refreshment frequency. The proposed circuit needs a refreshment each 60 cycles compared to only 40 cycles for comparable techniques. The proposed read/ write circuit can be used effectively in designing high-density memory circuits.

TABLE.1 READ/WRITE CIRCUITS COMPARISON

Comparison Aspect	Dynamical [7]	El-Shamy [8]	Proposed
Power 1	270	270	270
	290	290	290
	56	260	52
	88	290	90
Convert stage area 2)	800	4	0.008*
SA stage 2)	277	294	13
(mV)	370	60	355
***N* cycles before refreshment**	60	40	60

*The Memristor area is estimated as (Area=Length*Width)

Acknowledgement

This work was partially funded by Zewail City of Science and Technology, AUC, Cairo University, NTRA, ITIDA, SRC, ASRT, the STDF, Intel, Mentor Graphics, MCIT, NSERC.

References

[1] L. Chua, "Memristor-the missing circuit element," Circuit Theory, IEEE Transactions on, vol. 18, pp. 507-519, 1971.

[2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," Nature, vol. 453, pp. 80-83, 2008.

[3] K. Eshraghian, K.-R. Cho, O. Kavehei, S.-K. Kang, D. Abbott, and S.-M. S. Kang, "Memristor MOS content addressable memory (MCAM): Hybrid architecture for future high performance search engines," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, pp. 1407-1417, 2011.

[4] X. Wang, Y. Chen, H. Xi, H. Li, and D. Dimitrov, "Spintronic memristor through spin-torque-induced magnetization motion," Electron Device Letters, IEEE, vol. 30, pp. 294-297, 2009.

[5] D. C. Ralph and M. D. Stiles, "Spin transfer torques," Journal of Magnetism and Magnetic Materials, vol. 320, pp. 1190-1216, 2008.

[6] S. F. Nafea, A. A. Dessouki, S. El-Rabaie, K. El-Barbary, and H. Mostafa, "Read disturbance and temperature variation aware spintronic memristor model," in Electrical and Computer Engineering (CCECE), 2016 IEEE Canadian Conference on, 2016, pp. 1-4.

[7] Y. Ho, G. M. Huang, and P. Li, "Dynamical properties and design analysis for nonvolatile memristor memories," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 58, pp. 724-736, 2011..

[8] M. Elshamy, H. Mostafa, Y. H. Ghallab, and M. S. Said, "A novel nondestructive read/write circuit for memristor-based memory arrays," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, pp. 2648-2656, 2015.

[9] Y. Chen and X. Wang, "Compact modeling and corner analysis of spintronic memristor," in Proceedings of the 2009 IEEE/ACM International Symposium on Nanoscale Architectures, 2009, pp. 7-12.

[10] L. Wang, C. Yang, J. Wen, S. Gai, and Y. Peng, "Overview of emerging memristor families from resistive memristor to spintronic memristor," Journal of Materials Science: Materials in Electronics, vol. 26, pp. 4618-4628, 2015.