A New Read Circuit for Multi-Bit Memristor-Based Memories based on Time to Digital Sensing Circuit

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***Abstract*— Memristors have gained significant attention in various applications because of their unique properties especially in memory technologies. Owing to their analog nature, memristors have a remarkable ability to store multi-bit values in a single cell. In order to support the full potential of this memory technology the cell must be read with a circuit that exhibits low voltage operation, less complexity, fast, and compatible with digital designs. In this work, a time-based read circuit is proposed that supports the read of multi-bit storage 1T1R cells. This time-based read circuit utilizes a time-based analog-to-digital converter (T-ADC) with 200 mV dynamic range and with time resolution of 6 ps to distinguish between multi-bit states of the memristor. The proposed circuit can support 256 1T1R memory cells**

Keywords— Memristor; 1T1R; multi-bit memory; read circuit, low power; time to digital converter .

I. INTRODUCTION

Memristor (concatenation of "memory resistor") was first introduced in 1971 by Professor Chua [1]. Memristor offers a good alternative for memory design due to low power, high density, non-volatility, high speed, and analog behavior. This analog behavior is used to store more than one bit in a single memristor memory cell [5], [6]. Since HP announced the fabrication of memristor in 2008 [3], several papers have been published on a single bit and multi-bit memristor memory realizations. Despite the many features of the memristor, memristors are still remaining at an early stage due to several weaknesses in practice. These weaknesses come from the non-linearity characteristics that make it difficult to determine the proper pulse to achieve the desired states [5]. Therefore, it has been considered as a problem for multi-bit memory designs.

Typical read methods include comparing the resistivity of the selected memory against the reference resistor to determine the current state for single bit memristor [7]. The limitation for this approach is the complexity when designing multi-bit memristor memories because 2n comparisons and 2n reference resistors are required between the stored state and the upper/lower bound for all possible states ; where n: represents the number of bits [6], [10]. In order to support memristor as an emerging memory technology, the cell should be read with circuits that exhibit low mismatch and operate at low voltage operation, less complexity, fast, and compatibility with digital designs. One electric circuit noted for this demeanor is the time to digital converter (TDC) [13]. In addition, representing a signal as a delay better serves the essential multiplexing operation of memory technology [13].

In this paper, a read technique based on time based ADC that supports multi-bit storage per cell with enough margin to detect the stored state digitally, and reduce the complexity of the used hardware. Moreover, by utilizing a transistor as a selector device and the memristor as a storage element for RRAM array, the sneak path current during reading operation is decreased through proper sizing of the used transistor [11].

II. MEMRISTOR MODEL

The total resistance of the memristor is the sum of the resistances of two layers; one layer has a high concentration of dopants and the other layer has a low concentration. The total resistance of Memristor is given as:

$$R = \frac{w}{D} R_{ON} + (1 - \frac{w}{D}) R_{OFF} \qquad (1)$$

Where w is the width of the doped region, D is the total length of the thin film, R_{ON} is the lowest resistance when $w = D$ and R_{OFF} is the highest resistance when $w = 0$.

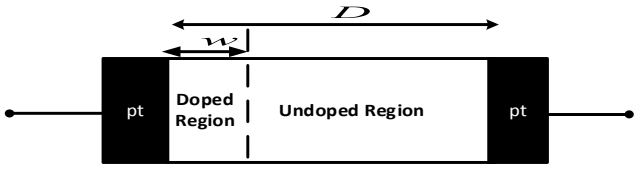


Figure 1. Memristor Device Structure.

III. PRELIMINARIES

A. Memristor Cell Srtucture

The structure of the 1T1M RRAM cell is a mimic to the structure of the DRAM cell and consists of a memristor as a storage element and the transistor acts as an access switch. The memristance is a function of the state variable [2], therefore, it can be divided into several resistance ranges [2], [9]. For a single bit memristor, the region for writing and reading '0' or '1' is bounded by one threshold that is selected to be midway between R_{ON} and R_{OFF} as displayed in Figure 2.

Figure 2. Memristor storing 1–bit value.

For multi-bit memristor memory cell, the cell is divided into 2^n equal regions. For example the 3-bits Memristor is divided into eight equal regions, where each region is assigned a 3-bits word. This division is referred to be a uniform state division. Figure 3 shows, the threshold value for these regions (i.e., T1, T2 …. and T7) and their mean values (i.e., M1, M2….and M8).

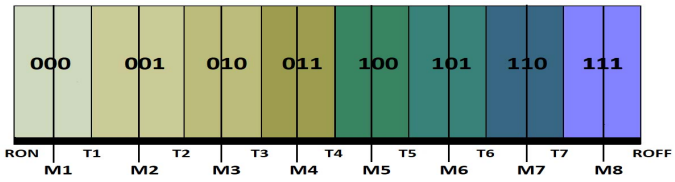


Figure 3. Memristor storing 3-bits value.

B. *Architecture Array*

The proposed architecture of 1T1R memory array presented in Figure 4. The 1T1R array is the main storage area. The read interpreted circuit is connected serially to the selected column to perform a read operation. The address decoder selects which column should be read from the array. The column switch connects the required column to the divider sensing resistor and (T-ADC) circuit that converts the analog voltage that represents the stored data into digital bits.

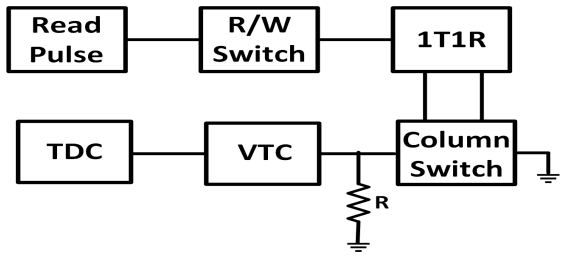


Figure 4. Proposed block diagram for reading operation.

IV. PROPOSED DESIGN

The proposed read sensing circuit aims to eliminate the hardware complexity. The proposed circuit deals with the memristor as single bit and multi-bit memristor memory cell, based on simple circuit of (T-ADC) with 200 mV dynamic range.

A. *The T-ADC Read Path*

Figure 5 presents the T-ADC read path and the accompanying timing diagram shown in Figure 6, describing the sequence of input signals at each stage. To perform a read operation for the selected cell a voltage VG is applied to the word line and a read pulse VD is applied to node D with the same duration. Depending on the stored data (i.e., the resistance of the memristor) the bit line charges to one of the 2^n unique voltage levels corresponding to one of the 2^n states. in order to perform correct read operation the voltage swing at node 'X' between reading distinct binary stored data in form of different resistance states, should be large enough for the two states to be easily distinguishable. These interpreted voltages that start from a value of 385 mV to 585 mV appear on the bit line. The smallest change that is measured by the voltage to time converter (VTC) circuit is given as :

$$Resolution = \frac{Dynamic\ Range}{2^n} \qquad (2)$$

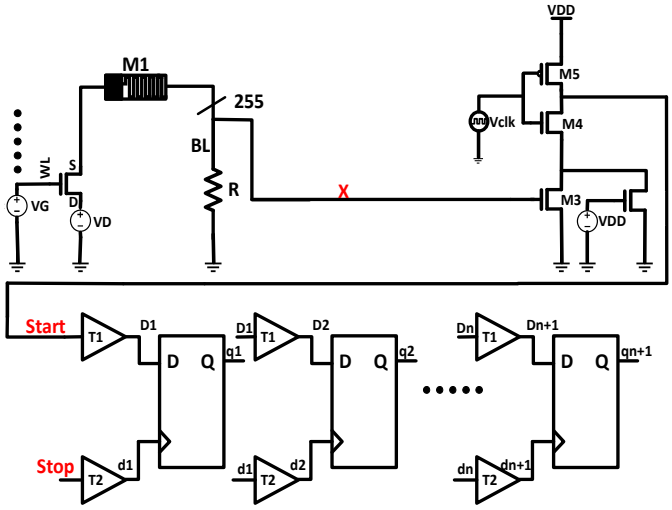


Figure 5. The simplified schematic of time to digital read path.

The Analog voltage that represents the memristor state at node 'X' controls the delay of the falling edge of the clock signal, Vclk; through the inverter (Transistors M4 and M5), by controlling the discharging current of transistor M3 [14]. According to the stored data the starved inverter generates the unique corresponding delay.

Next stage is the (TDC) circuit that converts the output delay produced by the starved inverter into the thermometer code that is encoded into binary code through a time to digital converter using vernier delay line. This vernier delay line consisted of 2 parallel delay chains and sense amplifier based on D-flip flops [15]. The stop signal is the reference signal. The signals (start, stop) travel through these delay chains until they become aligned. The D-flip flops sense amplifier determines which of the two input signals comes first and produces the thermometer code. Fundamentally, the TDC sensing circuit needs only a starved inverter and the numbers of flip flops are determined according to this formula: 2^n -1; where n: represents the number of bits.

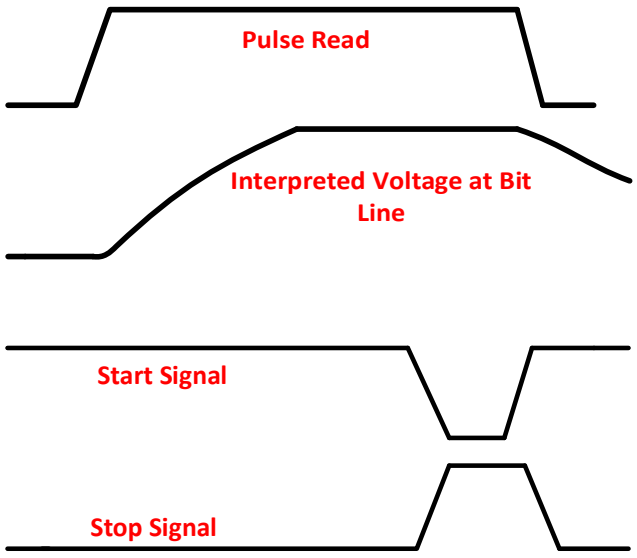


Figure 6. Timing diagram for the proposed circuit.

V. SIMULATION RESULTS

The proposed read circuit behavior is verified using Cadence Spectre simulation tool and the TSMC 130nm CMOS technology. The ThrEshold Adaptive Memristor Model (TEAM Model) for the memristor is used with the proposed circuit. For more information on the TEAM model; please refer to [4].

1) READ Simulations

The following values were used R_{OFF} = 200 KΩ, R_{ON} = 100 Ω for M1, and R = 400 KΩ, Read pulse magnitude = 600 mV, Read pulse duration = 100 ns, Dynamic Range = 200 mV, Time Resolution = 6 ps. In these simulations, it is assumed that the Memristor cell stores 3-bits (i.e., 8 resistive states) and the circuit objective is to read the stored data. This stored data corresponds to a certain voltage level at bit line (at node 'X') and this level of voltage considered within the voltage ranges of T-ADC as shown in Table.1

TABLE.1 the output voltages for different states of the memristor.

State	Voltage range of T-ADC	Volt at node 'X'
000	385 m V – 409 m V	407 m V
001	410 m V – 434 m V	425 m V
010	434 m V – 460 m V	445 m V
011	460 m V – 485 m V	467 m V
100	485 m V – 510 m V	491 m V
101	510 m V – 535 m V	517 m V
110	535 m V –560 m V	547 m V
111	560 m V – 585 m V	580 m V

This level of voltage is then given to the VTC circuit to operate on it and represent the corresponding unique delay as shown in Figure 7, the outputs of VTC are 8 different delays based on 8 resistive states of the Memristor cell with time resolution of 6 ps. In order to get the ordinary 3-bits binary code, a simple adder circuit is used that takes the 7-bits of the thermometer code, adds them together to get the equivalent binary code (i.e., this adder converts the thermometer code to the 3-bits corresponding word). Moreover, the results confirm that the reading operation does not change the internal state of Memristor as shown in simulation results showing only four cases Figure 8, Figure 9, Figure 10, and Figure 11.

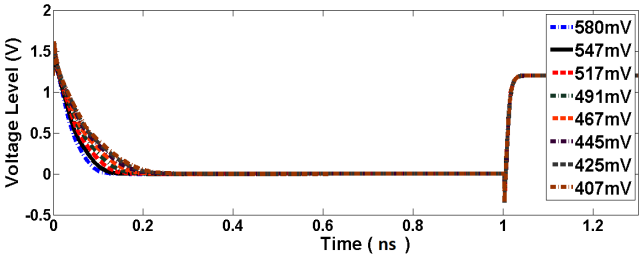
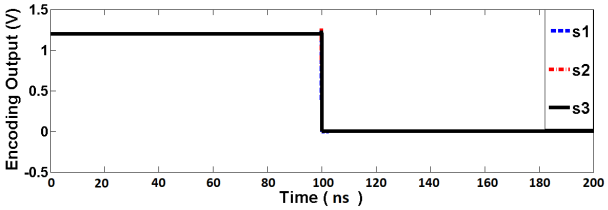


Figure 7. Output wave form of starved inverter at different input voltage in case of 3-bits.



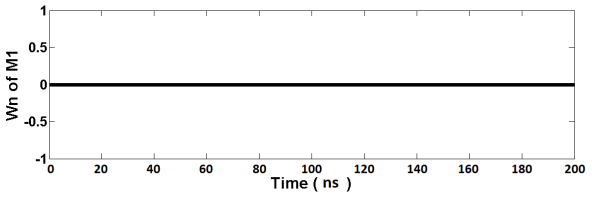
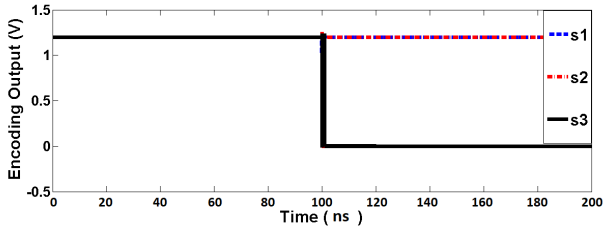


Figure 8. Reading state of M1 in case of 000.



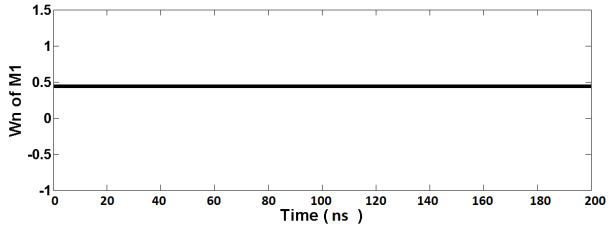
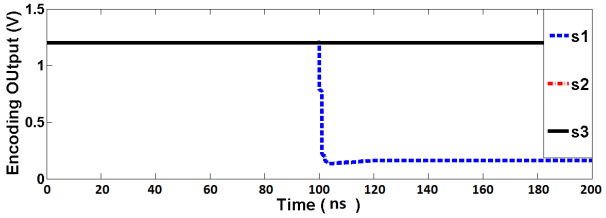


Figure 9. Reading state of M1 in case of 011.



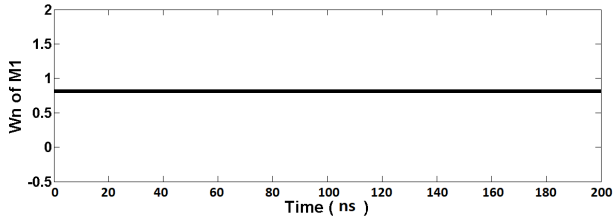
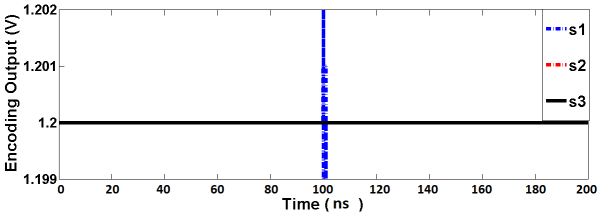


Figure 10. Reading state of M1 in case of 110.



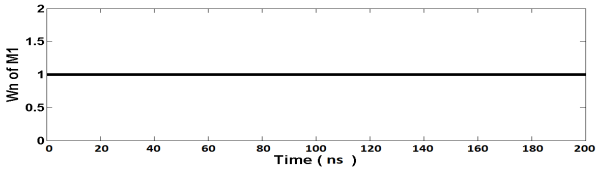


Figure 11. Reading state of M1 in case of 111.

By increasing the numbers of cells the interpreted voltage may not reach the expected level of voltage as result of the large capacitance on the bit line. Therefore the pulse read duration should be increased. Table.2 represents the number of memory cells that T-ADC sensing circuit supports and the required read pulse duration in each case.

TABLE.2 shows number of cells that can be supported by T- ADC.

Read Pulse Duration	Number of Cells
1 ns	3
2 ns	6
3 ns	9
4 ns	12
5 ns	16
6 ns	19
7 ns	22
8ns	25
9 ns	28
10 ns	31
100 ns	256

Table.3 shows the effect of the transistor when added to the memristor as a selector device to form 3×3 crossbar. A read operation is then operated in comparison with the crossbar pure memristor without any selector device. Simulations are shown in Table.3 output current is used to determine ON/OFF state stored in memory cells, I_{ON} and I_{OFF} indicate the resulted output currents when reading an ON-state or OFF-state. As indicated in Table.3 the effect of sneak path current is greatly noticed in pure crossbar when reading the ON state and all the other cells are ON/OFF there is large difference between the reading values: 3.74 u A and 1.97 m A. By adding the transistor to the memristor as a selector device, the effect of sneak path current is decreased through proper sizing of the used transistor and the current values are considered the same: 666.7 n A in case of the selected cell is ON- State and all other cells are ON/OFF and this noticed in table.3. Also indicated in table.3 that the power consumption is decreased greatly when transistor added to the memristor.

TABLE.3 comparison between the performance of cross bar and 1T1R

Aspects	**Crossbar Structure**	**1T1R**
I_{ON} all other cells off	3.749 u A	666.7 n A
I_{ON} all cells on	1.972 m A	666.7 n A
I_{OFF} all other cells on	1.501 u A	501.6 n A
I_{OFF} all cells off	1.073 u A	506.5 n A
I_{ON} range	3.75 u A to 1.97 m A	666.7 n A
I_{OFF} range	1.073 u A to 1.501u A	501.6 n A to 506.5 n A
Power range	643.8 n W to 1.18 m W	300.96 n W to 400.02 n W

VI. CONCLUSION

In this paper, a read circuit for multi-bit Memristor-based memory cell is presented and discussed. Eliminating the dependency on the op-amp circuits and analog circuits is the significant of the proposed time-based read circuit. Moreover this sensing scheme (time to digital converter) supports the class of semiconductor memories to achieve their full potential.

ACKNOWLEDGEMENT

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