A Single-Wavelength Photonic Network on Chip Design Based on Optical Orthogonal Codes

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***Abstract*—Silicon photonic-based interconnects are becoming a very promising solution for multi-core system on chip (SoC) platforms. In this paper, a novel photonic network on chip (PNoC) design for multi-core SoC is proposed, based on optical code-division multiple-access (OCDMA) using a single on/off-chip laser diode (LD). The proposed design offers a much lower optical power consumption, and consequently, cost, as compared to the state-of-the-art PNoC designs, in which multiple on/off chip LDs are usually utilized. The core-to-core communication over the proposed PNoC is simulated, with the bit error rate (BER) as the performance metric of interest. Simulation results confirm the analytical BER expressions and show that an error free core-to-core transmission is achieved.**

***Index Terms*—Optical code division multiple access (OCDMA), optical orthogonal codes (OOCs), photonic network on chip (PNoC), system on chip (SoC).**

I. Introduction

Multi-core SoC architectures are becoming an attractive platform for high-speed processing applications. In these architectures, a huge amount of information, typically several tens of Gbits, should be processed and exchanged under power budget constraints. Unfortunately, core-to-core communications is responsible for about 25% of the entire available power budget consumption due to the high ohmic loss exhibited by metallic interconnects. Moreover, the capacitive coupling, resulting form the high dense packing of these metallic interconnects, tends to limit the core-to-core transmission bit rate and increases the delay. Accordingly, it is highly desirable to dedicate this relatively large proportion of the consumed power to the computational effort of the multiple cores to improve the per-watt performance of the entire SoC under power budget constraints.

In the past few years, large scale silicon photonic integrated circuits (PICs) have emerged as a promising solution for high speed, low delay and power economic SoC interconnects for microelectronic integrated circuits. On the chip level, core-to-core optical interconnects, based on silicon photonic waveguides, in which the optical loss is essentially independent of the core-to-core distance, whether the two cores are 2 mm or 2 cm distance apart. Due to their numerous advantages, several approaches have been proposed to offer energy efficient high-bandwidth connectivity via a PNoC for multi-core platforms. The common principle behind these approaches is the orthogonalization of mutual core signals represented in different signal spaces to increase the diversity of the PNoC. In [1], for instance, space-time domain arbitration of core-to-core signals over the PNoC has been applied to achieve the diversity of the optical interconnect network. Unfortunately, the major limitation associated with this approach is that, a perfect synchronisation among the communicating cores and the PNoC switching elements is required. The complexity of this requirement, measured by the number of the required time slots, is $\mathcal{O}(N^2)$, where N is the number of switching elements in the PNoC. In [2], core-to-core signals are routed over a single wavelength multimode PNoC at a transmission rate of 100 Gbps/mode, based on mode division multiplexing (MDM). However, a minimum BER of only 1e-4 has been achieved using this technique, due to the cross talk exhibited by adjacent mode channels. A PNoC, based on the wavelength division multiplexing (WDM) of eight LDs in the wavelength domain, with an overall capacity of 320 Gbps, has been experimentally demonstrated in [3]. In this technique, the limited cross talk, down to -28 dB, among mutual adjacent wavelength channels relies on the liberty of the power budget constraints as required by the eight LDs. Although bandwidth efficient, the robustness of this design against a limited power budget is not guaranteed in a power constrained multi-core system. The expected consequences of this liberty is an unavoidable degradation of the per-Watt performance of the processing cores.

From a communications mathematics perspective, it can be observed that the ultimate capacity of a photonic link is approached by the aforementioned techniques by orthogonalizing the core-to-core signals in the time, space, wavelength and mode domains. Nevertheless, increasing the channel capacity via code division multiple access has been a successful orthogonality-based diversity technique that has been transferred from the narrowband to the broadband communications regime. In these techniques, the energy and bandwidth efficient utilization of a channel connecting the individual transceiver pairs depends only on the orthogonality properties of the codes assigned to these pairs without the need for tedious time, space and/or wavelength resource allocation and scheduling algorithms.

In [4]-[6], OOCs have been introduced as a suitable orthogonalization set for OCDMA systems in a shared fiber optic link. In this paper, a novel PNoC design is presented based on the code dimensionality of core-to-core signals in

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a single wavelength photonic routing channel. The rest of this paper is organized as follows. In Section II, the proposed PNoC architecture is presented and its principle of operation is mathematically modelled. The BER performance of the proposed PNoC is simulated in Section III and the simulation results are analyzed. Finally, the main conclusions are drawn in Section V.

II. Proposed PNoC Architecture: System Level Modelling

Fig. 1 (a) depicts a general block diagram representation for a multi-core SoC based on PNoC routing. On the system level, the SoC architecture consists of a number of on-chip processing cores, a PNoC and an electronic router (ER). The basic building blocks of the PNoC are one or more on/off-chip LDs, a photonic switching element array, a silicon photonic waveguide and a high-speed photodetector (PD) as depicted in Figs. 1 (b)-(d). The traffic exchanged by the processing cores over the PNoC is regulated by the ER, which controls the switching processes of the input-output (I/O) ports of each core. Once established, a transparent error free core-to-core photonic link should be secured by the ER and dedicated to each individual core pair.

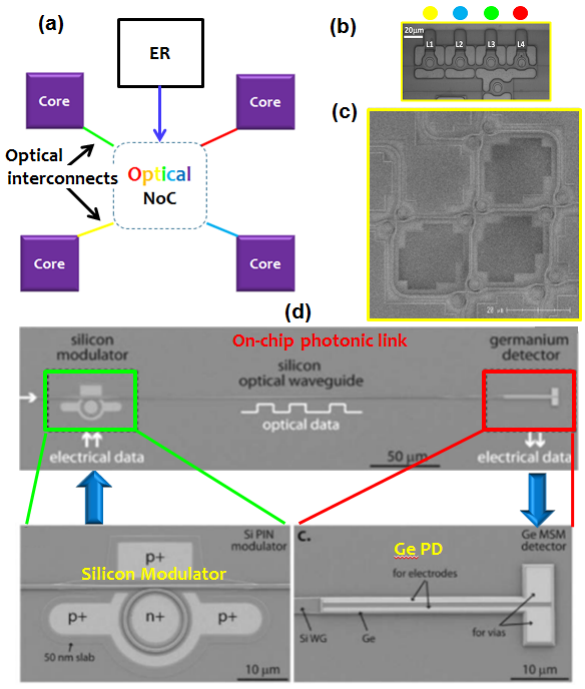

Fig. 1. Typical architecture and basic building blocks of PNoCs. (a): Block diagram of an electronic controlled optical routing network on chip. (b): four wavelength array of on-chip LD (from [7]). (c): an array of photonic switching elements (from [8]). (d): a typical on-chip photonic link, based on a single wavelength LD, a direct path silicon photonic waveguide and a Germanium-based photodetector (from [9]). ER: electronic router.

A. Core Traffic Multiplexing Based on OOC

As illustrated in Fig. 2, the first (multiplexing) part of the proposed PNoC design consists of a single monochromatic continuous wave (CW) LD, a number of M hybrid (optoelectronic) three inputs AND gate and a set of M OCC optical generators. A unique OOC $\psi_m(t) = \sum_{q=0}^{N_c-1} \phi_{m,q} w(t - qT_c); \phi_{m,q} \in \{0,1\}$ and $w(t)$ is an amplitude normalized optical encoding waveform, consisting of N_c chips and selected from an orthonormal distinct code set $\{\psi_1(t), \psi_2(t), ..., \psi_M(t)\}$, is dedicated to each of the M processing cores, once an information bit is received from the relevant core output port. The uniqueness of each OOC assigned to each core is distinguished by the positions of the 1's chips within this OOC. The process of encoding an information bit by an OOC is gated by the ER via a hybrid optoelectronic AND gate. The information bit streams, emitted by each of the M cores are encoded by their relevant optically generated OOCs and are combined by an M:1 optical coupler. The resulting signal, $s(t)$, is propagated down a silicon photonic waveguide and is mathematically expressed as follows:

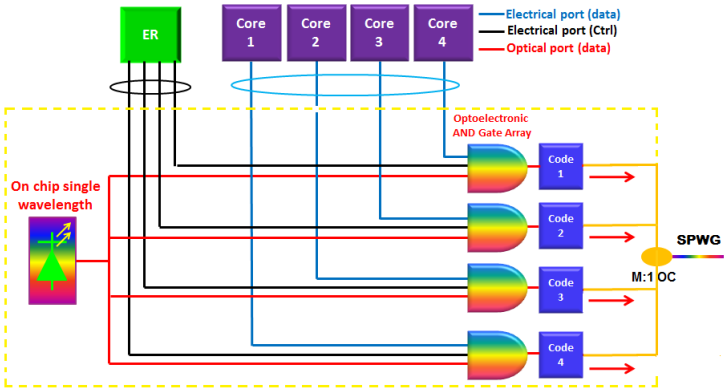

Fig. 2. Schematic diagram of the transmitter part of the proposed PNoC design. OC: optical coupler. By definition, an optoelectronic AND gate operates on electrical and optical logic inputs and generates only an optical logic output.

$$s(t) = \sum_{j=-\infty}^{\infty} \sum_{m=1}^{M} \sum_{q=0}^{N_c-1} b_{j,m} \phi_{m,q} w(t - qT_c - jT_b) \quad (1)$$

where $b_{j,m} \in \{0,1\}$ is the j^{th} bit, emitted by the m^{th} core to the silicon photonic waveguide. It should be noted that, the propagating OOC encoded bits emitted by the different cores can be either synchronous or asynchronous.

B. Core Traffic De-Multiplexing and Post Photodetection Processing

The receiver part of the proposed PNoC design is illustrated in Fig. 3. As shown in Fig. 3 (a), at the output port of the silicon photonic waveguide, $s(t)$ is divided by an 1:M optical divider into M identical branches, each of which is forwarded to one of the input ports of an $M \times M$ photonic switching element array, whose operation is best described by an $M \times M$ switching matrix $\mathbf{S}$. The value of the general

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entry $(\mathbf{S})_{mn} \in \{0,1\}$ describes the connection status of the (m^{th}, n^{th}) photonic switching element between the output of the m^{th} core and the input of the $n^{th}; m \neq n$, where 1 denotes a connected core pair, 0 denotes a disconnected pair and $(\mathbf{S})_{mn} = 0; m = n$. Once connected, a photonic switching element enables a transparent link between the output of a source core and the PD of a destination core via the silicon photonic waveguide. The photodetected signal is then applied to a correlator after being multiplied by a scaled optical replica of $\psi_m(t)$ and integrated over each bit duration. The result of integration at the correlator output is sampled and dumped every T_b seconds and is expressed as follows:

$$z_{j,m} = \left(\frac{G\Re}{\sqrt{M}}\right) \int_{t_o}^{t_o+T_b} s(t)\psi_m(t - jT_b)dt \qquad (2)$$

where $z_{j,m}$ is the sampled output of the m^{th} correlator, $\Re$ is the responsitivity of the PD and G denotes the gain of the active OpAmp integrator. To simplify the analysis, it is assumed that $G\Re/\sqrt{M} = 1$. The binary value of $b_{j,m}$ is estimated from the samples $z_{j,m}$ by the decision threshold as follows:

$$\widehat{d}_{j,m} = \frac{1}{2}\left(\text{sign}(z_{j,m} - V_{Th}) + 1\right) \qquad (3)$$

where sign(.) is the conventional signum function, defined as sign(x)= 1; $x \geq 0$, sign(x)= -1; $x < 0$ and V_{Th} is a fixed threshold voltage level. Since any of the M on-chip cores can arbitrarily access the PNoC for a transmit and/or a receive process, synchronous and/or asynchronous core-to-core transmission modes are two possible scenarios. According to [6], the BER of a transparent optical link, shared by OOC transceivers is attributed to the common positions of the 1's chips. For synchronous and asynchronous optical channel access, the BER is denoted by P_e^S and P_e^A, respectively, and is given by the two following relations:

$$P_e^A = \frac{1}{2}\sum_{m=1}^{M-1} \binom{M-1}{m} \left[\frac{w^2}{2N_c}\right]^m \left[1 - \frac{w^2}{2N_c}\right]^{M-m-1} \qquad (4)$$

$$P_e^S = \frac{1}{2}\sum_{m=1}^{M-1} \binom{M-1}{m} \left[1 - \frac{w^2}{2N_c}\right]^{M-m-1} Q\left(\frac{V_{Th} - m}{\sqrt{m/12}}\right) \qquad (5)$$

where M is the number of cores, w is the code weight, defined as the number of 1's chips in the OCC, N_c is the total number of chips in an OOC and V_{Th} is the threshold voltage, $Q(x)$ is the conventional Gaussian Q-function, defined as follows:

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty \exp\left(-u^2/2\right) du \qquad (6)$$

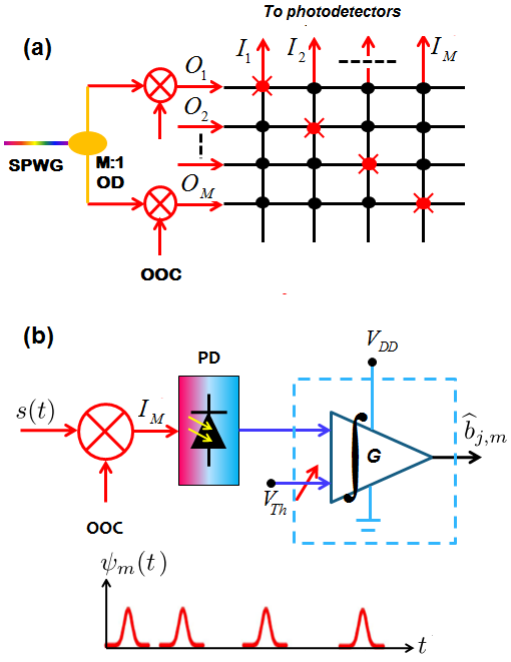

Fig. 3. Schematic diagram of the receiver part of the proposed PNoC design. (a): an $M \times M$ passive photonic switching element array. Black dots: ON/OFF mode photonic switching elements. Red dots: only OFF mode photonic switching elements. (b): post photodetection processing at the receiver side. OD: optical divider. SPWG: silicon photonic waveguide.

III. Simulation Results and Analysis

In this section, the BER expressions in (4) and (5) are numerically evaluated with respect to M and V_{Th}. The values of the simulation parameters are as follows: $w = 4, N_c = 217$, and M take values through $2, 3, ..., 16$, while V_{Th} is varied over the range of 1 V - 5 V to ensure that it covers the voltage levels required by CMOS and TTL-based technologies. Moreover, Table I lists the 16 OOCs, assigned to each of cores that access the common silicon photonic waveguide.

TABLE I
Positions of 1's chips in the routing OOC codes assigned to OCDMA cores

Core ID	Positions of 1's	Core ID	Positions of 1's
C_1	$\{1, 2, 16, 106\}$	C_9	$\{1, 17, 26, 70\}$
C_2	$\{1, 3, 59, 143\}$	C_{10}	$\{1, 19, 29, 71\}$
C_3	$\{1, 4, 42, 65\}$	C_{11}	$\{1, 21, 32, 72\}$
C_4	$\{1, 5, 18, 107\}$	C_{12}	$\{1, 27, 95, 130\}$
C_5	$\{1, 6, 61, 144\}$	C_{13}	$\{1, 28, 78, 125\}$
C_6	$\{1, 7, 44, 66\}$	C_{14}	$\{1, 30, 97, 131\}$
C_7	$\{1, 8, 20, 108\}$	C_{15}	$\{1, 31, 80, 126\}$
C_8	$\{1, 9, 63, 145\}$	C_{16}	$\{1, 33, 99, 132\}$

Fig. 4 shows the BER performance versus the number of cores M, communicating in the synchronous and asynchronous transmission modes at a fixed threshold of $V_{Th} = w = 4$. Clearly, a completely error free (i.e., zero BER) core-to-core transmission is achieved using three and five cores considering

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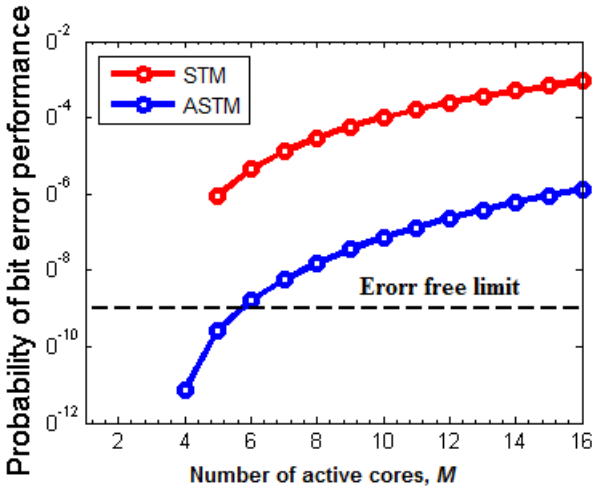

Fig. 4. BER performance versus the number of active cores, M sharing the PNoC. STM : synchronous transmission mode. ASTM : asynchronous transmission mode.

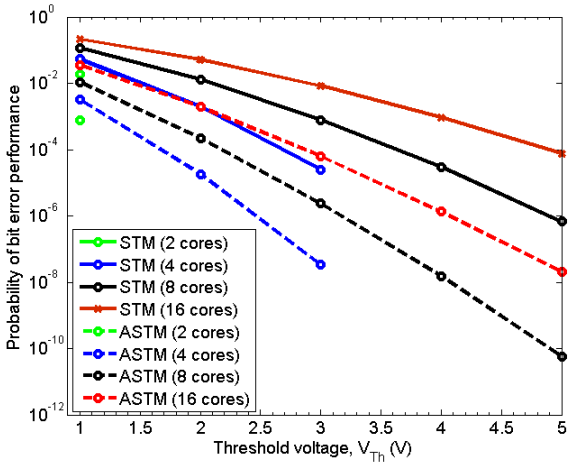

Fig. 5. Impact of threshold variation on the BER performance of OCC-based PNoC for cores operating in the synchronous and asynchronous transmission modes.

asynchronous and synchronous transmission modes, respectively. However, error free transmission, corresponding to a BER of 1e-9, is achieved only if the PNoC is utilized by five active cores. Accordingly, it can be correctly concluded that a minimum BER can be achieved iff the synchronization, on the bit level, among different cores is guaranteed by the ER.

On the other hand, Fig. 5 plots the variations of the BER performance versus the threshold voltage V_{Th}. Clearly, a completely error free two core operation is achieved beyond a threshold voltage of 1 V , weather the two cores are operating in the STM or the ASTM transmission mode. However, the same BER performance can be achieved in a four cores scenario, provided that the threshold voltage just exceeds 3 V. These two cases recommend the CMOS-based technology when implementing the ER. However, a completely error free transmission cannot be achieved if the proposed PNoC is accessed by more than two cores simultaneously. For a given threshold voltage, except for the two cores access scenario, the BER performance is degraded by increasing the number of active cores as well as their mode of operation. In this case, the BER is decreased by increasing the threshold voltage the threshold voltage and is determined by the adequate BER performance as determined by the PNoC designer.

IV. Conclusion

This paper presents a novel and power efficient photonic network on chip design for a multi-core system on chip. The key idea of the proposed design relies on increasing the diversity of a single wavelength photonic link by employing the optical code division multiple access technique using optical orthogonal codes. The impact of several design parameters on the bit error rate performance of the proposed design is simulated. Simulation results show that error free mutual core-to-core links can be established by the proper control of these design parameters.

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