Read Disturbance and Temperature Variation Aware Spintronic Memristor Model

Sherif F. Nafea¹, Ahmed A.S. Dessouki², S. El-Rabaie³, Kh.El-Barbary⁴, Hassan Mostafa⁵
¹,⁴ Electrical Engineering Dept., Faculty of Engineering, Ismailia, Suez Canal Univ., Egypt.
² Electrical Engineering Dept., Faculty of Engineering, Port Said, Port Said Univ., Egypt.
³ Electronics and Electrical Communications Dept., Faculty of Electronic Engineering, Menoufia University, Menouf, Egypt.
⁵Electronics and Communications Engineering Department, Cairo University., Egypt.
Emails: sheriff_kamel@eng.suez.edu.eg, dessouki2000@yahoo.com, srabie1@yahoo.com, hmostafa@uwaterloo.ca

Abstract— A novel nonvolatile memory technology is needed to meet the increasing demand of large storage elements. Spintronic memristor is a promising candidate for emerging memory technologies. The spintronic memristor combines the non-volatility advantage of memristors, the good scalability, and radiation hardness of spin-transfer torque magnetic random access memories (STT-MRAMs). In this paper, a modified model of the spintronic memristor device is proposed. The model takes into account the read disturbance, and the temperature variation in spintronic memristor-based memory cells.

Keywords— nonvolatile memory; Spintronic memristor; modeling; read disturbance; temperature variation.

I. INTRODUCTION

In 1971, Professor Leon Chua predicted the existence of a forth two-terminal passive element that completes the missing link between the electric charge (q), and the magnetic field (Φ) as shown in Fig. 1 [1]. He called it the “memristor” which is an abbreviation for memory-resistor.

Memristors have unique properties that permit great opportunities in future memory design. They offer excellent scalability, and non-volatility properties, leading them to become one of the main promising candidates for the next-generation high-performance high-density storage technology. In 2008, HP labs announced a physical realization of a solid-state memristor using TiO₂ [2]. The HP memristor’s basic structure is shown in Fig. 2. It consists of a layer of TiO₂ sandwiched between two Platinum electrodes. The TiO₂ layer is divided into two parts -doped and undoped. The bound between the doped and undoped TiO₂ is called “domain-wall”. The domain-wall’s position (state) is changed under the effect of the applied voltage or current.

A. Spintronic Memristor

After the HP memristor, many devices have been submitted as a physical realizations of the memristor [3]–[5]. One of the most promising realization of the memristor is the domain wall spintronic memristor [6], which is the main focus of this work.

The device is divided into two layers as shown in Fig. 3. A reference or a pinned layer (PL), and a free layer (FL). The magnetization direction in the reference layer is fixed. The position of the domain-wall in the free layer can be changed by passing a driving current, and hence the total memristance of the device changes.
unplugged from a power source. It also has the advantages of Magnetic random-access memories (MRAM) such as radiation hardness, and mature memory technology. Thus, the spintronic memristor-based memory devices could be the future of the non-volatile memories.

B. Previous model

The model of the spintronic memristor that is modified in this work was proposed in [7]. It uses \( r_L \) and \( r_H \) to denote the values of the resistance per unit length of the spintronic memristor at the low-resistance and the high-resistance states, respectively. The memristance of a spintronic memristor can be calculated as [7]:

\[
M(x) = r_L x + r_H (D-x)
\]

where \( x \) is the position of the domain-wall, and \( D \) is the length of the device. The domain-wall velocity \( (v) \) is proportional to the effective current density \( J_{\text{eff}} \) [7], i.e.

\[
v = \frac{dx}{dt} = \Gamma_v J_{\text{eff}}
\]

where the effective current density \( J_{\text{eff}} \) only affects the domain-wall position if it is greater than a specific critical value \( J_{cr} \).

\[
J_{\text{eff}} = \begin{cases} J, & J \geq J_{cr} \\ 0, & J < J_{cr} \end{cases}
\]

From equation (3), it is obvious that this model did not include an important phenomenon that occurs in all Magnetic Tunneling Junction (MTJ)-based structures which is denoted by the thermal fluctuation. This model needs to be modified to include this important phenomenon. The proposed modified model is implemented in a Verilog-A code, thus it can be integrated with SPICE-based CAD tools to carry out any desired analyses of different circuits that utilize the spintronic memristor.

C. Thermal fluctuation

Experimental studies of MRAM structures show that increasing the temperature of MRAM cells increases the probability of the cell switching between the parallel and the antiparallel states [8]. The thermal fluctuation becomes a disadvantage during the reading process as it can cause an undesirable switching to the data stored in the MRAM cell.

The probability that an MRAM cell switches its state after a duration time \( (t) \) is calculated by [9]:

\[
P(t) = 1 - \exp \left( -\frac{t}{\tau_{P\rightarrow AP}} \right)
\]

where \( \tau_{P\rightarrow AP} \) is the Neel-Brown relaxation time of an ensemble in an initial parallel state and can be calculated as[8]:

\[
\tau_{P\rightarrow AP} = \tau_0 \exp \left[ \frac{K_u V}{k_B T} \left( 1 + \frac{H(t)}{K} \right)^2 \left( 1 - \frac{H(t)}{H_{cr}} \right) \right]
\]

where \( H(t) \) is the applied magnetic field, \( I(t) \) is the applied current, \( \tau_0 \) is the nominal switching time when a current equals to \( I_c \) is applied to the cell, \( K_u \) is the anisotropy constant, \( V \) is the volume of the MRAM cell’s (memristor’s) FL, \( K_B \) is the Boltzmann constant, and \( T \) is the absolute temperature in Kelvin.

Equations (4) and (5) show that increasing the temperature increases the relaxation time \( (\tau_{P\rightarrow AP}) \), which increases the probability of the MRAM cell switching. This effect occurs in both writing and reading processes.

II. PROPOSED MODEL

The spintronic memristor model presented in [7] assumed that when the current density is less than a specific critical value \( J_{cr} \), then no change occurs to the domain wall position. According to this assumption, if the current used to read the data stored in a spintronic memristor-based memory cell is smaller than this critical value \( (I_{read} < I_{cr}) \), then the data stored within the cell is not affected by the reading process. Correspondingly, there exists no read disturbance regardless of the number of successive read cycles or the operating temperature value.

However, as reported in [8], it is shown that even if the applied current is less than the critical current, the data stored in the memory cell is changed due to the thermal fluctuation [8].

From equation (4), the probability of switching the cell state during the read process is [11]:

\[
P_{\text{failure}} = 1 - \exp \left( -\frac{t_p}{\tau_{P\rightarrow AP}} \right)
\]

where \( t_p \) is the duration time when \( I_{\text{read}} \) is applied to the memristor that achieves a full memristor state switching (i.e., switching the memristor from the low-resistance state to the high-resistance state). In case of successive read cycles, \( t_p \) becomes the total duration of the successive read pulses required to have a full switching in the memristor state. In absence of external applied field \( (H(t)=0) \), \( \tau_{P\rightarrow AP} \) defined in (5) is reduced to [11]:

\[
\tau_{P\rightarrow AP} = \tau_0 \exp \left[ \frac{K_u V}{k_B T} \left( 1 - \frac{I_{\text{read}}}{I_{cr}} \right) \right]
\]

Equation (6) shows that when the summation of the read pulses durations, and consequently the number of read cycles, increases, there are a high probability that the domain wall switches its state from parallel to anti-parallel or vice versa. In other words, the memristor switches its state even if the read current \( (I_{\text{read}}) \) is lower than the critical current value \( (I_{cr}) \) especially, for large number of successive read operations. Equation (7) shows that increasing the temperature decreases the duration \( (\tau_{P\rightarrow AP}) \) and thus increasing the probability of failure. The term \( (K_u V/K_B T) \) is considered as a “stability factor” to the memory circuit.

Equation (7) also shows another important design factor, which is the ratio between the read current \( (I_{\text{read}}) \) and the critical current \( (I_{cr}) \). Decreasing the term \( (I_{\text{read}}/I_{cr}) \) gives a better stability against thermal fluctuation.

These model modifications have a great significance on the analysis of the memory reading process, and can be used to define the maximum allowable successive read cycles before the stored data in the spintronic memristor is disturbed.

Now we need to modify the model in [7] to take into account the effect of thermal fluctuation. Instead of assuming that \( J_{\text{eff}} \) equals zero for \( (J<J_{cr}) \) as in [7], the thermal fluctuation effect on \( J_{\text{eff}} \) is taken into account in the modified model.
From its definition, \( \tau_0 \) is the switching time when a current of magnitude equal to \( I_{cr} \) is applied to the cell. Based on (2) we can write that:

\[
\int_0^D dx = \int_0^{\tau_0} \Gamma_v J_{cr} dt
\]

This equation gives that:

\[
D = \Gamma_v J_{cr} \tau_0
\]

Now we need to define the value of \( J_{eff} \) that achieves the same full switching in a duration time equals to \( \tau_p \). Thus from (2) we can write that:

\[
\int_0^D dx = \int_0^{\tau_p} \Gamma_v J_{eff} dt
\]

This equation gives that:

\[
D = \Gamma_v J_{eff} \tau_p
\]

Equating (9) and (11) gives that the equivalent effective current density for the thermal fluctuation is:

\[
J_{eff} = \frac{I_{cr} \tau_0}{\tau_p}
\]

Thus, the value of \( J_{eff} \) in (3) is modified to be:

\[
J_{eff} = \begin{cases} 
\frac{\int_0^{\tau_p} \Gamma_v J_{eff} dt}{\int_0^{\tau_p} \Gamma_v J_{cr} dt} & \text{if } \int_0^{\tau_p} \Gamma_v J_{eff} dt \geq \int_0^{\tau_p} \Gamma_v J_{cr} dt \\
\frac{\int_0^{\tau_p} \Gamma_v J_{eff} dt}{\int_0^{\tau_p} \Gamma_v J_{cr} dt} & \text{if } \int_0^{\tau_p} \Gamma_v J_{eff} dt < \int_0^{\tau_p} \Gamma_v J_{cr} dt
\end{cases}
\]

where \( \tau_p \) can be calculated from (6) for a given design parameter (\( P_{failure} \)), as follows:

\[
\tau_p = \tau_{p \rightarrow AP} \ln \left( \frac{1}{1 - P_{failure}} \right)
\]

III. SIMULATION RESULTS

The spintronic memristor’s material properties and model parameters are taken from [7]. The nominal switching time calculated from (9) is \( \tau_0 = 100nS \). The duration of the read pulse is chosen to be \( \tau_{read}=10nS \) [12] The thermal factor (\( K_I V/KB T \))=50 at room temperature (\( t=27^\circ C \)).

Fig. 4 shows the probability of failure versus the number of cycles that achieves a full switch to the memristor memory cell for different values of \( (I_{read}/I_{cr}) \) at room temperature. The figure indicates that decreasing the read current strongly increases the stability of the memory cell during the read process.

However, decreasing the read current has two disadvantages. First, the sensed voltage difference becomes very small, which reduces the cell’s noise immunity and makes the design of the supporting read circuit very challenging.

To understand this concern, let us study this issue using the read circuit design proposed in [13]. The critical current is \( I_{cr}=35\mu A \), and the two memristance states are \( R_{p}=5K\Omega \) and \( R_{AP}=6K\Omega \). Let us consider \( I_{read}=0.9*I_{cr}=31.5\mu A \). The read circuit is based on comparing the memristance value (\( R_p \) or \( R_{AP} \)) with the average value of the parallel and anti-parallel resistances (5.5 K\( \Omega \)). Thus the voltage difference sensed at the input of the comparator terminals will be \( \Delta V=I_{read}*(R_{AP} - R_{read}) \approx 16mV \). This sensed voltage is too small compared to the comparator offset voltage which is typically larger than 50mV. Accordingly, reducing \( I_{read} \) results in very complex, power consuming, and large area read circuits.

Second, decreasing \( I_{read} \) decreases the speed of the reading process. Therefore, choosing the read current value \( (I_{read}) \) is a trade-off between reducing the thermal fluctuation and achieving a larger sensed voltage difference.

A final remark in Fig. 4 is that the calculated number of read cycles represent total cycles before “full switch”. The reason for this is that the \( P_{failure} \) defined in (6) assumed the probability of failure is the probability of a “full switch” as the phenomenon were studied generally for any Magnetic Tunneling Junction (MTJ) based structure. In case of the domain-wall spintronic memristor, if the memristor state changes from 0% to 50%, then the data stored in the cell is already destroyed. For example at \( P_{failure}=10\% \) & \( I_{read}=0.9*I_{cr} \), data will be destroyed after 80 read cycles only as the state variable \( x \) exceeds 0.5*D.

Fig. 5 shows the relationship between the number of cycles before failure versus the read current ratio \( (I_{read}/I_{cr}) \) under different \( P_{failure} \) values at room temperature. As shown in this figure, in order to achieve less probability of failure, the maximum number of read cycles before failure is reduced. This is a hard limitation on the memory design which must be taken into consideration. In memory design, if the probability of failure is \( P_{failure}=0.1\% \), at \( I_{read}=0.8*I_{cr} \), the maximum number of read cycles before failure is 110.

Fig. 4. Probability of failure versus the number of read cycles before failure

Fig. 5. Calculated number of read cycles before failure versus the read current ratio \( (I_{read}/I_{cr}) \) for different probabilities of failure.
Fig. 6 studies the effect of temperature variation on the maximum allowable successive read cycles versus the read current ratio \( \frac{I_{\text{read}}}{I_{\text{cr}}} \). As shown in this figure, the maximum allowable successive read cycles decreases exponentially with temperature increase. In the design of memory circuits, it is convenient to assume a temperature of around 70°C.

![Graph showing maximum allowable read cycles vs. \( \frac{I_{\text{read}}}{I_{\text{cr}}} \) for different temperatures.]

IV. DESIGN INSIGHTS

From the proposed modified model as well as the presented simulation results, the following design guidelines and insights are extracted to help the spintronic memristor-based memory designers.

1) The read current \( I_{\text{read}} \) should be chosen carefully. Increasing \( I_{\text{read}} \) reduces the stability of the circuit due to thermal fluctuations, and thus reduces the maximum allowable successive read cycles. On the other hand, reducing \( I_{\text{read}} \) reduces the sensed voltage difference, the noise immunity, and the speed of the reading process. Therefore, the selection of the \( I_{\text{read}} \) value is a trade-off between thermal fluctuation impact and the supporting read circuit complexity.

2) Memory circuit design always requires a strict constraint on the allowable probability of failure as it causes a considerable data disturbance. Spintronic memristor based memory designers should define the accepted \( P_{\text{failure}} \) and based on that, the maximum allowed successive read cycles is defined. A refresh scheme is needed to avoid read disturbance. Thus, this model gives the designer an important insight on when the refreshment circuit is required.

3) Temperature variation greatly impacts the probability of failure in spintronic memristor based memories. Spintronic memristor based memory designers should define carefully the expected operating temperature of the memory device.

V. CONCLUSION

In this work, we have proposed a modified spintronic memristor model. The proposed model is used to study the read disturbance in spintronic memristor based memory cells due to the thermal fluctuation. The simulation results show that, for a specific probability of failure during the reading process, there is a maximum allowable number of successive read cycles before failure. These results can be used to define the needed frequency of a data refreshment scheme. It is shown that increasing the read current increases the probability of data disturbance. Also, increasing the operating temperature reduces the maximum allowable successive read cycles before failure.

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