On the use of a programmable front-end for multi-band/multi-standard applications

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Abstract

Modern wireless devices require a compact wireless receiver that can access all the available services with fewer bulky off-chip passive components. This advocates the need for multi-band multi-standard receivers. This paper proposes a reconfigurable such receiver front-end controlled by its driving clocks. The receiver adopts charge sampling and impedance translation techniques. Its driving clocks are adjusted based on the targeted frequency. The receiver is tested over the existing standards specifications: GSM 2G (850 MHz, 900 MHz, 1.8 GHz and 1.9 GHz), UMTS 3G (850 MHz, 1.8 GHz, 1.9 GHz and 2.1 GHz), Bluetooth (2.4 GHz) and LTE (700 MHz – 5 GHz) and Wi-Fi (2.4 GHz and 5 GHz). The proposed front-end architecture achieves NF of 8 dB, out-of-band IIP3 of 0 dBm and in-band IIP3 of – 5 dBm across the tested frequencies in 65 nm CMOS technology. The design occupies 0.45 mm2.

1. Introduction

Conventional receivers employ narrow band selective filter with off-chip components such as Surface Acoustic Wave (SAW) filter and LC passive matching network made of off-chip inductors and capacitors [1, 2]. These components are inherently hard to tune. Eliminating band selection filters imposes stringent linearity requirements on the receiver front-end. Different solutions for receiving widely spaced bands were proposed in literature. A multi-path narrow-band front-end architecture is a classical choice where one path is powered at a time [3, 4]. This design consumes large area on-chip and off-chip and has high power consumption. Wide-band receivers using wide-band Low Noise Amplifiers (LNAs) alleviate the power penalty incurred [5–7]. This approach offers moderate linearity and poor impedance matching. Transferring the signal sampling and analog-to-digital interface from the baseband to RF side enables further signal processing to take place in the digital domain. Nevertheless, it imposes high speed and resolution requirements on the ADC. A step towards RF-to-digital converter is shown in [8]. The discretization and digitization occur at the RF side. Connecting the antenna directly to a passive mixer while delegating more amplification to the base-band side, aka mixer-first architecture is advantageous [9, 10]. Such a configuration provides considerable benefits, such as wide tuning range and high out-of-band linearity. However, it has poor in-band linearity and consumes high power. Sampling receivers [11–15] are also considered as a viable solution for software defined applications

The proposed architecture is composed of two parallel paths. A tunable band-pass charge sampling filter forms the signal path and a time-varying matching network based on impedance translation is in the parallel path. The receiver’s driving clocks and biasing current are determined based on the targeted frequency. This paper is organized as follows; Section 2 introduces the proposed architecture, discusses the charge sampling technique and the time-varying matching network. Section 3 investigates the circuit implementation of the design. Section 4 presents the required specifications of a multi-band multi-standard receiver, and the results including pre-layout simulations across process corners with post-layout simulations. Conclusions are drawn finally in Section 5.

2. The proposed architecture

Shown in Fig. 1 is the proposed system block diagram. A tunable time-interleaved quadrature band-pass charge sampling filter forms the signal path. A transconductor \( G_m \) converts the input differential RF voltage into current which is then integrated on the sampling capacitances. The filter’s center frequency is adjusted through its controlling clocks. This sets gain, image rejection, and
performs down-conversion to IF frequency at the targeted frequency. The transconductor’s current is controlled to satisfy the required noise figure and linearity. A time varying matching network in the parallel path offers additional selectivity, hence enhances the receiver’s linearity. Its switches are driven by clocks to control the matching frequency. The analysis of the architecture is discussed in Section 3.

2.1. Charge sampling

Current sampling is gaining more interest than voltage sampling as it offers a lower noise figure (NF) and better anti-aliasing filtering effect. Integration of current in certain time interval \(T_i\) (the integration time) on a sampling capacitance \(C_s\) then sampling the resulting voltage to the output gives a low pass sinc filter response with notches at multiples of \(1/T_i\) [16]. After sampling the resulted voltage to the output, the sampling capacitances are discharged. The transfer function of the resulting low pass sinc filter response is given in (1) [16]. This gives dc voltage gain of \(G_m = \frac{C_m}{C_s}\) where \(G_m\) is the transconductance and \(C_s\) is the sampling capacitance.

For an optimal anti-aliasing filtering effect, filter notches should be placed at multiples of the sampling frequency. This mandates that the sampling time of the sampler should equal the total integration time of all current samples. However, the sampling-to-output and the discharging phase’s durations should be considered in the sampling time in addition to the integration phase. Time-interleaved integrating operation gives a hand to solve this problem. This is done by having the first channel in the integration phase while the second channel in the sampling-to-output and discharging phases and vice versa.

\[
H(f) = |H_{\text{SINC}}(f)| = \frac{C_m}{C_s} \left| \frac{\sin(\pi f T_i)}{\pi f} \right|
\]  

(1) Integrating successive \(N\) current samples on the sampling capacitance in the integration phase and sampling them to the output at the sampling rate \(f_s\) gives additional FIR filtering response with sampling frequency \(F_{\text{SIRC}}\). The output sampled voltage on the capacitance is read out after the accumulation of the \(N\) current samples [16]. The resulting FIR filter response has notches at multiples of \((1/N T_i)\). The FIR filter transfer function shown in (2) [16] is composed of three multiplied terms; the first one represents the DC gain, the second one represents the continuous sinc filter response and the third term represents the discrete FIR filter response. The DC voltage gain is \((N G_m T_i/C_s)\).

\[
H(f) = \frac{C_m}{C_s} \left| 1 - e^{-j 2 \pi f T_i} \right| \sum_{k=0}^{N-1} h_k z^{-K} |z^2 = e^{j \pi f T_i}|
\]

(2) Where \(f\) is the frequency and \(N\) is the number of integrated current samples.

Multiplying the impulse response of the FIR LPF by \(e^{j \pi f T_i}\) translates it to a band-pass FIR filter centered at \(f_c = (1/4 T_i)\) [13], where \(T_i\) is the time between two successive samples. This is implemented by multiplying the integrated samples by successive sequences of \(+1, +j, -1\) and \(-j\). This means multiplying the real channel samples by successive sequences of \(+1, 0, -1\) and 0, whereas the imaginary channel samples are multiplied by \(0, +1, 0\) and \(-1\). The current samples are integrated alternately on the real and imaginary channels sampling capacitances. The negative sign is implemented by cross coupling the positive and negative signal paths with a pair of additional switches. This quadrature band-pass filter down-converts the signal to low IF frequency or to DC and provides good image rejection as it has a notch at the image frequency \(-f_c\) that suppresses the image band. The DC voltage gain of the band-pass filter at \(f_c\) equals \((2 \sqrt{2} G_m N T_i/\pi C_s)\) [16].

In the proposed design, a two-time-interleaved channels quadrature band-pass FIR filter forms the receiver signal path. This filter down-converts the signal to IF frequency, provides good image rejection and sub-samples the signal in order to reduce the sampling frequency of the following ADC to \((1/N T_i)\).

Placing the filter notches at multiples of the sampling frequency provides anti-aliasing filtering effect decreasing the sampling noise and enhancing the overall noise figure.

By adjusting the sample integration time \(T_i\), the band-pass FIR charge sampling filter center frequency \((f_c = 1/4 T_i)\) is maintained at the desired Local oscillator frequency. The number of integrated samples determines the position of the filter’s notches and the bandwidth of the signal pass band. It also affects the sample’s gain and consequently impacts the receiver’s noise figure and linearity. It is chosen to be 8 based on a tradeoff between the receiver’s noise figure and linearity.

Fig. 2 shows the time interleaved quadrature band-pass FIR filter. The clocks controlling the two channels for 2 GHz frequency are shown in Fig. 3, where \(T_i\) is 125 ps and number of integrated samples \((N)\) is 8. At each channel, 8 current samples of successive sequences of \(+1, +j, -1\) and \(-j\) are integrated on the sampling capacitances to the output.

2.2. Time varying matching network

In conventional receivers, a passive network of inductors and capacitors is used for impedance matching; however, these components are inherently narrow band. The matching network is hence required tune over the entire frequency range. High frequency passive networks are hard to tune, a programmable
matching network based on impedance translation technique is
used in the proposed architecture.

The proposed time-varying matching network is based on implementing the matching impedance in the base-band side and translating its impedance to the RF side [10]. It is composed of four bi-directional passive switches controlled by 25% duty-cycle non-overlapping clocks followed by parallel combination of resistance and capacitance. Low pass filter (LPF) effect of the resistance with the capacitance in the base-band side is translated to band-pass filter centered at the LO frequency in the RF side providing more selectivity, hence enhancing the receiver’s out-of-band linearity.

The impedance seen by the antenna is shown in Fig. 4 where \( R_b \) is the base-band resistance, \( \gamma \) is scaling factor counting for the impedance translation effect and \( R_{sh} \) is the resistance counting for the harmonic re-radiation losses. These losses arise due to the remixing of the base-band signal with the LO odd harmonics and then re-radiating to the antenna side due to the bidirectional nature of the switches. As the radiations increase, the shunt resistance value decreases and its effect becomes more severe. The usage of quadrature clocks eliminates the image of each harmonic. In order to make the matching controlled by the base-band resistance (\( R_b \)) value, \( R_{sh} \) should be much larger than \( R_b \) and the switch resistance \( R_{sw} \) should be much smaller than \( R_b \). This can be achieved by designing the matching network switches with high \((W/L)\) transistor ratio.

The final matching network is shown in Fig. 5 [17,18]. The base-band resistance is implemented by a resistance wrapped around an amplifier in order to decrease its noise contribution. This configuration matches the real part of the antenna impedance. The cross-coupled feedback resistance between the in-phase and quadrature-phase channels is counting for the matching of the imaginary part of the impedance. The imaginary part is due to the base-band capacitance and the parasitics of the pads and the bond wires at the antenna side resulting in a shift of the matching
frequency from its desired value. The sizes of the switches, the base-band resistances and the amplifier gain are chosen as a trade-off between the matching (S11), linearity and the noise figure (NF).

By adjusting the LO frequency of the matching network controlling clocks, the tunable matching and selective BPF is set at the desired LO frequency.

In reality the impedance seen by the antenna is a parallel combination of the transconductor's input impedance and the translated matching network impedance. In order to have the matching and the translated band-pass filter effect controlled by the matching network, the transconductor should be designed with high input impedance.

3. Circuit implementation

3.1. Transconductor and switches

The transconductor is required to have low noise and high linearity. It should additionally have high output resistance and low output capacitance in order to allow the current to pass in the integrating switches. A folded cascode transconductor shown in Fig. 6 with current sensing common mode feedback (CMFB) circuit is chosen for its high linearity and high output impedance.

The transconductor's output impedance affects the amount of integrated current and consequently the receiver's gain and overall linearity. The transconductor input impedance should be high so that the matching and translated bandpass filter are controlled by the matching network alone.

The transconductor is required to have high linearity, and high input and output impedances at all frequencies. Since the transconductor's input and output impedances vary with frequency, its current is made programmable.

The transconductor's power consumption ranges from 9 mW to 11 mW across the tested frequencies.

The P1dB (1 dB compression point) and IIP3 (third order intercept point), IIP3 and its power consumption across the frequency range (700 MHz – 5 GHz) are listed in Table 1. The transconductor is designed with low noise at the targeted frequencies from 500 MHz to 5 GHz. That is the reason that its corner frequency is less than 100 MHz as shown in Fig. 7. The input referred noise of the transconductor on the targeted band (500 MHz to 5 GHz) is shown in Fig. 8.

The sampler's switches are implemented using I/O 2.5 V devices for its better linearity and low ON resistance to allow most of the current to pass through the switches. The sizes of the switches are chosen so that they have low ON resistance and at the same time low drain and source capacitance.

The transconductor's output resistance and capacitance (i.e., the transconductor's current and the sizes of the devices at the output node), the switch ON resistance and capacitance (i.e. sizes of the switch) and the sampling capacitance are chosen so that the ac current passing in the switches integrated on the sampling capacitance is sufficient enough to achieve the desired gain at the frequency range from 500 MHz to 5 GHz. The desired gain is limited by the required noise figure and linearity specifications.

3.2. Digital circuitry generating charge sampler's controlling clocks

The circuit block diagram shown in Fig. 9. The divider is implemented using two consecutive differential flip-flops, one is controlled by clk and the other is controlled by clk_bar. The output of the second one is fed back to the input of the first flip-flop. The first divider is controlled by clk and clk_bar and generates four 90°-phase-shifted 50% duty-cycle clocks (Q1, Q1_bar, Q2 and Q2_bar) of half the clk frequency. The divider schematic is shown in Fig. 10.
The in-phase clocks (Q1 & Q1_bar) are ANDed with clk_bar and the quadrature-phase clocks (Q2 & Q2_bar) are ANDed with clk resulting in four 90° phase shifted 50% duty cycle clocks (out1, out2, out3 & out4). Q1 & Q1_bar are the controlling clocks of the successive differential divider generating four 90° phase shifted 50% duty-cycle clocks (Q3, Q3_bar, Q4 and Q4_bar) of half the controlling clock Q1 frequency. The quadrature clocks (Q4 & Q4_bar) are the controlling clocks of the following divider generating four 90° phase shifted 50% duty-cycle clocks (Q7, Q7_bar, Q8 and Q8_bar) of half the controlling clock Q4 frequency. The frequency of the clocks Q8 and Q8_bar is equal to the sampling frequency. By ANDing each one of them with each clock of (out1, out2, out3 & out4), the required integration pulses of the first channel (imagn, realn, imapp and realp) and that of the second channel (imagn_interleaved_realn_interleaved, imapp_interleaved_realp_interleaved) shown in Fig. 9 are obtained.

For the first channel; the sampling-to-output clock is generated by ANDing the clock realn_interleaved with Q3, whereas the discharging clock is generated by ANDing realn_interleaved with Q3_bar. For the second channel; the sampling-to-output clock is generated by ANDing realn with Q3 whereas, the discharging clock is generated by ANDing realn with Q3_bar.

Each stage is loaded by the capacitance of the next stage, so buffers of minimum sized cascaded inverters are inserted between two successive stages.

3.3. Digital circuitry generating matching network controlling clocks

The matching network needs four non-overlapping 25% duty cycle clocks with LO frequency. The circuit includes a divider with two successive differential flip flops, one controlled by clk_MN and the other is controlled by clk_bar_MN. The output of the second one is fed back to the input of the first flip-flop as shown in Fig. 11 to generate four 90° phase-shifted 50% duty-cycle clocks (Q1_MN, Q1_bar_MN, Q2_MN and Q2_bar_MN) of half the clk_MN frequency. The in-phase clocks (Q1_MN& Q1_bar_MN) clocks are ANDed with the controlling clk_bar_MN and the quadrature clock cycles (Q2_MN & Q2_bar_MN) are ANDed with the controlling clk_MN and the quadrature clock cycles (Q2_MN & Q2_bar_MN) are ANDed with clk_MN resulting in four 90° phase-shifted 25% duty cycle clocks (out1_MN, out2_MN, out3_MN & out4_MN).
The block diagram of the digital circuit is shown in Fig. 11.

4. Analysis and results of the proposed architecture

In this section the required specifications for multi-standard receiver are shown and proposed architecture is analyzed considering its noise, linearity and power matching.

4.1. Specifications

The design is targeting multi-standard/multi-band applications which mandates the satisfaction of the specifications of GSM (2G), UMTS (3G), Bluetooth, LTE and Wi-Fi. Table 2 shows the specifications of each standard with the required specifications of the receiver supporting all covered standards and the achieved results.

The design can be adaptive by saving power when targeting standards with relatively relaxed linearity specifications such as GSM and UMTS and pumping more power for standards with stringent specifications.

Ref. [19] targets 500 MHz, 1 GHz and 2 GHz as a test case to prove the programmability concept. However, the architecture is tested to satisfy different frequency standards.

4.2. Gain

The gain of the proposed receiver front-end is controlled by the charge sampler’s gain. It depends on the $G_m$ of the transconductor, the sampling capacitance ($C_s$), the number of the integrated samples ($N$) and the integration time ($T_i$).

The charge sampler’s gain needed is based on a tradeoff between its linearity and noise figure. The charge sampler’s linearity is enhanced as its gain decreases which means that decreasing its output swing, while its noise figure decreases as its gain increases.

The receiver’s gain ranges from 13 to 15 dB across the tested frequencies as shown in Table 3. The minimum gain of 13 dB occurs at 5 GHz and maximum gain of 15 dB occurs at 700 MHz as shown in Fig. 12.

4.3. Noise analysis

The noise of the system is defined by its noise figure. We are interested in the thermal noise region as the targeted IF frequency is 10 MHz. The noise of the band-pass FIR charge sampling filter is added to the time varying matching network noise. The total noise figure is 8/8.5 dB at 10 MHz for all frequencies as shown in Table 4. The highest noise figure is 8.5 dB at 10 MHz occurs at 700 MHz and 850 MHz as shown in Fig. 13. The charge sampler has noise of (5–6.3) dB across the targeted frequencies and the matching network adds (2–3) dB. The receiver’s total noise figure with the contribution of each block across the targeted frequencies are shown in Fig. 14.

### Table 2

<table>
<thead>
<tr>
<th>Standard</th>
<th>NF (dB)</th>
<th>Out-of-band IIP3 (dBm)</th>
<th>Out-of-band P1dB (dBm)</th>
<th>In-band IIP3 (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM (850 M, 900 M, 1.8 G and 1.9 G Hz)</td>
<td>9</td>
<td>–19</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>UMTS (850 M, 1.8 G, 1.9 G and 2.1 G Hz)</td>
<td>8</td>
<td>–13</td>
<td>–26</td>
<td>–</td>
</tr>
<tr>
<td>Bluetooth (2.4 GHz)</td>
<td>8</td>
<td>–19</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>LTE (700 M – 3.6 GHz)</td>
<td>9</td>
<td>–10</td>
<td>–</td>
<td>–21</td>
</tr>
<tr>
<td>WiFi (2.4 and 5 GHz)</td>
<td>8</td>
<td>–10</td>
<td>–20</td>
<td>–21</td>
</tr>
</tbody>
</table>

### Table 3

PAC gain for all frequencies.

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7</td>
<td>15</td>
</tr>
<tr>
<td>0.85</td>
<td>14.8</td>
</tr>
<tr>
<td>0.9</td>
<td>14.4</td>
</tr>
<tr>
<td>1.8</td>
<td>13.8</td>
</tr>
<tr>
<td>2.4</td>
<td>15</td>
</tr>
<tr>
<td>3.6</td>
<td>14.3</td>
</tr>
<tr>
<td>0.5</td>
<td>13</td>
</tr>
</tbody>
</table>

### Table 4

Total noise figure at all frequencies.

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>NF (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>700</td>
<td>8.5</td>
</tr>
<tr>
<td>850</td>
<td>8.5</td>
</tr>
<tr>
<td>900</td>
<td>8.1</td>
</tr>
<tr>
<td>1800</td>
<td>8.4</td>
</tr>
<tr>
<td>2400</td>
<td>8.4</td>
</tr>
<tr>
<td>3600</td>
<td>8.1</td>
</tr>
<tr>
<td>5000</td>
<td>8.4</td>
</tr>
</tbody>
</table>
in-band and out-of-band linearity. Out-of-band linearity is when the blockers exist away from the signal band and in-band linearity is when the blockers exist within the signal band.

The quadrature band-pass FIR charge sampling filter provides good in-band and out-of-band linearity. The out-of-band linearity is much more enhanced through the matching network selectivity. The receiver achieves out-of-band IIP3 of $-0.8 - 0.426$ dBm, in-band IIP3 of $-4 - 6$ dBm, out-of-band P1dB of $-8 - 11$ dBm and in-band P1dB of $-13 - 14.5$ dBm as shown in Table 5. The worst out-of-band IIP3 of $-0.8$ dBm occurs at 2.4 GHz band for two input frequencies of 2.2 GHz and 2.22 GHz as shown in Fig. 15 and the worst in-band IIP3 is of $-6$ dBm occurring also at 2.4 GHz band for two input frequencies of 2.401 GHz and 2.403 GHz as shown in Fig. 15.

The charge sampler’s achieves in-band IIP3 of $-5 - 7$ dBm and out-of-band IIP3 of $-4 - 6$ as shown in Fig. 16.

The capacitance in the matching network affects the receiver’s linearity. As the capacitance increases, the receiver achieves better linearity.

4.5. Matching

The matching network parameters are chosen based on a trade-off between power matching and noise figure. $R_b = 800 \Omega$, $R_0 = 90 \Omega$ and $\text{cap} = 3$ pF. Matching is indicated by S11. S11 for all frequencies is shown in Fig. 17. Indicating a good matching $< -10$ dB at all of them.

4.6. Corner analysis

The design is implemented using a 65 nm CMOS process kit. This kit has different corner analysis. In addition to the well-known process corners fast-fast (ff), slow-slow (ss), fast-slow (fs) and slow-fast (sf), there is a third letter which can be g, p or f. The letter g stands for global process variations determined by random distributions. The letter p stands for passive mismatch determined by random distributions with a unique set of values for each instance of the model. The letter f stands for FET doping and geometric mismatch effects determined by random distributions with a unique set of values for each instance of the model. The design is tested across process corners at all frequencies achieving highest NF of 9.7 dB at ssf corner and worst in-band IIP3 of $-10$ dBm and out-of-band IIP3 of $-7$ dBm at ssf corner. It is obvious that (f) is the most effective condition as the design is differential.

4.7. Layout

The layout of the whole architecture is shown in Fig. 18, it occupies area of 0.45 mm$^2$ (870 $\mu$m $\times$ 540 $\mu$m).

For the transconductor, the design is differential so matching is very important. That is why large width transistors are divided to many fingers and they are inter-digitated. The area of the transconductor is (116 $\mu$m $\times$ 45 $\mu$m).

The area of the integration, sampling-to-output, discharging switches and the sampling capacitances is (307 $\mu$m $\times$ 75 $\mu$m). The sampling capacitance using MIM caps occupies most of the area.

The sizes of the matching network switches increase after layout as the effective base band resistance after layout increases due to the effect of the parasitic resistance. Consequently the width of the transistors increases to reduce the switch resistance to compensate for this effect. The area of the matching network is (715 $\mu$m $\times$ 217 $\mu$m).

The achieved pre-layout and post-layout results are compared with other existing architectures in Table 6. This work provides programmable front-end that can support multi-frequencies. However, designs [11,20] based on sampling receivers are targeting single frequency. In addition, this work has better linearity due to further selectivity of the time varying matching network. Also it has better matching and lower power consumption. Wide-band receiver [21] using wide-band LNA also has worse linearity and poor matching when compared to this work.

### Table 5

Out-of-band and in-band IIP3 and P1dB of all frequencies.

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>700</th>
<th>850</th>
<th>900</th>
<th>1800</th>
<th>2400</th>
<th>3600</th>
<th>5000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Out-band IIP3 (dBm)</td>
<td>$-0.135$</td>
<td>$-0.64$</td>
<td>$-0.7$</td>
<td>$-0.066$</td>
<td>$-0.8$</td>
<td>$-0.083$</td>
<td>$0.426$</td>
</tr>
<tr>
<td>In-band IIP3 (dBm)</td>
<td>$-10.4$</td>
<td>$-9.2$</td>
<td>$-10.1$</td>
<td>$-8.1$</td>
<td>$-10.2$</td>
<td>$-11.2$</td>
<td>$-10$</td>
</tr>
<tr>
<td>Out-band P1dB (dBm)</td>
<td>$-13.2$</td>
<td>$-13.2$</td>
<td>$-12.8$</td>
<td>$-14$</td>
<td>$-14.2$</td>
<td>$-14$</td>
<td>$-1$</td>
</tr>
<tr>
<td>In-band P1dB (dBm)</td>
<td>$-13.2$</td>
<td>$-13.2$</td>
<td>$-12.8$</td>
<td>$-14$</td>
<td>$-14.2$</td>
<td>$-14$</td>
<td>$-1$</td>
</tr>
</tbody>
</table>
5. Conclusion

The aim of this work is to implement a programmable receiver front end controlled by adjusting the driving clocks of the receiver's blocks to be able to receive different frequency bands. By controlling the clocks of the charge sampler (the integration pulse width) and the clocks of the time varying matching network, the receiver is able to receive a certain frequency band. This receiver alleviates the moderate linearity and poor matching in sampling receivers and wide-band receivers. The receiver achieves better linearity than the other wide-band designs. In this design; the receiver's linearity is controlled by the transconductor and is more enhanced by the time varying matching network selectivity.

Fig. 15. Worst out-of-band and in-band IIP3.

Fig. 16. Out-of-band and in-band IIP3 of the charge sampler.

Fig. 17. S11 at 2 GHz, 1 GHz and 500 MHz.

Fig. 18. The design layout.
design has better matching than other designs. Matching is based on a programmable matching network instead of a wide-band one. Good matching can be held at multi-bands. This design can receive any frequency band of any standard. By adjusting the controlling clocks, the band pass filter response and the matching are held at the desired frequency. By adjusting the number of integrated samples (N) and the sampling capacitance (C), the receiver’s gain is controlled, consequently the receiver’s noise and linearity are controlled. Adjusting the resistances and capacitances values in the matching network controls matching, noise and linearity due to its further selectivity.

Table 6: Performance metrics comparison with existing designs.

<table>
<thead>
<tr>
<th>Design</th>
<th>Schematic results</th>
<th>Post layout results</th>
<th>[7]</th>
<th>[14]</th>
<th>[15]</th>
<th>LTE specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS technology</td>
<td>65 nm</td>
<td>65 nm</td>
<td>65 nm</td>
<td>65 nm</td>
<td>180 nm</td>
<td></td>
</tr>
<tr>
<td>Frequency (Hz)</td>
<td>0.7 – 5</td>
<td>0.7 – 5</td>
<td>1</td>
<td>0.5-3</td>
<td>2.3</td>
<td>0.7–2.7</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>13 – 15</td>
<td>–</td>
<td>20.2</td>
<td>35</td>
<td>30</td>
<td>–</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>8 – 8.5</td>
<td>8 – 8.5</td>
<td>7.5</td>
<td>4.5</td>
<td>6</td>
<td>9</td>
</tr>
<tr>
<td>Out-of-band IP1dB (dBm)</td>
<td>–10 – 12</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Out-of-band IP3 (dBm)</td>
<td>–4 – 6</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>In-band IP1dB (dBm)</td>
<td>–16 – 17</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>In-band IP3 (dBm)</td>
<td>–6 – 8</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>S11 (dB)</td>
<td>–9 – 11.5</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>9 – 11</td>
<td>10 – 12 (Analog) + 4 (Digital)</td>
<td>18.2 (A) + 16.8 (D)</td>
<td>28</td>
<td>26.7</td>
<td>40</td>
</tr>
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References