Micro-scale variation-tolerant exponential tracking energy harvesting system for wireless sensor networks

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Abstract

Self-powered stand-alone electronic systems, targeting low power applications, are the future of power management. In wireless sensor networks (WSNs) and implantable devices, battery replacement is expensive and power management of these systems is essential. Energy harvesting is considered one of the main power management methods that scavenge energy from the ambient resources that are available and abundant. They take the advantage of minimizing the maintenance costs as well as saving area (Penella-Lopez and Gasulla-Forner, 2011). This paper presents a new tracking technique for maximum power harvesting of solar energy using a micro-scale photovoltaic cell. The new design is based on the analytical derivation of the system equations. The power converter used is a tree topology charge pump, the control circuit is a low frequency voltage controlled oscillator (VCO), and the energy storage element is an output super-capacitor. The system is designed using TSMC 65 nm technology node. Typical power efficiency of the proposed circuit reaches 63% where the proposed design is targeting indoors and outdoors light intensities at zero load condition. The maximum power consumption of the harvester reaches 170 μW.

1. Introduction

Energy harvesting is a technique used to collect energy from ambient sources. This operation is carried out by means of transducers to transfer the ambient power into electrical power. This power is then managed through power regulating circuits to be suitable for supplying different loads. This process is also called “energy scavenging”. Actually, the idea is old and suits a lot of common applications. For example, it can be used in solar photovoltaic (PV) panels to supply electricity to houses and also in wind turbines, which are considered large-scale systems. In this work, design challenges for powering micro-scale systems, denoted by stand-alone electronic systems, are discussed. The most important application of power harvesters is wireless sensor networks (WSNs). In WSNs, it is very expensive to make the battery replacement frequently and it becomes impossible when the number of WSNs nodes is large. Therefore, integrated harvesters can save time and money for powering WSNs. Other stand-alone applications are traffic, medical and environmental applications, navigation, and system controls of buildings.

Solar energy has the highest energy density among the available ambient resources. Table 1 shows a comparison between different ambient energy sources. Solar energy harvesting includes many design challenges especially for the micro-scale systems. First, the size of these tiny systems limits the area of the energy harvester. Thus, the PV cell area should be small. The terminal open circuit voltage of the solar cell (VOC) is in the order of 0.75 V. This small voltage cannot directly power an electronic system, especially if there are RF data transceivers that are considered as power hungry modules. Therefore, a voltage multiplier should be added to increase the voltage to a higher value, and this voltage multiplier contains many design issues. Second, the control unit design is critical in terms of power consumption and its tracking approach. Hence, there is a technique called maximum power point tracking (MPPT), used to lock the PV cell at the maximum power that corresponds to a certain light intensity. This technique guarantees the delivery of the highest possible power to the load. However, the power overhead of this MPPT control circuit should be minimized.

This paper proposes a new circuit technique that has several advantages over the design presented in [3]. The design of the proposed harvester is based on the maximum power locking mechanism that makes use of the exponential relationship between the charge pump frequency and the PV terminal voltage, as discussed in Section 3. The advantages of the proposed design in this paper include (1) the PV cell output power reaches up to 3 mW due to the locking mechanism, whereas the work in [3] produces a maximum PV cell output power up to 0.5 mW, which makes it suitable only for

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indoor applications. Hence, the proposed design has wider locking range that is suitable for indoor and outdoor applications. (2) The power overhead of the tracking system is smaller as extra circuitry for current sensing and decision generation circuits are not needed, it is a plus also in terms of area.

The paper is organized as follows: Section 2 gives an overview of the system blocks. Section 3 shows the analytical derivation of the new tracking approach and the hardware implementation. The simulation results of the whole system are monitored in Section 4 capturing the main performance metrics with concentration on some optimization techniques. Section 5 presents the impact of process variations on the system. Section 6 draws the conclusion and future work.

2. Microscale energy harvesting system

Efficient design of microscale energy harvesters are discussed in details in [4]. In this section, the system blocks are discussed focusing on the parts used in this work.

2.1. PV photovoltaic cell

The energy transducer of the solar energy based harvesters is the photovoltaic cell. Since a typical WSN requires power in the range of microwatt, a micro-scale PV cell is used as shown in Fig. 1. The amount of extracted power reaches up to 3 mW. The PV cell is used to directly convert the light energy into electrical energy through photovoltaic effect and is modelled as a voltage limited current source. Fig. 2 shows the power profile versus the PV voltage at different light intensities. The amount of power extracted from the PV cell varies with the output impedance value ($Z_{ph}$) [5]. For a constant light intensity, there is a corresponding optimum PV voltage that gives the maximum power at this light intensity value. The dotted line represents the locus of the maximum power curve across different light irradiances. The PV model used in the simulations of this study is a compact verilog-A model that is given in [6].

2.2. Power converters

Power converters are used in the energy harvesters in order to increase the voltage to a suitable value that is able to drive different loads. There are two types of converters. The first one is the DC–DC buck-boost converter that is used to increase or decrease the input voltage. The main drawback of using these converters is the bulky off-chip inductor. This introduces huge electromagnetic interference (EMI) noise as well as occupies large area, that is not suitable for low cost integration due to the die area constraints. The second power converter type is the charge pump power converters, which uses on-chip capacitors and transistors that makes them the perfect match for low cost integration.

ChARGE pumps have different design metrics such as power conversion efficiency, output ramp up time, and output ripples. The most important metric is the charge sharing capability (the ability of the charge pump to do a complete charge sharing), which is characterized by the knee frequency (the frequency at which the output current of the charge pump reaches $(1/\sqrt{2})$ of the maximum possible current value) of the architecture used [7]. The first published converter is the Dickson charge pump [8], which exhibits a linear characteristics. Linear topologies performance degrades in terms of charge sharing for low input voltage values which is the case for micro-scale harvesters. Several topologies are proposed recently and the most effective architecture proposed is the tree topology [7]. It increases the capability of the charge sharing by decreasing the worst charging time constant, and correspondingly, increases the knee frequency.

Fig. 3 shows a two stages tree charge pump that is used in the proposed design in this work. The number of stages is determined by the input voltage and the output voltage levels. Here, the output voltage is four times the input voltage according to Eq. (1). The charge pump output current depends on the flying capacitance values ($C_1$), frequency of Clk1, Clk2, and the difference between the input voltage and the output voltage [7]. The flying capacitance is chosen to be 500 pF in order to decrease the operating frequency range:

$$V_{out} = (N + 1)V_{ph}$$

(1)
where \( N \) is the number of charge pump stages used, here three stages is used to reach an output voltage of 1.8 V.

### 2.3. Control unit

The control unit used in the harvester has distinct approaches and metrics such as the tracking algorithm, the frequency range, the power consumption, and the voltage tracking efficiency. Efficient design of the control unit means tracking the voltage of the maximum power with the smallest area overhead and the minimum possible power overhead. These challenges dictate low frequency range operation and impact directly on the overall power efficiency.

A typical energy harvester is discussed in [9]. The design is mainly based on increasing the output current of the charge pump by placing a current sensor at the charge pump output to sample the current. Then, a decision generation circuit is used to find the next step whether to increase the VCO frequency or decrease it. This architecture is good in terms of the PV voltage tracking efficiency. However, it consumes high power and exhibits large area overhead.

Another technique used for MPPT tracking is proposed in [3]. The approach is based on investigating the system design equations and finding a compact relationship between photovoltaic terminal voltage and the target operating frequency, required for maximum power transfer. Fig. 4 shows the closed loop operation of this MPPT technique. Each light intensity has a frequency range that sweeps the entire voltage range. Among these frequencies, there is only one frequency that corresponds to the maximum power point. The dotted line shows the locus of the optimum operating point across different light intensities. Therefore, the relationship that verifies this locus was implemented using circuit design changes for the basic VCO. This technique reduces the power and area overheads compared to that in [9]. However, it suffers from limited dynamic voltage range because it attempted to approximate the exponential relationship with a quadratic equation, using pinch-off saturated transistors. In the proposed work, the exponential relationship is modeled by using sub-threshold operating transistors which allows higher dynamic voltage range than that in [3] as well as higher tracking efficiency.

In order to have a deeper understanding of the system locking dynamics, Fig. 5 shows the transition between two different light samples (i.e., light 1 to light 3). When the input light intensity is changed instantaneously, the PV terminal voltage is changed at the operating frequency. The control unit responds to this change by varying the frequency of the charge pump, accordingly the PV terminal voltage is maintained to the charge pump interface perturbation. This process is repeated, until the whole system stabilizes at the intersecting point between the operating light curve and the control unit trajectory. The closed system is considered as a solution finder for these two intersecting curves.

### 2.4. Energy buffer

The output converted power of the charge pump is then stored in a huge reservoir. It can be a super-capacitor or a rechargeable battery. A super-capacitor is an electrochemical capacitor that has high energy density. It takes values in the range of tens of micro-farads and gains the advantage of high resistance to rate-capacity and aging problems. Whereas rechargeable battery suffers a lot from these problems. The main disadvantage of the super-capacitors is that the leakage power is exponentially increasing with the terminal voltage [10]. In this work, a capacitor of 1 \( \mu \)F is used to mimic the output voltage at 2 V.

### 2.5. Wireless sensor node modeling

A typical wireless sensor node can be modeled as load with four different states: transmitting, receiving, idle and off. Most of the time, a WSN is working in the off mode. During a small period of time, it performs data processing, transmission and reception [1]. Accordingly, the average load current that a WSN consumes is relatively small as portrayed in Fig. 6.

The power converter generates power greater than or equal to the average power required by the WSN \( (P_{\text{harvested}} \geq P_{\text{load/average}}) \). The main problem comes in the active mode when huge power is needed instantly to be supplied, since the active mode power is higher than the harvested power by several orders of magnitude. That is why a super-capacitor or a rechargeable battery should be used, in order to save the extra power generated during the idle mode. However, it should be guaranteed that the stored energy in the super capacitor is larger than the difference between the instantaneous load power and the average harvested power \( (E_{\text{stored}} \geq E_{\text{load}} - E_{\text{harvested}}) \).
3. Exponential tracking based microscale energy harvesting

3.1. Analytical derivation

The detailed analysis of the system design is found in [3]. Eq. (2) shows the final relationship between the switching frequency and the PV voltage for maximum power delivery [3]

\[
\frac{I_{\text{sat}}}{N(C(V_{\text{MPP}}/C_0 - V_{\text{EB}})) + \beta} = \frac{1}{A}\left(e^{-q/V_{\text{th}}} - e^{-q/V_{\text{th}} + \alpha}\right)
\]

where \( N \) is the ideal step-up ratio of the charge pump, \( V_{\text{MPP}} \) is the desired PV voltage, \( C \) is the capacitance used in each stage, \( V_{\text{EB}} \) is the energy buffer voltage, \( \alpha \) is the ratio \( (V_{\text{MPP}}/V_{\text{OC}}) \), \( K/q \) is the thermal voltage and equals to 25 mV, and \( A \) is the ideality factor of the solar cell used.

In order to realize this relationship using a VCO, a typical VCO found in Fig. 7 is used to maintain this relationship. Eq.(2) has to be mapped to the VCO equation [3]

\[
f_{\text{clk}} = \frac{I_d}{2V_{\text{max}}C_s}
\]

where \( I_d \) is the charging current of the ring oscillator, \( C_s \) is the ring oscillator input capacitor, and \( V_{\text{max}} \) is the maximum voltage of the capacitor \( C_0 \).

From Fig. 7, the current \( I_d \) is the subtraction of the two currents that are maintained by two transistors in the sub-threshold operation. The control circuit needs careful design in order to verify this relationship. Eq. (2) can be approximated to

\[
f_{\text{clk}} \approx K_1\left(e^{-q(V_{\text{th}} - V_{\text{th}})/nV_{\text{th}}} - e^{-q(V_{\text{th}} + \alpha)/V_{\text{th}}}ight)
\]

where \( K_1 \) and \( K_2 \) are constants, \( V_{\text{MPP}} \) is the locus of the maximum power PV voltage, and \( \alpha \) is the ratio \( (V_{\text{MPP}}/V_{\text{OC}}) \). The transistor operating at sub-threshold region is modeled as [18]

\[
I_d = I_s(e^{q(V_{\text{th}} - V_{\text{th}})/nV_{\text{th}}} - 1)
\]

\[
I_d = I_s e^{-qV_{\text{th}} - nV_{\text{th}}/V_{\text{th}}}
\]

where \( V_{\text{th}} \) is the gate-source voltage, \( V_{\text{th}} \) is the threshold voltage, \( V_{\text{th}} \) is the thermal voltage, and \( I_s \) is the transistor current at \( V_{\text{gs}} = V_{\text{th}} \).

Using Eqs. (3) and (6), the VCO frequency \( f_{\text{clk}} \) of Fig. 7 is given by

\[
f_{\text{clk}} = \frac{I_d\left(e^{q(V_{\text{th}} - V_{\text{th}})/nV_{\text{th}}} - e^{q(V_{\text{th}} + \alpha)/V_{\text{th}}}ight)}{2V_{\text{max}}C_s}
\]

Now, the objective is to approximate Eq. (2) by Eq. (7) by matching the corresponding parameters. By analogy between the two equations, one can deduce the following:

\[
\frac{V_{\text{MPP}}}{V_{\text{EB}}} = \frac{C}{A}
\]

\[
V_{\text{th}} = \alpha(V_{\text{th}} - V_{\text{th}})
\]

\[
V_{\text{eff}} = \alpha V_{\text{th}}
\]

3.2. Proposed circuit design

The implementation of the control circuit displayed in Fig. 7 is divided into two major parts. The left part is the analog section which translates the PV voltage change into a current change through the feedback amplifier (i.e. the Op-Amp). The current mirror is used to replicate the current version to the right side. The

![Fig. 7. Realization of the exponential relationship between the PV voltage and the charge pump switching frequency inside the MPP tracking unit.](image)

![Fig. 8. Typical non-overlap two phase generator [11].](image)

![Fig. 9. DC sweep simulation for the new technique versus the previous technique in [3].](image)

![Fig. 10. Typical two stage common source amplifier with compensation.](image)
right part is the digital section, it is a current controlled ring oscillator. The frequency range is controlled by the delay of the inverter and the frequency tuning is controlled by the charging current of the capacitor \(C_s\). The output \(D\) flip-flop and the inverter are used to produce a 50% duty cycle clock.

The charge pump needs two control clock signals. Since the output of the control unit is only one clock terminal, a non-overlapping phase generator \([11]\) is utilized to generate the two non-overlapping clock signals. This is to prevent the switching leakage. A typical circuit is shown in Fig. 8 where the non-overlapping period is controlled by the delay of the cascaded inverters.

The main advantage of the proposed design over the design presented in \([3]\) is that it approaches the ideal curve of the \(f-V\) relationship required for the maximum power delivery through the realization of the \(f-V\) exponential relationship. Transistors \(M_{(6,7)}\), shown in Fig. 7 are doing this job. They take their gate voltages through a potential divider. The divider is done by a stack of diode-connected transistors \(M_{(1,2,3)}\) as shown in Fig. 7. The stack guarantees a sub-threshold operation for transistors \(M_{(6,7)}\).

Due to the Op-Amp high open loop gain, the voltage \(V_{fb}\) equals the feedback voltage. The current \(I_d\) is then mirrored to the digital side. The right side is a ring oscillator whose frequency is controlled by transistor \(M_8\), the capacitor \(C_s\), and the voltage \(V_{cm}\). Fig. 9 shows a DC sweep for the analog part of the control unit. During the Op-Amp lock range, the feedback voltage is changed linearly. It can be shown that the proposed technique provides an exponential relationship with input voltage \(V_{Ph}\), whereas the design in \([3]\) provides a quadratic relationship with \(V_{Ph}\). 

The flip-flop adopted in the design is the true single phase clock based flip-flop (TSPC) that is based on \([13]\). This topology has several advantages as it exhibits high speed, occupies small area, and consumes low power. The sizing of the pull up network is almost double the size of the pull down network \([14]\). The design of the TSPC flip flop is shown in Fig. 11.

### 3.3. System optimization

The problem of the proposed new technique is the power consumption, since it is needed to generate higher frequency to keep good tracking. This idea contradicts with low power requirements due to the trade-off between power consumption and frequency \([14]\). The tracking circuit has a direct impact on the

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**Fig. 11.** Typical true single phase clock based flip flop.

**Fig. 12.** Capacitive division for lowering the control circuit supply voltage.

**Fig. 13.** Transfer functions of different parameters affecting the whole system.

**Fig. 14.** Typical source follower stage.
power efficiency, as the amount of power you have gained through good tracking is wasted again in the control unit. This subsection is dealing with optimization techniques on the system and block level to find a practical solution for the power efficiency problem.

The control unit is consuming larger power than that in [3]. The most logical solution is to decrease the supply and re-adjust the sizing of the transistors, to get the same correspondence of the frequency–voltage relationship. This update has a great impact on the charge pump capacitance values, as those values should be updated to get the right voltage values at the PV terminal. So basically, when the frequency range is decreased, the capacitance increases to get the same voltage level values. This solution consumes area on the silicon, however higher power efficiency is predictable.

The first optimization is performed on the supply voltage of the control circuit. A capacitive divider is used to lower the supply voltage rather than taking the whole voltage. The output super-capacitor is used to mimic the voltage at 2 V. Therefore, by lowering the supply voltage of the control circuit, it should have a great impact on power consumption and the frequency range. Fig. 12 shows the capacitive division.

The second enhancement was done on the circuit level at the input of the control unit. Since, it is not guaranteed to have the...
exact required PV voltage that corresponds to a certain frequency from the charge pump side; a source follower stage is added before the control unit to ensure a controllable voltage shift at the Op-Amp input. Since \( V_{\text{ph}} - V_{\text{Voc}} \) is controllable, then the frequency that corresponds to a certain \( V_{\text{ph}} \) can be changed. Since a certain trajectory for \( P_{\text{ph}} \) versus \( V_{\text{ph}} \) is desired, Fig. 13 describes the effect of the voltage shift on the maximum power delivery of the whole system. The source follower stage consumes around 1.2% of the total control unit power. By controlling the transistors size and the resistance value as a result, a controllable voltage shift is obtained. Fig. 14 shows a typical source follower.

4. Simulation results

This section views the simulation results for the design replication of [3] versus the simulation results for the proposed new technique. The PV model used is an open source Verilog-A model [6]. Transistors are used from industrial hardware-calibrated TSMC 65 nm technology node. Fig. 15 shows the mathematical relationship between frequency and PV voltage for three different mechanisms. The first curve is the desired relationship, the second one is the relationship of the design in [3] and the third one is the relationship of the proposed design. As shown, the proposed design tracks the desired relation more accurate than that in [3].

After adding all the changes, the most important metrics are monitored to show the robustness of the new technique in comparison with that in [3].

The first simulation is showing the frequency range of each design. Fig. 16 shows the entire frequency range after adding the capacitive division and the source follower stage to the new proposed circuit. It can be seen that the new circuit is operating at much lower frequencies than the design replication of [3]. Nevertheless, decreasing power consumption comes at the expense of increasing the charge pump area. As when the frequency decreases, the input impedance perturbation rate decreases. Accordingly the PV voltage approaches \( V_{\text{Voc}} \), and the system loses locking. In order to make a compensation, the charge pump capacitance has to be increased to decrease the overall input impedance, thus the PV voltage is then decreased.

The second performance metric shown in Fig. 17 is the photovoltaic operating power across different light intensities. It can be shown that the proposed design tracks more efficient than [3]. Efficient tracking provides more power extracted from the solar cell, which has a great impact on power efficiency.

The most important metric in the design of the energy harvesters is the power consumption of the control unit, this metric greatly affects the efficiency. Decreasing the frequency range of operation leads to significant reduction of the dynamic power, therefore, the whole power consumption is decreased. The power consumed in the control circuit is divided into two portions; static power comes from the left side (i.e. analog part), which is responsible for voltage to current conversion and dynamic power comes from the right side (i.e. digital part), which is responsible for current to frequency conversion. Fig. 18 shows the power consumption of the two designs and it is clear that the proposed design operates at much lower power ranges.

Since a new tracking technique is proposed with adding some power optimization solutions, the power efficiency increases. Fig. 19 shows the power efficiency curves of the two designs. The simulation is performed by monitoring the power efficiency at six light samples. It can be shown that the proposed design provides better efficiency across different input light irradiances. It can be concluded also that at each light intensity, the two techniques locks at different PV voltage, which means that the proposed design approach the ideal locking PV voltages. The efficiency is calculated as given in the following equation:

\[
\eta = \frac{V_{\text{Voc}}}{P_{\text{ph}}} \quad \text{(10)}
\]

Fig. 21. Maximum control unit power and system settling time for different control unit supply voltages.

![Table 2](image)

Table 2
Performance metrics comparison table.

<table>
<thead>
<tr>
<th>Specifications</th>
<th>VLSID 2012 [3]</th>
<th>Work (( V_{\text{csv}} = 1.4 ))</th>
<th>Work (( V_{\text{csv}} = 2 ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency range</td>
<td>8.8 MHz → 21.9 MHz</td>
<td>1.84 MHz → 5.54 MHz</td>
<td>1.73 MHz → 6.81 MHz</td>
</tr>
<tr>
<td>PV voltage range</td>
<td>632 mV → 742 mV</td>
<td>638 mV → 717 mV</td>
<td>638 mV → 694 mV</td>
</tr>
<tr>
<td>Max. PV power</td>
<td>424 µW → 2.138 mW</td>
<td>425 µW → 2.3 mW</td>
<td>426 µW → 2.31 mW</td>
</tr>
<tr>
<td>Energy buffer power capability</td>
<td>66.8 µW → 1.08 mW</td>
<td>199 µW → 1.41 mW</td>
<td>14 µW → 1.34 mW</td>
</tr>
<tr>
<td>( \eta )</td>
<td>15.8% → 51%</td>
<td>47.2% → 63.1%</td>
<td>2.3% → 58.1%</td>
</tr>
<tr>
<td>Worst case settling time</td>
<td>0.8 µs</td>
<td>2.3 µs</td>
<td>0.96 µs</td>
</tr>
</tbody>
</table>

Fig. 22. Figure of merit for different control unit supplies.
From the previous simulations, it is evident that the harvester applications for indoors and outdoors light intensities depend on the dynamic range of the input voltage. It is defined by the tracking capability of the harvester itself. The lower limit of the voltage range is defined by the voltage that corresponds to the lowest power possible needed for supplying the control circuitry. At this point, there is no power that can be supplied to the load, so it is considered the lowest extreme point. On the other hand, the upper limit is defined by the voltage at which the tracking is in the worst case possible, so it has the worst power efficiency. The extracted power is very small, and is also the extreme point for supplying the control unit. The highest extreme point can be also considered the highest corresponding light intensity of the environment. In brief, the ceiling of the range is identified by whichever is earlier from the upper limits discussed. The dynamic range here is 79 mV, it is calculated by assuming the highest PV terminal power is around 3 mW.

Since the control unit power is crucial in the design of the energy harvesting modules, different simulations were done to test the reliability of the circuit while decreasing the wasted power. The capacitive voltage divider ratio is changed to deliver three voltage values to the control unit (i.e., 1.4 V, 1.6 V, 1.8 V and 2 V). The output voltage is tied to 2 V. Two important metrics are monitored; settling time of the PV voltage, which is defined as the time needed to change from an initial value to a final value with 99% of the step value. This metric is monitored by injecting a full range light step to the system like the simulation shown in Fig. 20. The second metric is the control unit power, which is the total power consumed by the control unit at the upper limit intensity. Fig. 21 shows the results of the stated simulation, it shows the tradeoff between the speed and the power consumption. It depends on the designer, whether to choose the speed over power consumption or vice versa. Since minimum power consumption is the target, the control unit supply voltage is set to 1.4 V.

Table 2 summarizes the performance metrics comparison between the proposed system design and the design in [3].

Two design versions are proposed. One is targeting high efficiency and low power consumption, the operating control unit supply voltage is 1.4 V. The other design is targeting speed, the operating control unit supply voltage is 2 V. The design replication of [3] is implemented without dividing the output supply, it is taken as it is and fed to the control unit directly. The common specifications of the three versions are output capacitor of 1 μF, open circuit voltage smaller than 0.8 V and initial output voltage of 2 V. It can be shown that the design with 1.4 V control unit supply offers the lowest frequency range thus the highest efficiency, but it has poor speed performance. Whereas, the design with 2 V control unit supply introduces better speed performance than that with the 1.4 V control unit supply. The design in [3] has the best speed performance, since it is not operating in the sub-threshold mode, but it has the worst efficiency. Fig. 22 shows the figure of merit defined by the product of the control unit power times the settling time of the system. If the designer wants to optimize on both parameters, he should select the minimum point on this curve.

5. Effect of process variations

5.1. Simulation results

Since some transistors in the control circuit are operating at the sub-threshold mode, it is important to capture the process corners.
in order to test the functionality. The current equation of the sub-threshold mode includes the threshold voltage at the exponent power as shown in Eq. (5), the value of the current is exponentially dependent on the threshold voltage value. Fig. 23 shows the process corner simulations, the simulation is performed for typical–typical, slow–slow, slow–fast, fast–slow and fast–fast corners. It can be seen that the locking process deviates from the typical curve for a non-typical corner, the frequency range is also affected across corners. The deviation of the curves affects the harvested power as the operating PV voltages are far from the maximum power values. It can be shown also that the frequency–voltage relationship is also varying; it does not take the exponential curvature for a non-typical corner. The frequency range is also affected across corners. The deviation of the curves affects the harvested power as the operating PV voltages are far from the maximum power values.

5.2. System optimization

In order to overcome the problem of process variations, some sort of control has to be added to introduce a compensating effect of the operating corner after fabrication. For example, if the operating corner is the slow–slow corner shown in Fig. 23(a), the P–V curve is shifted to the right side. So it is far away from the required locus. Therefore, the new control mechanism has to pull the curve to the left to coincide with the intended locus curve. On the other hand, if the operating corner is fast–fast corner shown in Fig. 23(a), the P–V curve is shifted downwards. So it is far away from the required locus. Then the new control technique has to push the curve upwards to be able to match the desired locus curve. A new adaptive technique is proposed in [15], the proposed circuit is based on perturbing the bulk voltage of both NMOS and PMOS transistors. When \( V_{th_{-N}} \) (i.e. NMOS threshold voltage) increases, \( V_{bulk_{-N}} \) (i.e. NMOS Bulk voltage) should increase to add an opposite effect to \( V_{th_{-N}} \) and vice versa. The same scenario occurs for the PMOS threshold voltage. Eqs. (11) to (15) [13] show the bulk voltage relationship with threshold voltage variations for both NMOS and PMOS

\[
V_{th} = V_{th_{0}} + \Delta V_{th_{n}}
\]

\[
\Delta V_{th_{n}} = \gamma \left( \sqrt{2\phi_f} - V_{BS} - \sqrt{2\phi_f} \right)
\]

\[
V_{BS} = \frac{2\sqrt{2\phi_f}}{\gamma}(\Delta V_{th_{n}}) - \frac{1}{\gamma^2}(\Delta V_{th_{n}})^2
\]

\[
V_{bn} = \frac{2\sqrt{2\phi_f}}{\gamma_n} (V_{th_{n}} - V_{th_{n0}}) - \frac{1}{\gamma_n^2} (V_{th_{n}} - V_{th_{n0}})^2
\]

\[
V_{bp} = V_{dd} - \frac{2\sqrt{2\phi_f}}{\gamma_p} (V_{th_{p}} - V_{th_{p0}}) + \frac{1}{\gamma_p^2} (V_{th_{p}} - V_{th_{p0}})^2
\]

where \( V_{th_{n}} \) is the threshold voltage under no body bias. \( V_{th_{n}} \) is the threshold voltage under body bias. \( \Delta V_{th_{n}} \) is the voltage increment due to body bias. \( \gamma, \gamma_n, \gamma_p, \phi_f, \phi_{ff}, \phi_{ff_1} \) are technology constants. \( V_{bn} \) is the bulk-source voltage difference. \( \Delta V_{th_{n}} \) is the threshold voltage variation change. \( V_{bn} \) is the NMOS body voltage. \( V_{bp} \) is the PMOS body voltage. \( V_{th_{n}}, V_{th_{p}} \) are the NMOS, PMOS threshold voltages under process variations. \( V_{th_{n0}}, V_{th_{p0}} \) are the NMOS, PMOS threshold voltages under typical conditions.

In [15], circuit designs are proposed to implement Eqs. (14) and (15). One of the most power hungry blocks in the design is the squaring circuit found in [15]. Since power consumption is the most critical metric in the proposed design, the design used in [16] is more convenient. In [16], Eqs. (14) and (15) are linearized through curve fitting. The new equations can be realized easily through the implementation of the summing Op-Amp based circuit shown in Figs. 24 and 25.

Fig. 26 shows the simulation results after adopting the adaptive body bias circuits. It can be concluded that process corners curves start to approach the typical corner curves and this is the goal of adding the adaptive circuits. By this way, the power extracted from the PV cell increases and in return the harvested power at the super-capacitor side also increases. The Op-Amp in each circuit shown in Figs. 24 and 25 is consuming 32 \( \mu W \) power.

6. Conclusion

This paper presents a new technique for maximum power locking of a solar based energy harvester. The system blocks are discussed, the technique is analyzed through system equations. Simulation results show how the new technique efficiently tracks the maximum possible power across different input lights. The design shows its reliability in terms of hardware cost by removing current sensing and decision generation circuits [9,17]. Circuit limitations are discussed. Process corners are highlighted. Some circuit design changes are proposed to overcome the process variations, it can be concluded that the energy harvester needs adaptive body bias technique [15,16]. The power consumption of the adaptive circuits is verified to be low enough, so the power efficiency cannot be affected greatly. Future work can be done at different block levels. The control circuit can operate at much
lower voltages and consume power in the range of nW, nevertheless, it comes at the expense of increasing the charge pump flying capacitances. The output capacitor can be replaced by a rechargeable battery model with management circuit for efficient energy flow regulation.

References