Using Calculator and Expressions for Parameter Analysis and Optimization
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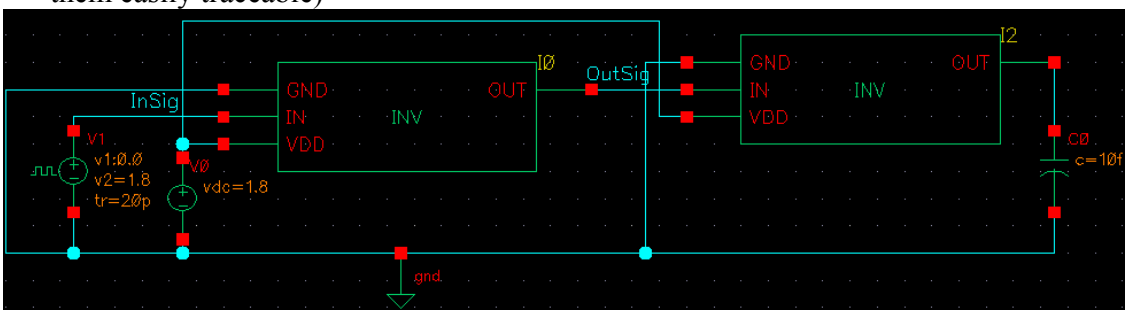
Cadence provides some useful features to do optimization and parametric analysis on circuits. Following, we solve a problem by using calculator and defining expressions.

Problem: Find the (W_P/W_N) ratio of a CMOS inverter which minimizes the propagation delay of the gate.

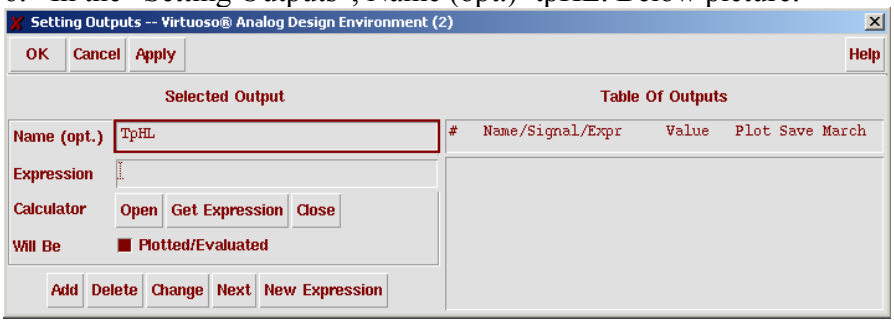
Discussion: It is known that the minimum delay CMOS does not necessarily correspond to symmetric or equal t_{pHL}, t_{pLH} design. Therefore, the objective will be minimizing the (t_{pHL}, t_{pLH})/2 directly.

Assumptions: Output capacitive load = 10 fF V_{DD}=1.8v W_N=600 nm t_r=t_f=20 pS.

Methodologies:
Approach 1) Parametric Analysis:
1. Create a CMOS Inverter.
2. Assign "ratioX600 nm" to the PMOS width. (Note that here "ratio will be the variable which we want to find in order to make delay minimum")
3. Create a chain shape test circuit schematic for the inverter corresponding to the given assumptions as shown below: (Assign names to the input and output wires to make them easily traceable)

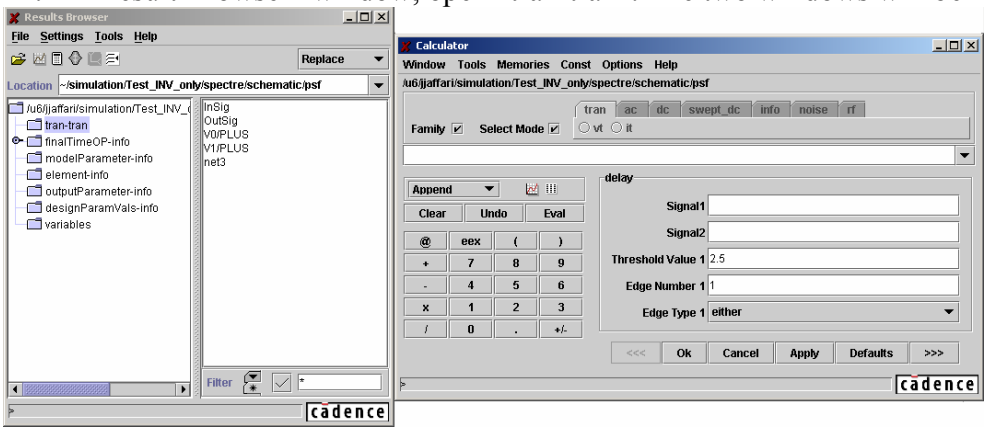


4. In the "Analog Design Environment" perform "model library" and "choose analyses" setting (transient).
5. In the "Analog Design Environment", Outputs->Setup…
6. In the "Setting Outputs", Name (opt.)=tpHL. Below picture:

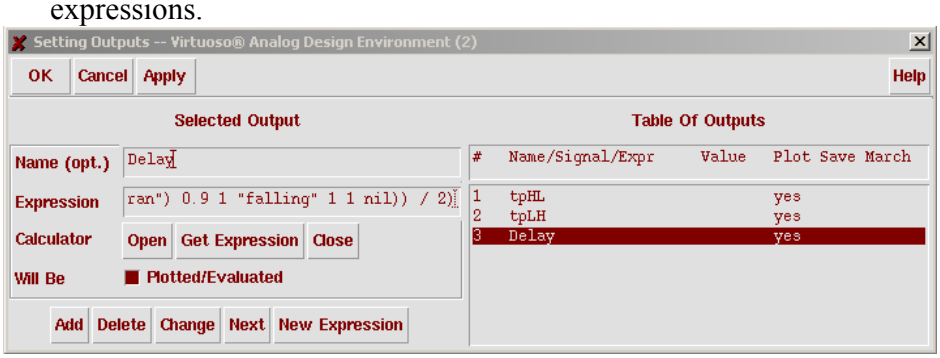


7. Click Calculator "Open". The Calculator window will be opened.
8. In "Calculator" window, Options->Set PRN, to remove the tick.

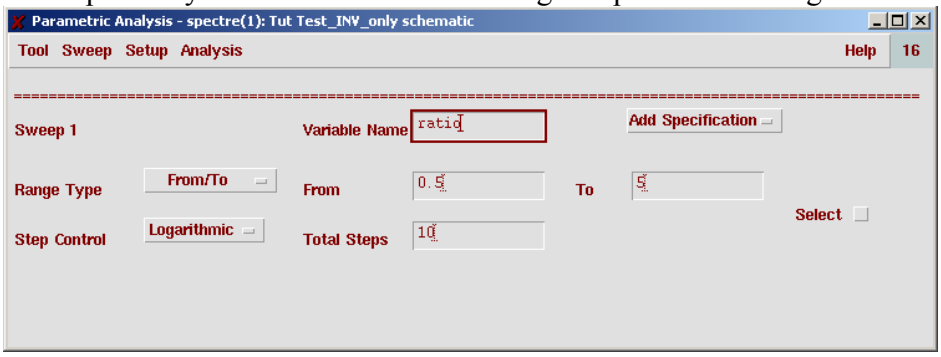
9. In “Calculator” window, Tools->Browser, The result browser will be opened. (Note that you had to ran the simulation one time before to see the signals in the browser)
10. In “Calculator” window, there is a list of functions click “delay”.
11. In “Result Browser” window, open “tran-tran”. The two windows will be like below:



12. Place the cursor in the Signal 1 textbox.
13. Click “InSig” from “Results Browser”.
14. Place the cursor in the Signal 2 textbox.
15. Click “OutSig” from “Results Browser”.
16. Change the Thershold Value 1 to 0.9 which is (V_{DD}/2).
17. Change the Edge Type 1 to “rising”
18. Click >>>
19. Change the Thershold Value 2 to 0.9 which is (V_{DD}/2).
20. Change the Edge Type 2 to “falling”
21. Click >>>
22. Click Apply
23. In the “Setting Outputs” window, Click “Get Expression”, then “Add”. An expression for t_{pHL} has been added.
24. Repeat previous steps this time for tpLH, but assign “falling” to Edge Type 1 and “rising” to Edge Type 2.
25. Now you have two expressions in the “Setting Outputs” window. Like below:
26. Now create an expression namely, “Delay” which is equal to (t_{pLH}+t_{pHL})/2. To do this, we must follow the same way we did for tpHL and tpLH and use “(”, “)”, “+”, and “/” buttons when are needed. (You need to redo steps to define delays from 12 to 22). Following is the picture of the “Setting Outputs” window after adding three expressions.

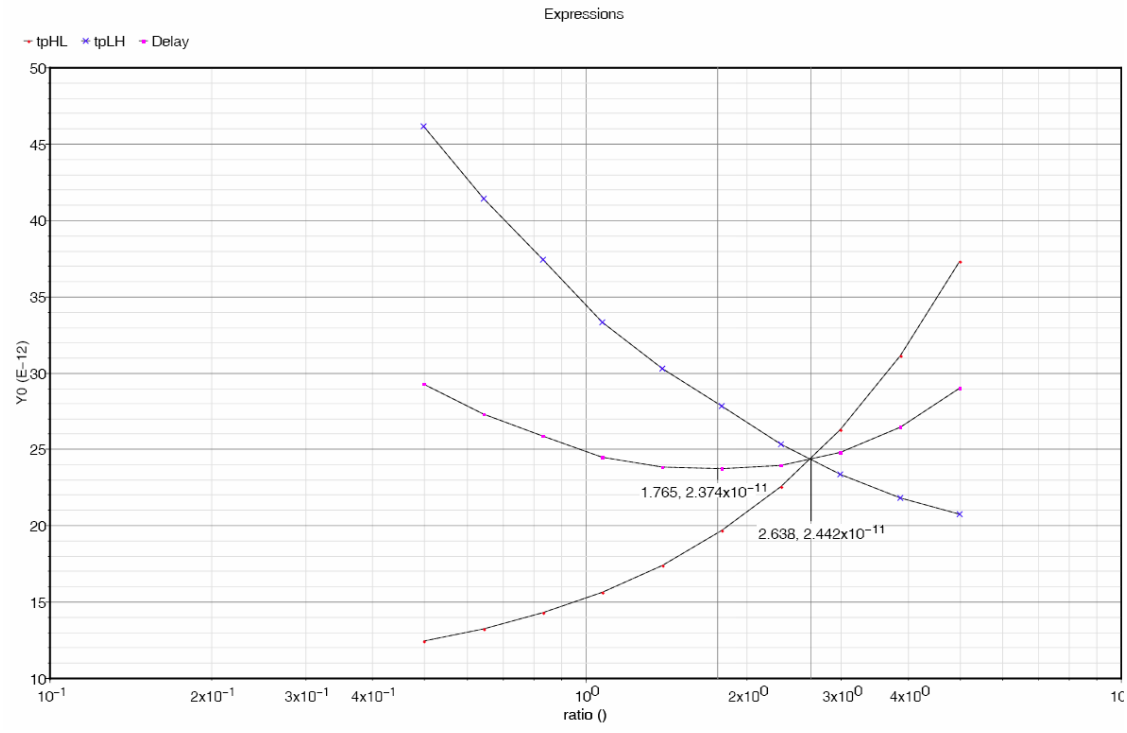


27. Go back to “Analog design Environment” window. You will see that the three expressions are listed.
28. Tools -> Parametric Analysis…, A new window will be opened.
29. In the “Parametric Analysis”, Setup->Peak Name For Variable->Sweep1…
30. Select “ratio”, OK.
31. Fill the “From”, “To”, and “Total Steps” with desired values. Let choose 0.5, 4, 10, respectively. As shown in below. Change Step Control to Logarithmic.



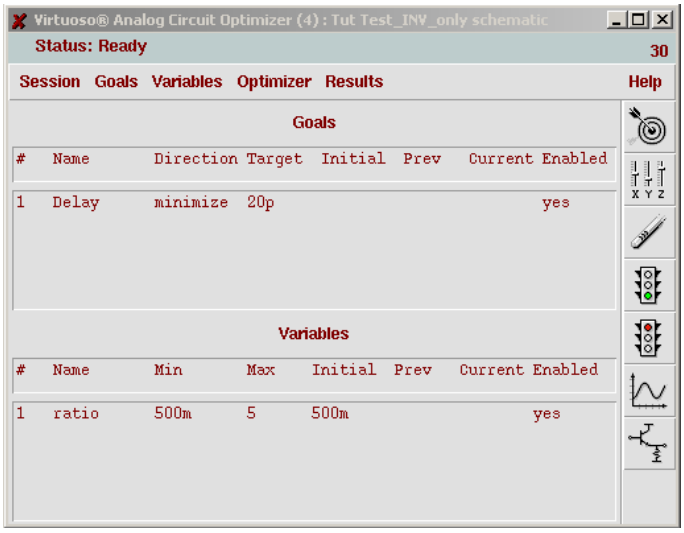
32. Analysis -> Star
33. The output will be the plot of three parameters for different PMOS/NMOS width ratios.

This is the output plot. It can be seen that the minimum delay ratio does not necessarily correspond to the symmetrical point.

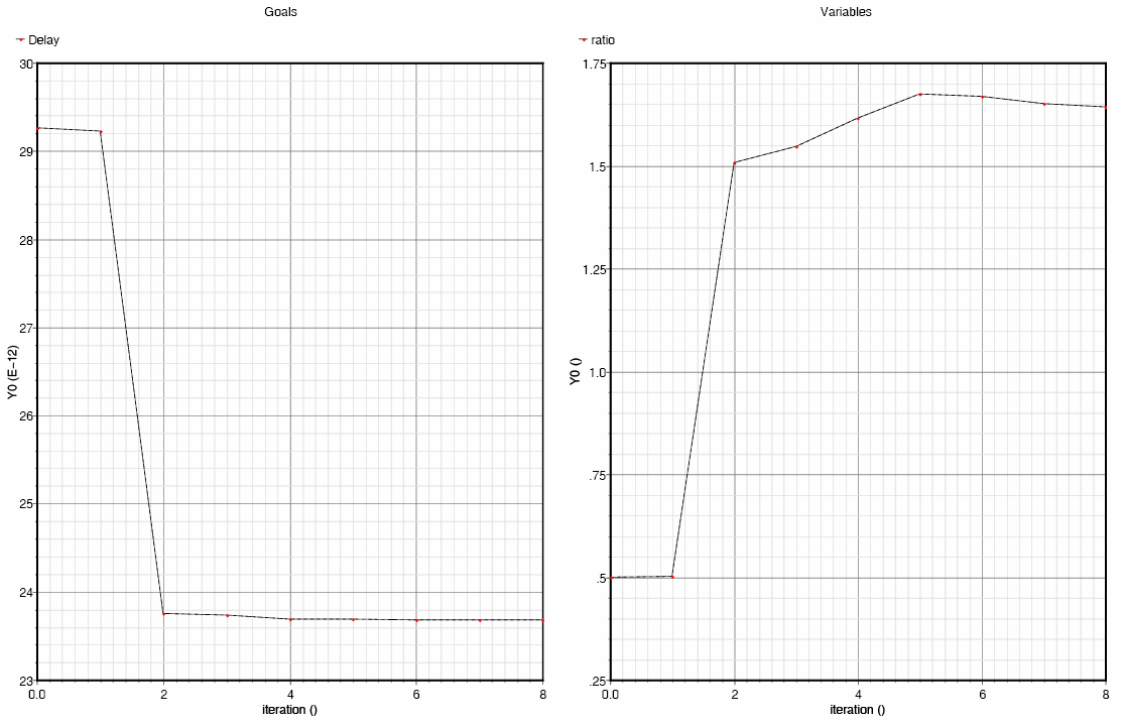


The ratio which gives the minimum delay is 1.765. And the corresponding delay will be 23.74 pSec. However the ratio which t_{pLH}=t_{pHL} is 2.638 for this case.

Approach 2) Optimization:
Follow steps (1)-(27) of the first approach.
28. Tools -> Optimization…, A new window will be opened.
29. In the "Analog Circuit Optimizer" window, Goals->Retrieve Outputs…, Then the three defined expression will be listed.
30. Delete "tpHL" and "tpLH" and just keep "Delay"
31. Double click on "Delay"
32. Choose direction as minimize.
33. Set a target for delay. Let say 20p.
34. Set the acceptable to 23p.
35. Hit OK.
36. In the "Analog Circuit Optimizer" window, Variables->Add/Edit…, Select "ratio". Assign initial value 0.5, minimum 0.5, and maximum 5. The window should become same as below:



37. Optimizer->Run
The output will be a graph of ratio and delay for every iteration. You may stop the optimizer when it doesn't give better result. (You should be aware that due to very nonlinear nature of the simulations, the optimization may converge to some local minima, therefore you may need to change the initial value of skip such local optimums).
Here is the sample output graph for our problem.


Goals
Delay
30
29
28
27
26
25
24
23
Y0 (E-12)
0.0
2
4
6
8
iteration ()
Variables
ratio
1.75
1.5
1.25
1.0
.75
.5
.25
Y0 ()
0.0
2
4
6
8
iteration ()