An Improved Design for High Speed Analog Applications of The Fully Differential Operational Floating Conveyor

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Abstract—This paper presents a novel concept along with a suggested CMOS-based design of the fully differential operational floating conveyor (FD-OFC). The FD-OFC concept and design has been introduced for the first time by the authors [9] as an 8 (4x4) port general purpose analog building block. The differential action offered by the proposed design can be employed in numerous analog and/or hybrid (analog/digital) VLSI applications, particularly where a high noise rejection ratio is desired. Furthermore, the proposed design can operate under biasing conditions as low as 1.2 V (instead of the 1.5 V bias in [9]) at frequencies up to 600 MHz in addition to higher open loop transimpedance gain of 104 dB (compared to 44.5 dB in [9]). These operating conditions recommend the proposed device to be integrated to a wide range of low power-high speed applications. The terminal behavior of the proposed device is mathematically modeled and its operation is simulated using the UMC 130 nm technology kit in Cadence environment.

I. INTRODUCTION

Active analog processing circuits usually rely on various operational amplifier (Op-Amp)-based configurations that operate either in the voltage mode or the current mode. Due to their numerous advantages, the voltage mode analog circuits are usually employed in many analog signal processing applications. However, these devices possess a fixed gain-bandwidth product (GBP) which induces a gain-bandwidth trade-off as required by each particular application. This limitation has been overcome by adopting the current as the active parameter instead of the voltage, a concept which has lead to the development of several current mode-based devices [2] along with their applications. For these and more advantages, the research interests have been directed to the development of such devices as they are perfect candidates for a wide range of analog applications such as biomedical instrumentation and data acquisition devices. The rest of this paper is structured as follows. In Section II, the principle of operation of the OFC is reviewed and its terminal behavior is characterized. Section III introduces the newly developed concept of the FD-OFC, its CMOS-based design and its terminal behavior is introduced based on the OFC model reviewed in Section II. The performance of the proposed FD-OFC is investigated in section IV via simulation results. The whole paper is finally concluded in Section VI.

Notation: Throughout the rest of this paper, boldface symbols and letters denote frequency domain transfer matrices, \([\cdot]^{T}\) denotes the matrix transpose operator and and \(\otimes\) denotes the Kronicker product.

II. OVERVIEW OF CURRENT MODE DEVICES

This section is devoted to review the development of the most common three types of current mode devices along with their principle of operation from a mathematical perspective with the aid of block diagram representation. The input-output (I/O) terminal behaviour of these three devices is modeled in terms of a frequency domain transfer matrix representation.

1) The second generation current conveyor (CCII): Figs. 1 (a) and (b) illustrate typical schematic representation for the non-inverting (CCII+) and the inverting versions (CCII-) of the
second generation current conveyor, respectively. The principle of operation of the CCII+ can be described as follows. The voltage applied at terminal Y exactly appears at terminal X with zero current at terminal Y (i.e., infinite input impedance at terminal Y) and independent voltage and current at terminal X of \( V_x \) and \( I_x \) respectively. The voltage following action at the input ports is accompanied by conveying the current \( I_y \) to the output terminal Z. This mechanism of operation can be represented using the following matrix notation as \([1],[2]\)

\[
\begin{bmatrix}
I_y(\omega) \\
V_x(\omega) \\
I_z(\omega)
\end{bmatrix}
= 
\begin{bmatrix}
0 & 0 & 0 \\
1 & 0 & 0 \\
0 & \pm 1 & 0
\end{bmatrix}
\begin{bmatrix}
V_y(\omega) \\
I_x(\omega) \\
V_z(\omega)
\end{bmatrix}
\]

(1)

where \( \omega = 2\pi f \) is the angular frequency and the + and - signs in (1) correspond to the CCII+ and the CCII-, respectively.

2) Fully differential second generation current conveyor (FDCCII): Fig. 1 (c) depicts a simplified schematic for the inverting and non-inverting versions of the FDCCII (FDCCII+ and FDCCII-) \([3],[4]\). As its name implies, the FDCCII is the differential form of the CCII. The differential action offered by both FDCCII types is achieved by splitting each of the three terminals of the CCII into two terminals, such that the FDCCII has six terminals as shown in Fig. 1 (c).

3) The Operational Floating Conveyor (OFC): The concept of the OFC, which offers more features than both the CCII and FDCCII, has been first introduced \([6]\) based on the BJT technology and re-designed \([7]\) using the more advanced CMOS technology. Fig. 1 (d) illustrates the operation of the OFC via its block diagram representation. As clear from this figure, the OFC is a four (2x2) terminal device. Ideally, the voltage applied at terminal Y appears exactly at the terminal X with \( V_x \) is invariant with the input current \( I_x \). This is the voltage following action at the input ports. The current at terminal Y is ideally zero, corresponding to infinite input impedance at Y. The voltage at terminal W is the product of \( I_z \) and the trans-impedance \( Z_x \) while \( I_w \) is ideally conveyed to the terminal Z as \( I_z \). This action is called the current following action at the output ports. This ideal operation of the voltage and current actions can be mathematically represented in matrix form as \([8]\)

\[
\begin{bmatrix}
V_x(\omega) \\
I_y(\omega) \\
V_w(\omega) \\
I_z(\omega)
\end{bmatrix}
= 
\mathbf{T}^{(OFC)}(\omega)
\begin{bmatrix}
V_y(\omega) \\
I_x(\omega) \\
V_w(\omega) \\
I_z(\omega)
\end{bmatrix}
\]

(2)

where

\[
\mathbf{T}^{(OFC)}(\omega) = 
\begin{bmatrix}
0 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 \\
Z_t & 0 & 0 & 0 \\
0 & 0 & 1 & 0
\end{bmatrix}
\]

In what follows, the FDCCII is used as a basic constituting block in building a proposed differential form of the OFC such that voltage following actions, the current following actions and the differential property of both the FDCCII and the OFC are achieved.

III. THE PROPOSED FD-OFC

This section introduces the novel concept along with a proposed schematic for the model of the FD-OFC as an extension of the OFC circuit \([4],[5]\) reviewed in Section II. This extension is achieved by cascading the two output terminals of an FDCCII’s to two current followers via two inverting trans-impedance coupling amplifiers \([3]\), of \( -Z_t \) gain each, such that the current following action is achieved. The two outputs of the trans-impedance coupling amplifiers are assigned to two of the FD-OFC outputs (\( W_1 \) and \( W_2 \)), while the outputs of the two current followers are assigned to the other FD-OFC output terminals as \( Z_1 \) and \( Z_2 \). This configuration is illustrated in Fig. 2 via a block diagram representation, while the schematic diagram representations for the FDCCII- and the trans-impedance amplifier and the current follower are depicted in Fig. 3.

![Block diagram representation of the proposed FD-OFC. (a): a 4x4 port representation. (b): building blocks of the FD-OFC.](image)
Fig. 3. Schematic diagram representation of the (a): FDCCII- and (b): the integrated trans-impedance amplifier and the current follower.

operation in the fully differential mode. Accordingly, the ideal I/O terminal behavior can be expressed in terms of the transfer matrix $T_{FD-OFC}(\omega)$ of the OFC as follows.

$$
egin{bmatrix}
V_{xd}(\omega) \\
I_{yd}(\omega) \\
V_{wd}(\omega) \\
I_{zd}(\omega)
\end{bmatrix}
= T_{FD-OFC}(\omega)
\begin{bmatrix}
I_{xd}(\omega) \\
V_{yd}(\omega) \\
I_{wd}(\omega) \\
V_{zd}(\omega)
\end{bmatrix}
$$

(3)

where the $(i,j)$ entry of the FD-OFC transfer matrix is given by $T_{FD-OFC}(\omega)_{ij} = I_{2} \otimes (T_{OFC})_{ij}$. Accordingly, the FD-OFC transfer matrix can be expanded as follows.

$$
T_{FD-OFC}(\omega) =
\begin{bmatrix}
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
Z_t & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & Z_t & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 0 & 0
\end{bmatrix}
$$

(4)

where $I_{xd} = [I_{x1}, I_{x2}]^T$, $I_{yd} = [I_{y1}, I_{y2}]^T$, $I_{wd} = [I_{w1}, I_{w2}]^T$, $I_{zd} = [I_{z1}, I_{z2}]^T$, $V_{xd} = [V_{x1}, V_{x2}]^T$, $V_{yd} = [V_{y1}, V_{y2}]^T$, $V_{wd} = [V_{w1}, V_{w2}]^T$, $V_{zd} = [V_{z1}, V_{z2}]^T$.

The transfer matrix $T_{FD-OFC}(\omega)$ implicitly depends on the angular frequency $\omega$ through the frequency dependence of $Z_t$.

IV. NUMERICAL SIMULATIONS AND DISCUSSIONS

This section presents the numerical simulations that validate the analysis provided in Section III as well as the workability of the proposed design. The proposed FD-OFC circuit is simulated using the UMC 130nm CMOS-based technology kit in Cadence environment. The simulation starts by characterizing each of the MOSFET transistors in Fig. 3 via their geometrical structural design parameters, given in Table I and II as required by Cadence. The entire circuit is simulated using 1.2 Volt biasing conditions.

### TABLE I

<table>
<thead>
<tr>
<th>Transistor Name</th>
<th>Transistor Aspect Ratio W/L (\text{\mu m})</th>
</tr>
</thead>
<tbody>
<tr>
<td>M7-M10-M18-M21</td>
<td>63 7/0.59</td>
</tr>
<tr>
<td>M9-M11-M20-M22</td>
<td>55 9/0.59</td>
</tr>
<tr>
<td>M3-M16</td>
<td>20 8/0.13</td>
</tr>
<tr>
<td>M1-M2-M12-M13</td>
<td>11 96/0.13</td>
</tr>
<tr>
<td>M3-M4-M14-M15</td>
<td>5 9/0.13</td>
</tr>
<tr>
<td>M6-M17</td>
<td>11 18/0.13</td>
</tr>
<tr>
<td>M8-M19</td>
<td>7 54/0.13</td>
</tr>
</tbody>
</table>

### TABLE II

<table>
<thead>
<tr>
<th>Transistor Name</th>
<th>Transistor Aspect Ratio W/L (\text{\mu m})</th>
</tr>
</thead>
<tbody>
<tr>
<td>M9 M12 M13</td>
<td>3.0 0.65</td>
</tr>
<tr>
<td>M10 M11</td>
<td>2.6 0.65</td>
</tr>
<tr>
<td>M14</td>
<td>2.0 0.13</td>
</tr>
</tbody>
</table>

Table III shows a comparison between the proposed design for the fully differential OFC and the design in [9] for the same device. Figs. 4 (a), (b) and (c) plot the magnitude frequency response (in dB) and the phase response (in degrees) resulting from the simulation of the FD-OFC, proposed in Section III, at frequencies ranging from 0 (DC) up to 10 GHz. Although the transfer matrix in (6) is generally frequency dependent, the magnitude and phase frequency responses in these three figures are essentially invariant with frequency up to about 10 MHz. Accordingly, the I/O behavior can be easily tracked within this frequency range. Clearly, Fig. 4 (a) confirms the voltage following action between the differential terminals $(X,Y)$ with a3-dB bandwidth of 600 MHz, with a gain of 0 dB and a constant phase shift of $0^\circ$. In Fig. 4 (b), the current following action between the differential terminals $(Z,W)$ is achieved with a gain of 0.6 dB and a constant phase shift of $0^\circ$, up to 25 MHz. Fig. 4 (c) illustrates that a transimpedance
gain between the differential terminals (W,X) is achieved with an open loop gain and phase shift of 104 dB and 0°, respectively. The abovementioned observations lead to the correct conclusion that the overall bandwidth of the proposed FD-OFC is about 600 MHz and an invariant response up to 10 MHz if both the magnitude and phase frequency responses are simultaneously concerned for the four differential terminals and a distortion free processing is desired. However, this range is extended to more than 100 MHz as long as the magnitude frequency response is the only design criteria of interest. This confirms the suitability of the proposed FD-OFC for the nominal switching speeds of analog applications.

V. CONCLUSION

This paper presents the novel design for the concept of the fully differential-OFC as an extension of the conventional OFC. A CMOS-based circuit design for the proposed device is introduced and simulated. Simulations results indicate that the proposed concept and circuit design are perfectly suitable for low power-high speed applications as it can operate under biasing conditions as low as 1.2 volts and bandwidths as high as 600 MHz with higher open loop transimpedance gain of 104 dBs. Moreover, the fully differential action offered by the proposed device makes it a perfect candidate for applications in which a high noise rejection ratio is desired like differential voltage amplifier, instrumentation amplifier and universal filters.

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REFERENCES