The Impact of FinFET Technology Scaling on Critical Path Performance under Process Variations

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Abstract—Comparisons of FinFET based ring oscillator (RO) metrics are evaluated with technology scaling from 20nm to 7nm technology. Simulations are based on predictive technology models (PTM) developed by Arizona state university. The impact of process and temperature variations on frequency, power, and power delay product is reported. Performance and power of the RO are improved with technology scaling, however performance is degraded after 14nm technology.

Index Terms — Nano-scale FinFET, Ring Oscillator, Process variations.

I. INTRODUCTION

Tri-gate (TG) FinFET becomes one of the most promising Alternative structures to keep on the industry scaling trend for future technology generations of 22 nm and beyond [1]. The tri-gate FinFET provides a symmetric device architecture where the channel is controlled by gate from three sides of the Si film. Since the gate control is increased, the requirements on the Si film thickness are relaxed as compared to single gate or double gate FinFET. Compared to FDSOI MOSFET or double gate FinFET, the tri-gate FinFETs are better due to the increased gate control over the channel. So we can efficiently control the short channel effects and also further scaling is possible to meet the ITRS trends [2].

Multiplexers are typical building block for datapaths, and are used extensively in a variety of applications, they are used in both logic blocks and routing channels in programmable logic devices and FPGAs [3].

One of the major design challenges for sub-micron technologies is reliability. Shrinking geometries, lower supply voltages, higher clock frequencies, and higher density circuits all have a great impact on reliability. Variations in critical dimensions (CD), random dopant fluctuation (RDF), voltage variations, temperature variations, bias temperature instability (BTI), and hot carrier injection (HCI) have a direct impact on threshold voltage of the device [4] [5] [6].

Some studies have discussed designing low power high performance multiplexers [7], and design benchmarking to 7nm with FinFET predictive technology models [8]. In this study, we report a critical path (RO) simulation performance and power dissipation variations due to limits within a given range of threshold voltage variations along with different technology nodes starting from 20 nm down to 7 nm.

This paper is organized as follows. Section II explains the simulation setup and methodology. Results and discussions are presented in section III. Some conclusions are drawn in section IV.

II. SIMULATION METHODOLOGY

In this paper, low-standby power devices (LSTP) predictive technology models (PTM-MG) [9] based on BSIM-CMG for multi-gate devices (Tri-gate FinFET) are used from 20nm down to 7nm technology nodes. A scaling strategy is adopted according to the PTM models which involves: scaling of the channel length (L), scaling of the supply voltage ($V_{dd}$), fin thickness ($T_{fin}$), and fin height ($H_{fin}$). For tri-gate FinFET devices the effective channel width is given by:

$$W = N_{fin}(2H_{fin} + T_{fin})$$

1

We extracted the nominal threshold voltage values at each technology node using Ids-Vgs characteristic curve first derivative method as shown in Fig. 2. We studied the threshold voltage variations within the ±18% range with 6% step of the nominal threshold voltage. The simulated FinFET device parameters are reported in Table 1.

The nominal threshold voltage is decreased with technology scaling since supply voltage also is decreased with technology scaling to satisfy high performance and low power requirements. The studied RO consists of 16:1 pass transistor multiplexer with three stages of logic gates (INV, 2-inputs NOR, and 2-inputs NAND).
Bias temperature instability (BTI), and hot carrier injection (HCI) have a direct impact on threshold voltage of the device, normally their shift the threshold voltage within ±18% of the nominal threshold value. Temperature, variations in critical dimensions (CD), random dopant fluctuation (RDF) also shift the threshold voltage of the device. The nominal threshold voltages at each technology is calculated according to Ids-Vgs characteristic curve first derivative method.

### III. SIMULATION RESULTS AND DISCUSSIONS

In this section, we present the simulation results of the RO shown in Fig. 1. We run the experiments considering process and temperature variations.

The RO is sized for minimal dimensions with one fin for each transistor. Transistor channel lengths, and nominal supply voltages are according to PTM low-standby power models and are reported in Table 1.

#### Table 1: The simulated device parameters

<table>
<thead>
<tr>
<th>Device</th>
<th>TG-FinFET</th>
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<tbody>
<tr>
<td>L (nm)</td>
<td>20 16 14 10 7</td>
</tr>
<tr>
<td>T fin</td>
<td>15 12 10 8 6.5</td>
</tr>
</tbody>
</table>

#### A. Performance

Fig. 3, and Fig. 4 show that the performance of the ring oscillator is improved with technology scaling, however scaling reverses beyond 14nm, while alternate trajectories with higher VDD would lead to improved performance at the cost of reduced power scaling. Device scaling options such as high mobility channels [10] and/or gate-all-around (GAA) nanowires [11] hold the potential to improve device scaling in this time frame, and are obvious areas for future work as research clarifies these potential device paths. For 7nm technology, the frequency period at the nominal threshold value is higher than the 14nm technology nominal threshold frequency period by a factor of 1.18, however the power is lower by a factor of 1.76.

Performance sensitivity (frequency variations normalized to the frequency nominal value) increases with technology scaling. For 7nm technology at +18% threshold variation, the frequency period is increased by a factor of 1.05 of its nominal value, however the 20nm technology frequency period at +18% threshold variation is increased by a factor of 0.6.

Also Performance trends are improved with temperature increase and degraded with threshold voltage increase. For 7nm technology, the frequency period at 120 temperature degree is lower than the 27 temperature degree frequency period by a factor of 0.45.

#### B. Power consumption

Power trends are improved with technology scaling as shown in Fig. 5, and Fig. 6. As a result of supply voltage scaling and other technology scaling effects. For 7nm the power at the nominal threshold value is lower than the 20nm nominal threshold power by a factor of 0.43. Power sensitivity (power variations normalized to the power nominal value) increases with technology scaling. For the 7nm technology power at +18% threshold variation, the power is decreased by a factor of 0.52 of its nominal value, however the 20nm technology power at +18% threshold variation is decreased by a factor of 0.41. Power trends are improved with threshold voltage increase and degraded with temperature increase. For 7nm technology, the power at 120 temperature degree is higher than the 27 temperature degree power by a factor of 1.2.

#### C. Power Delay Product (PDP)

As the power and the delay always have a trade-off, power delay product is used as a figure of merit. Observing power delay product trends with technology scaling, the power delay product is continuously decreasing.
(Improved) with technology scaling as shown in Fig. 7, and Fig. 8. For 7nm technology, the PDP at the nominal threshold value is lower than the 20nm technology nominal threshold PDP by a factor of 0.3.

Power delay product trends are improved with threshold voltage increase and degraded with temperature increase. For 7nm technology, the PDP at 120 temperature degree is higher than the 27 temperature degree PDP by a factor of 0.2.

As temperature increases RO driving current increases, hence the frequency period is decreased. For 7nm technology, the frequency period at 120 temperature degree is lower than the 27 temperature degree frequency period by a factor of 0.45.

Low power designs are so important nowadays not only for battery life for mobile devices but also for reducing cooling costs. From our study, power consumption of RO is decreased with technology scaling. For 7nm the power at the nominal threshold value is lower than the 20nm nominal threshold power by a factor of 0.43.

Increasing temperature has a proportional relation with RO power dissipation, since the driving current increases the dissipated power of RO is increased. For 7nm technology, the power at 120 temperature degree is higher than the 27 temperature degree power by a factor of 1.2.
It can be concluded that RO power delay product trends are continuously decreasing with technology scaling. For 7nm technology, the PDP at the nominal threshold value is lower than the 20nm technology nominal threshold PDP by a factor of 0.3.

PDP of RO has a proportional relation with temperature, due to power dominance. PDP increases with technology scaling. For 7nm technology at 120 degree temperature, the PDP is increased by a factor of 0.2 of its nominal value, however the 20nm technology PDP at same temperature is increased by a factor of 0.1.

From our study, we can observe improvement of performance with technology scaling till 14nm. Power dissipation decreases with technology scaling, and PDP decreases with technology scaling.

Threshold voltage increase has a positive effect on the power consumption, however it degrades the performance, but it enhances the PDP. Temperature increase has a negative effect on the power dissipation, and the PDP, however it enhances the performance.

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IV. CONCLUSION

Performance of FinFET Ring Oscillator (RO) based on predictive technology models (PTM-LSTP) is evaluated with technology scaling. The impact of a given range of threshold voltage and temperature variations on basic performance metrics is reported. The results show that, the performance is enhanced with technology scaling, however after the 14nm node and down to the 7nm clear performance degradation is observed. The degradation of the performance of RO with technology scaling as a result of scaling other parameters besides the channel length.

The study also shows that, with technology scaling the power consumption is reduced, and the power delay product is enhanced, however the sensitivity of the power and frequency to threshold and temperature variations is increased with technology scaling. Also power delay product trends are improved with threshold voltage increase and degraded with temperature increase.

REFERENCES