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Modified Mixed-Mode Universal Filters Using DVCC

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New modified mixed-mode universal filters using the Differential Voltage Current Conveyor (DVCC) are introduced. The proposed circuits have the advantages of a using all grounded passive elements, employ DVCC with Z+ output only and have very low input impedance. Simulation results are included to demonstrate the practicality of the proposed circuits.

Keywords: Mixed mode, Universal filters, Differential Voltage Current Conveyor (DVCC).

1 INTRODUCTION

Since the current conveyor mixed-mode universal filter was published in [1] and several mixed-mode filters were followed in the literature [2–7]. The mixed mode filters reported in [1] are driven by input current and they realize three output voltages, that is they realize transfer impedance functions. The main disadvantage is that the input impedance is not very small as it should be in the ideal case of current driven circuits and they employ one floating resistor. Before considering the improved mixed mode circuits a brief review of the circuits reported in [1] is given next.

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2 CCII MIXED MODE UNIVERSAL FILTERS

The first mixed-mode circuit given in [1] is shown in Fig. 1(a) which realizes the high-pass, band-pass and low-pass responses at the three CCII outputs. Fig. 1(b) represents the block diagram of the circuit of Fig. 1(a). The mixed-mode transfer functions are given by:

$$\frac{V_1}{I_i}=\frac{-R_4 s^2}{D(s)}\ ,\ \frac{V_2}{I_i}=\frac{\dfrac{R_4 s}{C_1 R_1}}{D(s)}\ ,\frac{V_3}{I_i}=\frac{-\dfrac{R_4}{C_1 C_2 R_1 R_2}}{D(s)} \tag{1}$$

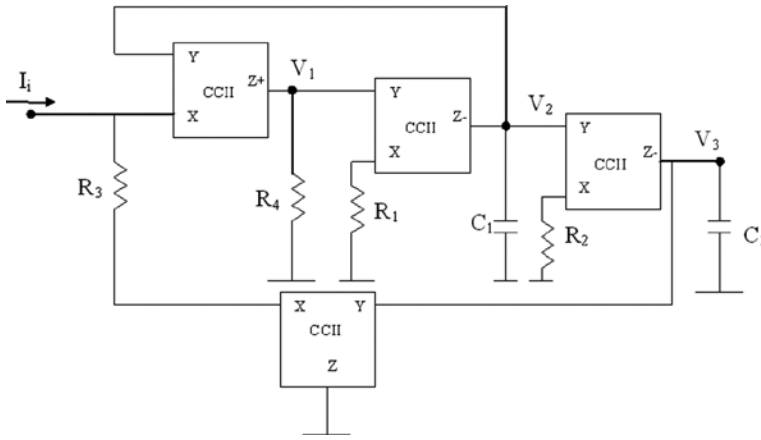

FIGURE 1A
First mixed mode circuit reported in [1].

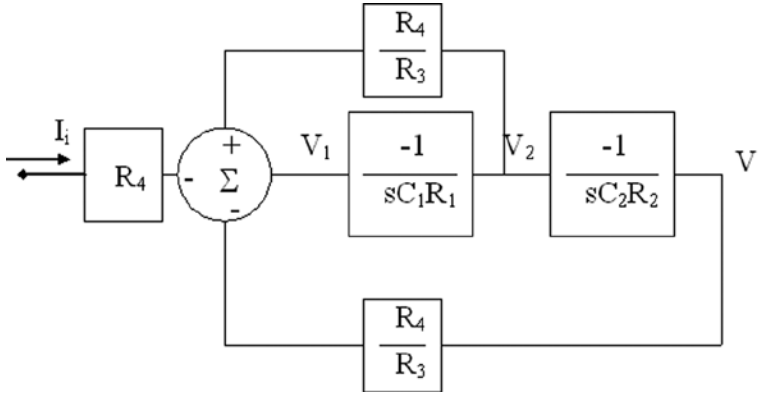

FIGURE 1B
Block diagram of the circuit in Fig. 1(a).

Where $$D(s)=s^2+\frac{R_4 s}{C_1R_1R_3}+\frac{R_4}{C_1C_2R_1R_2R_3} \quad (2)$$

The ωo and Q are given by:

$$\omega_o=\sqrt{\frac{R_4}{C_1C_2R_1R_2R_3}}\ ,\ Q=\sqrt{\frac{C_1R_1R_3}{C_2R_2R_4}} \quad (3)$$

The design given in [1] is based on taking $C_1 = C_2 = C$, $R_1 = R_3$ and $R_2 = R_4$ and the design equations are given by:

$$R_1 = R_3 = 1/\omega oC,\quad R_2 = R_4 = R_1/Q \quad (4)$$

The second mixed-mode circuit given in [1] is shown in Fig. 2(a) which also realizes the high-pass, band-pass and low-pass responses at the three CCII outputs. Fig. 2(b) represents the block diagram of the circuit of Fig. 2(a). The mixed-mode transfer functions are given by:

$$\frac{V_1}{I_i}=\frac{R_4s^2}{D(s)}\ ,\ \frac{V_2}{I_i}=\frac{-\frac{R_4s}{C_1R_1}}{D(s)}\ ,\ \frac{V_3}{I_i}=\frac{\frac{R_4}{C_1C_2R_1R_2}}{D(s)} \quad (5)$$

D(s) is the same as given by equation (2).

The circuit has opposite transfer function polarities to the circuit of Fig. 1(a). Equations (3) and (4) apply also to this circuit.

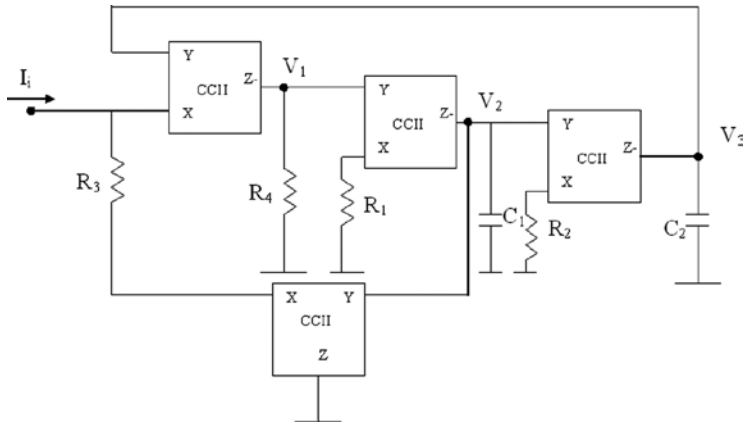

FIGURE 2A
Second mixed mode circuit reported in [1].

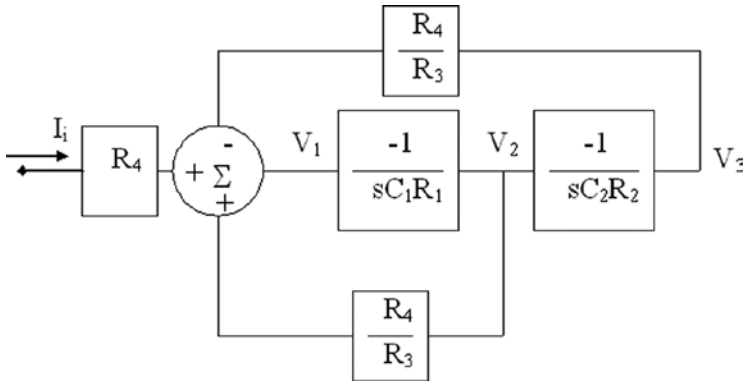

FIGURE 2B
Block diagram of the circuit in Fig. 2(a).

3 DVCC MIXED MODE UNIVERSAL FILTERS

The Differential Voltage Current Conveyor (DVCC) was introduced in [8], and has also been independently introduced and defined in [9] as the Differential Difference Current Conveyor. The DVCC is defined as a four port building block with a describing matrix of the form:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_x \\ V_z \end{bmatrix} \tag{6}$$

Four new circuits realizing the mixed-mode universal filters and using four DVCC are introduced next.

The first two circuits are equivalent to the circuit of Fig. 1(a) and are shown in Fig. 3(a) and Fig. 3(b) respectively. The block diagram given in Fig. 1(b) represents these circuits and equations (1) to (4) apply to both of these circuits. Each of the proposed circuits use four DVCC with Z+ outputs only thus avoid the current mirrors at the Z outputs. All passive elements are grounded which is an advantage [10] over the circuits of Figures 1 and 2 which uses one floating resistor.

The main difference between the two circuits of Fig. 3(a) and 3(b) is in the mixing node of the feedback current from DVCC number 4 to the DVCC number 1. In Fig. 3(a) the current feedback from DVCC number 4 is mixed with Ii at node X of the DVCC number 1. In this case the parasitic resistance

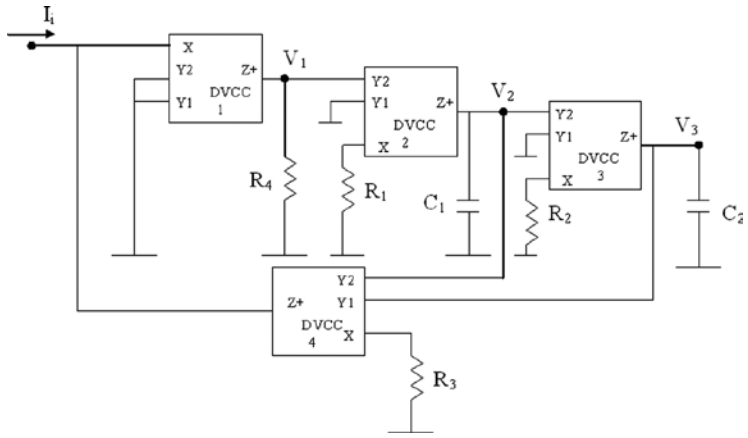

FIGURE 3A
Mixed mode universal filter-A-1 equivalent to Fig. 1(a).

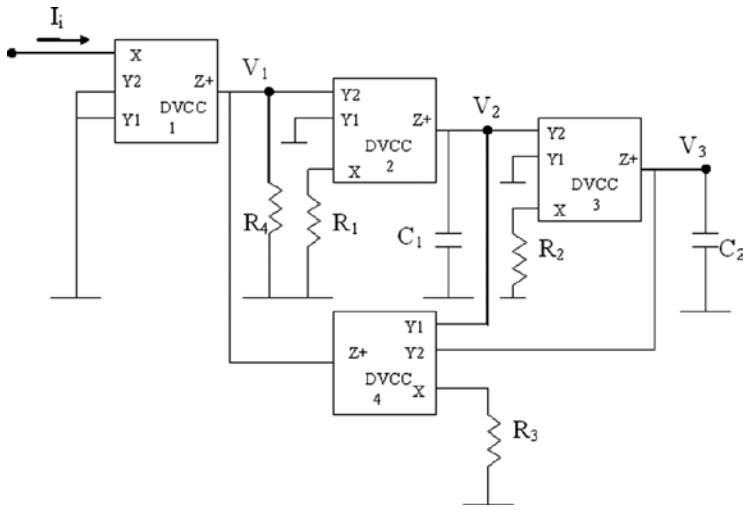

FIGURE 3B
Mixed mode universal filter-A-2 equivalent to Fig. 1(a).

R_{x1} will interact with C_{z4} and will affect the circuit operation at very high frequencies depending on the parasitic values. The other parasitic parameter affecting the circuit of Fig. 3(a) at very high frequencies is C_{Z1} which acts in parallel with R_4 to produce a first order pole. All other parasitic parameters namely R_{x2}, R_{x3}, R_{x4}, C_{z2}, C_{z3} can be self compensated by absorbing their values in R_1, R_2, R_3, C_1 and C_2 respectively.

On the other hand in the circuit of Fig. 3(b) the current feedback from DVCC number 4 is mixed at node Z+ of the DVCC number 1. In this case R_{x1} has no effect on the circuit performance.

The parasitic parameters affecting this circuit are $(C_{z1} + C_{z4})$ which act in parallel with R_4 to produce a first order pole. All other parasitic parameters namely R_{x2}, R_{x3}, R_{x4}, C_{z2}, C_{z3} can be self compensated by absorbing their values in R_1, R_2, R_3, C_1 and C_2 respectively.

Two more mixed mode circuits using four DVCC with single Z+ outputs are shown in Fig. 4(a) and 4(b).They are based on using a positive integrator followed by a negative integrator as described in the block diagram of Fig. 4(c).

The mixed-mode transfer functions are given by:

$$\frac{V_1}{I_i} = \frac{-R_4 s^2}{D(s)}, \quad \frac{V_2}{I_i} = \frac{-\frac{R_4 s}{C_1 R_1}}{D(s)}, \quad \frac{V_3}{I_i} = \frac{\frac{R_4}{C_1 C_2 R_1 R_2}}{D(s)} \tag{7}$$

D(s) is the same as given by equation (2). Equations (3) and (4) apply also to this circuit.

The main difference between the two circuits of Fig. 4(a) and 4(b) is in the mixing node of the feedback current from DVCC number 4 to the DVCC number 1 and all comments on the parasitic elements mentioned above for the circuits of Fig. 3 apply also to the circuits of Fig. 4.

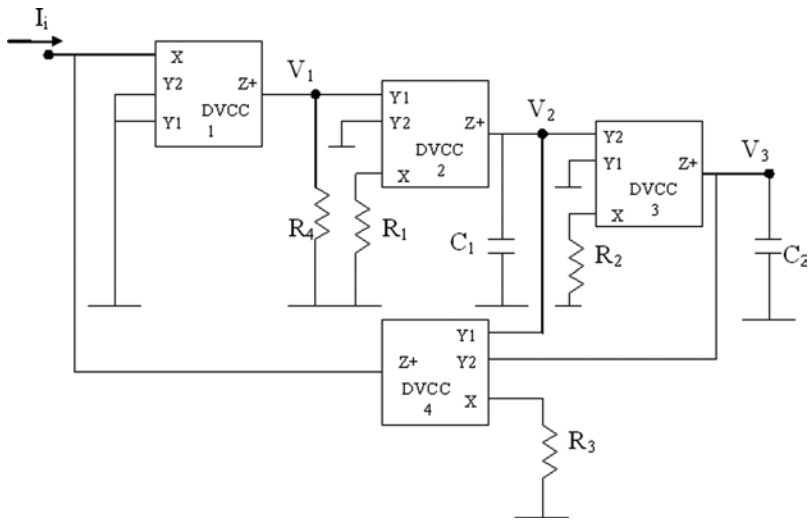

FIGURE 4A
Mixed mode universal filter-B-1.

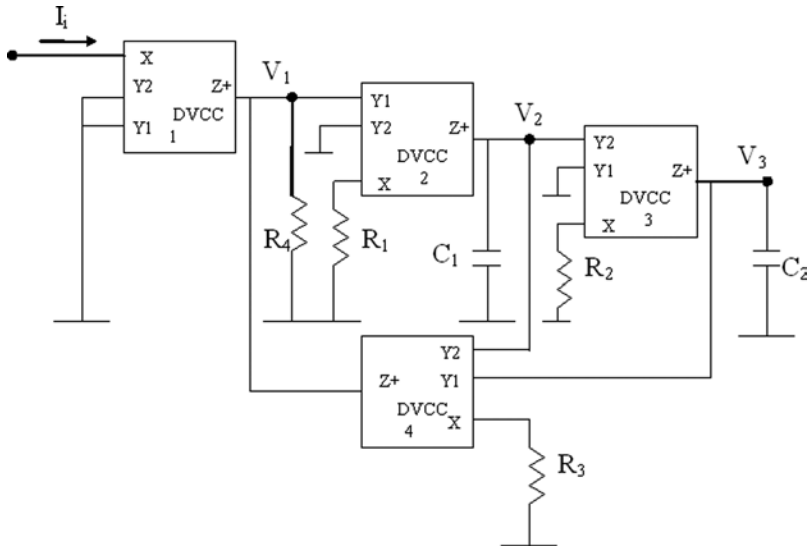

FIGURE 4B
Mixed mode universal filter-B-2.

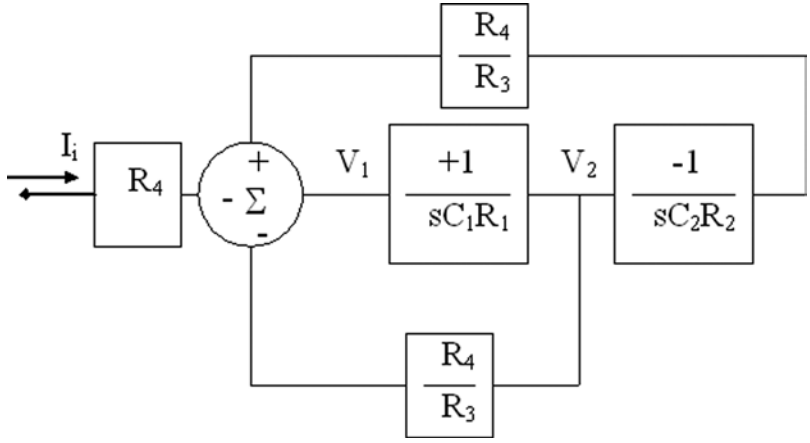

FIGURE 4C
Block diagram of the circuit in Fig 4(a) and 4(b)

4 SIMULATION RESULTS

The four proposed circuits are simulated using the CMOS DVCC circuit shown in Fig. 5 [8]. The transistor aspect ratios are given in Table I based on

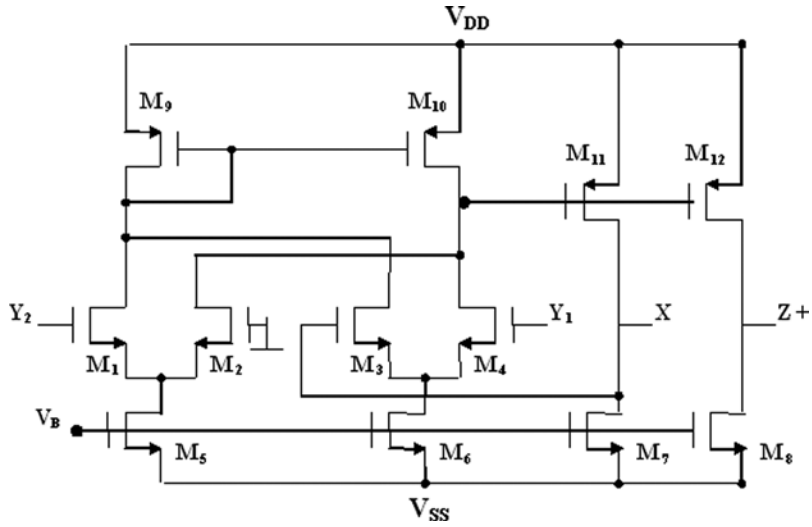

FIGURE 5
CMOS circuit of the DVCC with Z+ output [8].

TABLE 1
Dimensions of the MOS Transistors in the DVCC of Fig. 5.

NMOS Transistors	**W(μm)/L(μm)**
M_1, M_2, M_3, M_4	4/1
M_5, M_6, M_7, M_8	8/1
PMOS Transistors	**W(μm)/L(μm)**
M_9, M_{10}	10/1
M_{11}, M_{12}	16/2

the 0.5 μm CMOS model from MOSIS. The supply voltages used are $\pm$ 1.5 V and $V_B = -0.5$ V.

Each of the four circuits is designed for fo = 1 MHz and Q = 10 by taking $C_1 = C_2 = 10$ pF, $R_1 = R_3 = 15.9\,\text{k}\Omega$ and $R_2 = R_4 = 1.59\,\text{k}\Omega$

The Spice simulation results for the four circuits are shown in Figures 6 and 7 indicating good agreement with the theoretical expected results.

CONCLUSIONS

Four new modified mixed-mode universal filters using the Differential Voltage Current Conveyor (DVCC) are introduced. The proposed circuits

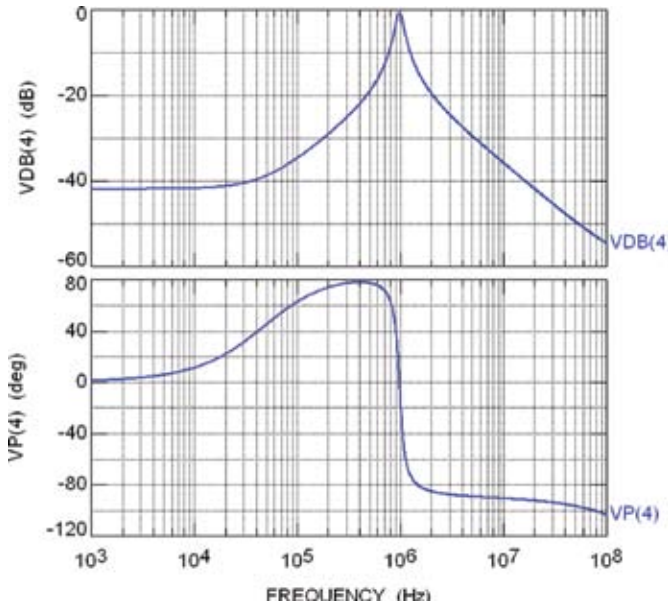

FIGURE 6A
Magnitude and phase of the circuit of Fig. 3(a).

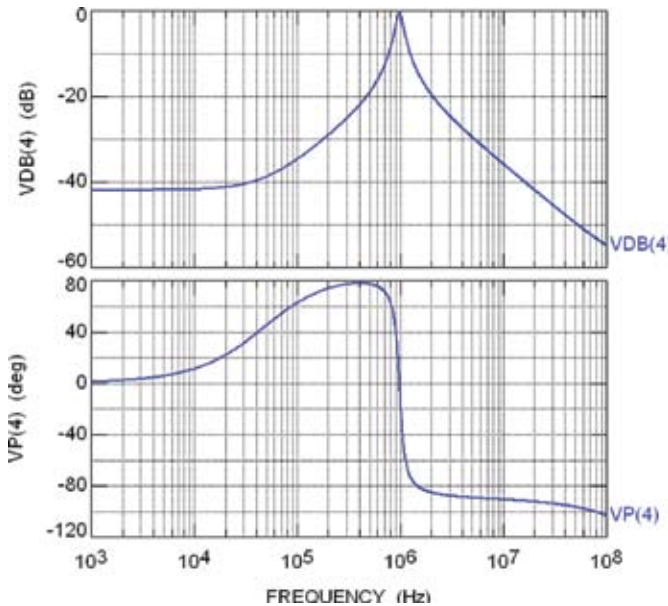

FIGURE 6B
Magnitude and phase of the circuit of Fig. 3(b).

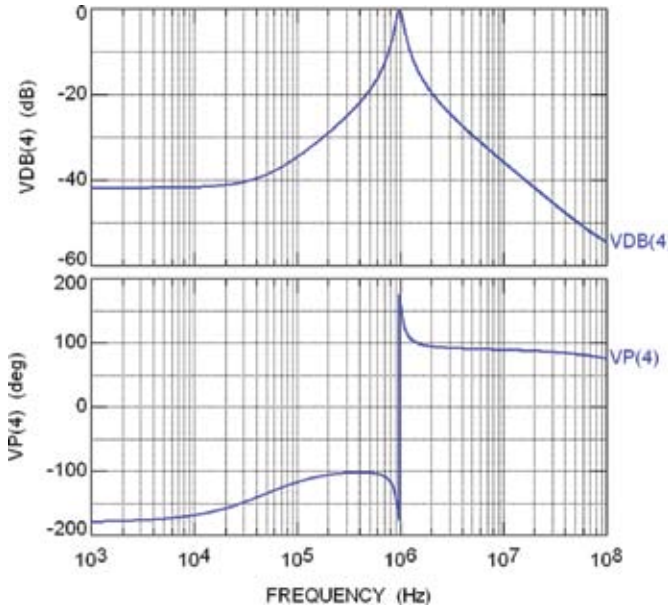

FIGURE 7A
Magnitude and phase of the circuit of Fig. 4(a).

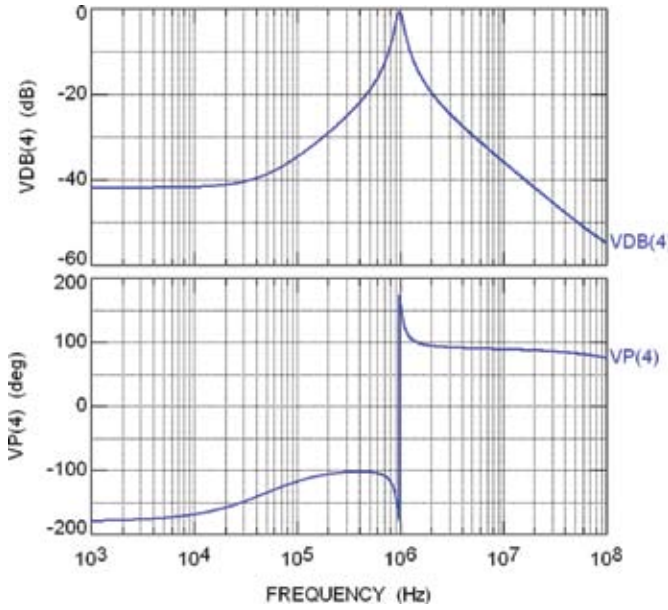

FIGURE 7B
Magnitude and phase of the circuit of Fig. 4(b).

have the advantages of a using all grounded passive elements, employ DVCC with single Z+ output only and have very low input impedance. Simulation results are included to demonstrate the practicality of the proposed circuits.

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