On Series Connections of Fractional-Order Elements and Memristive Elements

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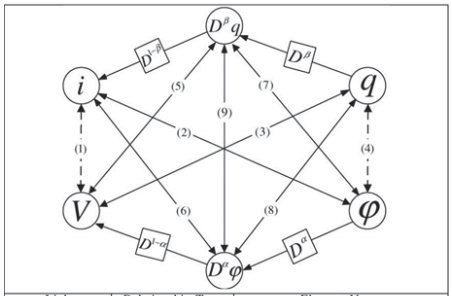
***Abstract*—This paper proposes a current-controlled fractional-order memristor emulator based on one active building block. The emulator consists of a multiplication mode current conveyor (MMCC) block with three passive elements. Additionally, the series connection of fractional-order inductor (FOI) and fractional-order capacitor (FOC) with memristive elements in the $i-v$ plane is demonstrated numerically for different cases. Changing the order of the FOC or FOI and its effect on the pinched hysteresis loop area are investigated, which improve the controllability of the double loop area, the location of the pinched point, and the operating frequency range. Numerical, PSPICE simulation results, and experimental verification are investigated for different cases to approve the theoretical findings. Moreover, a sensitivity analysis using Monte Carlo simulations for the tolerance of the discrete components of the memristor emulator is investigated.**

***Keywords*—Memristor, MMCC, Emulator, FOC, Pinched hysteresis, Fractional-order circuits.**



Link	Relationship Type	Element Name
(1), (4) and (9)	Linear	Resistor
(2)	Linear	Inductor
(3)	Linear	Capacitor
(4)	Nonlinear	Memristor
(5) and (8)	Linear	Fractiona-order Capacitor (FOC)
(6) and (7)	Linear	Fractional-order Inductor (FOI)
(9)	Nonlinear	Fractional-order Memristor (FOM)

Fig. 1. The relation between fractional-order elements and memelements.

I. Introduction

Chua discovered the fourth electrical circuit element named memristor [1]. One of the most widely known characteristics of the memristor is the pinched hysteresis loop, which is defined by the nonlinear relation between the voltage and current measured under periodic excitation. In [2], the inverse memristor was proposed where the hysteresis loop area is increased with increasing the applied frequency. The memristor is recently employed in many applications, such as oscillators [3], encryption [4],chaotic circuits [5], and logic circuits [6].

Until now, the memristive elements are not commercially available as two-terminal devices. Several circuits have been proposed in the literature to simulate their behavior [7]. Based on a TiO2 model, the grounded memristor emulator was built-in [8] using a second-generation current conveyor (CCII) and an operational transconductance amplifier (OTA). In [9], the grounded and floating memristor emulators were presented based on the current differencing transconductance amplifier (CDTA). The performance of the proposed memristor emulator was employed in the realization of a current-mode analog filter. Employing CCII with a multiplier, grounded, and floating higher-order emulation circuits were proposed in [5], providing more than one pinched point. The floating memristor emulator was realized using the current conveyor transconductance amplifier (CCTA) block with three resistors and one capacitor in [10]. The emulator in [10] was realized employing the CMOS technology and the integrated circuits such as AD844 and CA3080. Besides, it was applied to different applications such as high-pass filter and Chua's oscillator. A tunable memristor emulator was proposed in [11] using OTA plus two passive elements. The inverse memristor emulator was proposed using two BJT transistors with parallel RC and applied on a chaotic circuit [12]. The fractional calculus (FC) which is the generalization of conventional calculus [13] was associated with memristive systems in several applications [5], [14]. The relations between the fractional-order elements and memelements are illustrated in Fig. 1 and discussed in [15]. The fractional-order parameters provide a further degree of freedom and increase the controllability of the system [16].

The paper presents a memristor emulation circuit using one active block with three passive elements. Also, the serial connection of different fractional-order elements and the memristor is investigated. The FOC order's effect on the memristor's characteristics is discussed based on numerical and PSPICE results in the i vs. v plane. Also, the tolerance of the memristor emulator's passive components on the memristor characteristics is investigated using Monte Carlo analysis.

The organization of this paper is as follows: section II presents the memristor emulator based on the MMCC block. In section III, the series connection of memristor/inverse memristor with FOI and FOC in the i vs.v curve is presented. In section IV, the PSPICE simulations and experimental results are discussed for different cases. Finally, the conclusion of the work is in section V.

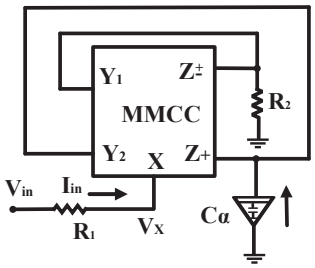


Fig. 2. The proposed current-controlled memristor emulator.

II. The Proposed Memristor Emulator

A very useful analog block called MMCC was firstly proposed in [17]. It consists of a differential voltage current conveyor (DVCC) preceded by a folded Gilbert multiplier. The relationships of the MMCC block between its terminal characteristics are defined as follows:

$$I_{Y1} = I_{Y2} = 0, \tag{1a}$$
$$V_X = V_{Y1} V_{Y2}, \tag{1b}$$
$$I_Z = \pm I_X, \tag{1c}$$

The MMCC is a main building block in many electric circuits such as the voltage-controlled and the current-controlled oscillator [18]. The implementation of the current-controlled memristor emulator is proposed in Fig. 2 employing one MMCC block. By direct analysis of Fig. 2, the input voltage is defined as follows:

$$v_{in}(t) = I_{in} R_1 + v_X, \tag{2}$$

where V_X is the voltage at X-terminal which is given by:

$$v_X(t) = k \frac{R_2}{C} q_\alpha(t) i_{in}(t), \tag{3}$$

where k represents the voltage multiplier gain and the q_α represents the fractional integral of the input current. The memristance is thus given by:

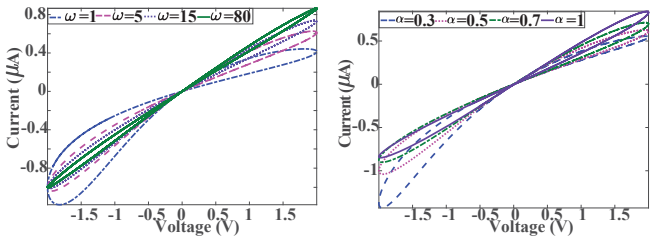
$$R_m = R_1 \mp k \frac{R_2}{C} q_\alpha(t), \tag{4}$$

where the positive/negative means incremental/decremental memductor, respectively. One of the main characteristics of the memristor is the hysteresis loop in the i - v plane, which is decreased with increasing the applied frequency as depicted in Fig. 3(a). Also, the hysteresis loop of the memristor is introduced in Fig.3(b) at different values of α where the hysteresis loops are symmetric at $\alpha = 1$ and asymmetric for $\alpha < 1$.

III. Series connection of FOI and FOC with memristive elements

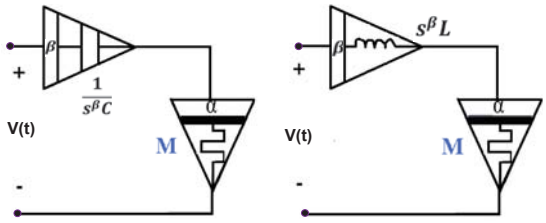
The general mathematical model of different electrical circuit connection with memristor and inverse memristor is defined in [19] and is depicted as follows in the fractional-order domain:

$$v(t) = a i(t) + b D_t^\alpha i(t) + k i(t) D_t^\beta i(t) + f J^\beta i(t) + h i(t) J^\alpha i(t), \tag{5}$$



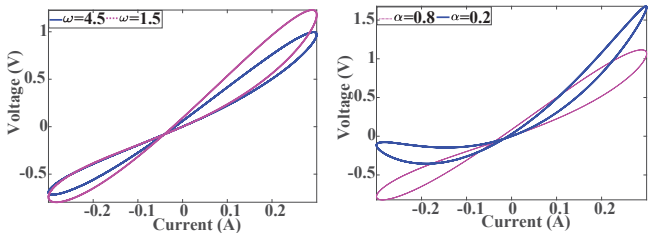
(a) (b)

Fig. 3. Numerical simulations of memductance for $a = 9 \times 10^{-5}$at different (a) frequencies when $\alpha = 0.7$, and (b) α when f=0.16Hz



(a) (b)

Fig. 4. Series fractional-order memristor with (a) FOC, and (b) FOI.



(a) (b)

Fig. 5. Numerical simulations of fractional-order memristor connected in series with FOC at different (a) ω when $\alpha = \beta = 0.7$ (b) α when $\beta = 0.8$ at $\omega = 4.5$.

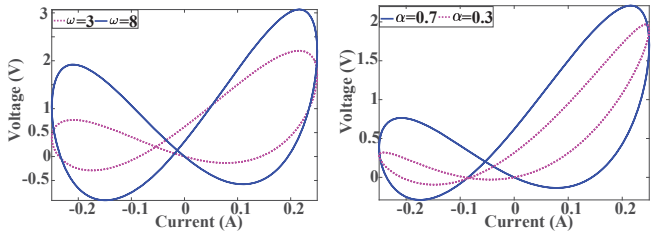
where (a, b, k, f, h), D_t^α, and J_t^β are constants, fractional-order derivative and integral operation, respectively. Based on Eqn.5, the fractional inductor and capacitor are realized when $b = L$ and $f = 1/C$ and all constants are zero, respectively. The fractional-order memristor and inverse memristor are also realized at (a, h) and (a, k) are non-zero. The effect of the series connection of the fractional-order memelements and fractional-order passive elements on the pinched hysteresis lobes is discussed next.

A. Series fractional-order memristor/inverse memristor with FOC element

The series connection of the fractional-order memristor and the FOC is depicted in Fig.4(a). Based on Eqn.5, the total voltage yields as follows:

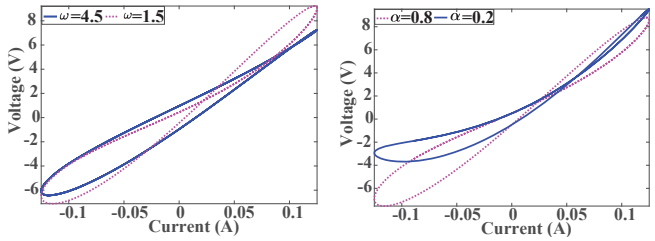
$$v(t) = (a + h J_t^\alpha i(t)) i(t) + \frac{1}{C} J_t^\beta i(t), \tag{6}$$

where a and h are the initial memristance and scaling constant, respectively. On applying a sinusoidal current $i_{in}(t) = i_0 sin(\omega t)$, the fractional integration of the sinusoidal current at steady state can be written as $J^\alpha(i_0 sin(\omega t))|_{s.st} =$



(a) (b)

Fig. 6. Numerical simulations of fractional-order inverse memristor connected in series with FOC at different (a) ω at $\alpha = \beta = 0.7$, and (b) α when $\beta = 0.8$ and $\omega = 3$



(a) (b)

Fig. 7. Numerical simulations of series fractional memristor and FOI at different (a) ω at $\alpha = \beta = 0.7$, (b) α when $\beta = 0.8$ and $\omega = 1.5$.

$i_0\omega^{-\alpha}(sin(\omega t - \frac{\alpha\pi}{2}) + sin(\frac{\alpha\pi}{2}))$ [15]. The total voltage is given by:

$$v(t) = (a+hi_0\omega^{-\alpha}(sin(\omega t-\frac{\alpha\pi}{2})+sin(\frac{\alpha\pi}{2})))i(t)+\frac{1}{C}q_\beta(t), \quad (7)$$

where $q_\beta(t) = i_0\omega^{-\beta}(sin(\omega t - \frac{\beta\pi}{2}) + sin(\frac{\beta\pi}{2}))$. Based on Eqn.7, the mathematical results of the two elements is investigated where the circuit parameters are chosen as $a = 2\Omega$, $h = 6$, and $C = 0.5F/sec^{1-\beta}$. At different values of ω, the i vs. v plane is depicted in Fig.5(a) where the area of the hysteresis lobes decreases with increasing the frequency of operation. The pinched point location moves in the negative direction as the α changes at $\beta = 0.8$ as presented in Fig.5(b). With the same procedure, the series connection of fractioal-order inverse memristor with FOC is written as follows:

$$v(t) = (a + hD_t^\alpha i(t))i(t) + \frac{1}{C}J_t^\beta i(t), \quad (8)$$

Figures 6 (a) and (b) display the impact of different ω and α values on the hysteresis lobe region and the pinched point location, respectively.

B. Series fractional-order memristor/inverse memristor and FOI element

The series connection of the fractional-order memristor and the FOI element is introduced in Fig.4(b) where the steady-state voltage is given as follows:

$$v(t) = (a+hi_0\omega^{-\alpha}(sin(\omega t-\frac{\alpha\pi}{2})+sin(\frac{\alpha\pi}{2})))i(t)+LD_t^\beta i(t), \quad (9)$$

where $D_t^\beta i(t) = i_0\omega^\beta(sin(\omega t - \frac{\beta\pi}{2})$. The numerical results of the series memristor and FOI elements is investigated where the circuit parameters are $a = 40\Omega$, $h = 60$, and

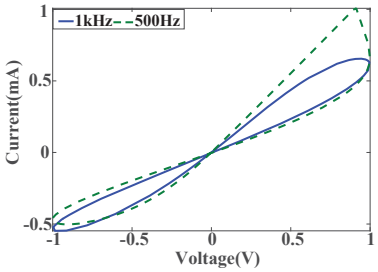


Fig. 8. The simulation results of incremental memristor for different frequencies at $\alpha = 0.8$.

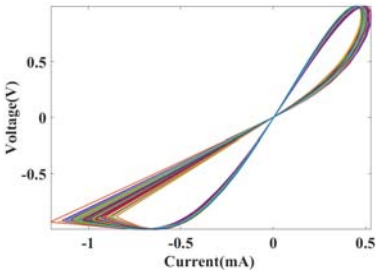


Fig. 9. The Monte Carlo results for the hysteresis loop of the memristor in the I-V plane at $\alpha = 0.8$.

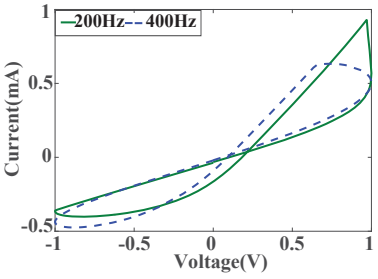


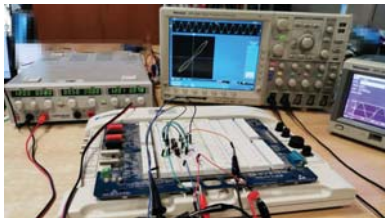
Fig. 10. The simulation results of the series connection of the fractional-order memristor and FOC at different frequencies.

$L = 0.3H/sec^{1-\beta}$. The i - v plane at different values of ω is presented in Fig.7(a) where the pinched point location is moved in the positive direction as the ω changes. Also, the effect of the different values of α on the pinched point location and hysteresis lobes area is presented in Fig.7(b). The series connection of the fractional-order inverse memristor with FOI is given at the steady-state as follows:

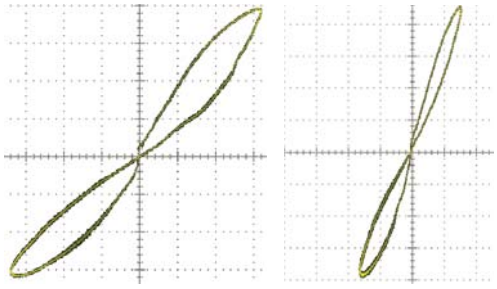
$$v(t) = (a + hi_0\omega^\alpha(sin(\omega t - \frac{\alpha\pi}{2})))i(t) + \frac{1}{C}q_\beta(t), \quad (10)$$

IV. The Simulation and Experimental Results

To validate the performance of the proposed emulator, the PSPICE simulations and experimental results are introduced in this section. The RC approximation proposed in [20] is employed to synthesize the fractional-order capacitor's behavior. The proposed emulator is implemented employing AD844 and AD633 with sinusoidal voltage input. The fractional-order current-controlled memristor presented in Fig.2 is simulated at different orders with parameters $R_1 = 2k\Omega$, $R_2 = 1k\Omega$, and $C_1 = 10nF$. The pinched hysteresis loop of the I-V plane is introduced in Fig.8 at $\alpha = 0.8$ with different frequencies



(a)



(b) (c)

Fig. 11. (a) The experimental connection of the memristor, the input current and voltage results at (b) $f = 4kHz$ (c) $f = 10kHz$.

where the hysteresis loop isn't symmetric and declined with increasing operating frequency. The Monte Carlo results are performed at $f = 500Hz$ for 100 runs, where the pinched hysteresis loop area changes with changing the value of R_1 as depicted in Fig.9. Employing the same parameters of the memristor, the series connection of FOC, and the fractional-order memristor is simulated in Fig.10. The pinched point location and the hysteresis loop area change as the frequency changes.

The fractional-order memristor circuit is validated experimentally where the experimental set-up is introduced in Fig.11(a), where the values of parameters are the same values used in the PSPICE simulations. The I-V plane at $f = 4kHz$ and $f = 10kHz$ are depicted in Figs.11(b) and (c) where the pinched hysteresis loop is decreased with increasing the frequency.

V. Conclusion

A current-controlled fractional-order memristor emulator was introduced using one active block. The series connection of a fractional-order element with a memristive element increased the controllability of the memristor/inverse memristor characteristics such as the pinched hysteresis loop area, the location of the pinched point, and the range of frequency. The numerical simulations were investigated with different α and frequency. PSPICE simulation and experimental results were performed to validate the proposed emulator. In the future, the series and parallel connections of fractional-order elements and memelements (meminductor and memcapacitor) will be discussed and employed in different applications.

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