# Fractional-order Memristor Emulator with Multiple Pinched Points

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***Abstract*—The paper proposes voltage-controlled first- and second-order memristor emulators. The emulators are designed using an operational-transconductance amplifier (OTA) and voltage multiplier blocks plus a fractional-order capacitor. The presented second-order emulator provides two pinched points controlled by order of the employed fractional-order capacitor. Numerical and PSPICE simulation results using AD844 and AD633 are introduced for different cases to validate the theoretical findings. The experimental verification is presented, showing the design flexibility and controllability based on the fractional-order parameters.**

***Keywords*—Memristor, OTA, Fractional-order circuits FOC, Pinched hysteresis.**

## I. Introduction

Memristor was theoretically postulated by L. Chua for the first time in 1971 [1]. It exhibits a constitutive non-linear relation between flux ($\varphi$) and charge ($q$). The memristor remained a theoretical concept until the HP team announced a physical model that approximates the performance of the memristor [2]. The memristor is employed in many applications such as neuromorphic hardware [3], relaxation oscillators [4], [5], and logic circuits [6].

The memristor is missing commercially as a two-terminal device. That's why different circuits have been proposed in the literature to realize its behavior employing commercial active and passive elements [7], [8]. In [9], a grounded memristor emulator was proposed using ten differential voltage current conveyor (DVCC) with six passive components. Based on the non-linear resistor, the adder and subtractor blocks were employed to realize the memristor circuit in [10]. The memristor emulator based on a two-second generation current conveyor (CCII) and an analog multiplier was introduced in [11]. In [12], a memristor emulator composed of three current feedback operational amplifiers (CFOA), six passive elements, and one diode was proposed. A tunable memristor emulator was presented in [13] using OTA plus two passive elements. Additionally, many researchers seek to associate the fractional calculus (FC) with memristive systems in several applications [14], [15].

FC studies the real-order integrals, and derivatives operators [16]. It can provide a further compact, and practical characterization of real-time physical systems [16]. To gain advantages of the fractional system; the multiple pinched points in the current versus voltage curve were observed in the charge-controlled memristor model, proposed in [17]. The conditions to realize multiple pinched points were discussed and applied to the fractional-order voltage-controlled memristor emulator in [7].

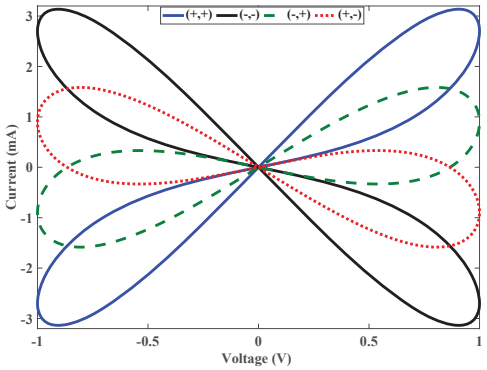



Fig. 1. The hysteresis loop at different polarities.

This paper suggests a voltage-controlled fractional-order memristor emulator. The introduced emulator employs two OTA blocks, one voltage multiplier plus fractional-order capacitor. By adding another voltage multiplier, the second-order memristor is achieved, providing two pinched points. Moreover, the employment of the FOC adds controllability to the pinched double-loop area and the range of frequency of the memristor.

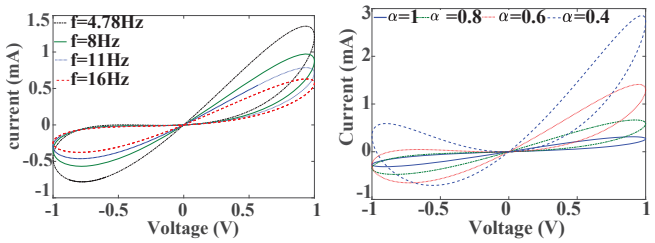
This paper is organized as follows: Section II discusses the theoretical simulations for the first- and second-order memristor model in the fractional-order domain. Section III introduces the proposed memristor emulator and its implementation to achieve multiple pinched points. The PSPICE simulations using commercial elements (AD844 and AD633) and experimental results are presented in section IV. Finally, the conclusion of the work is depicted in section V.

## II. The Memristor model in Fractional Domain

Recently, a general mathematical model of the first-order fractional-order memristor is characterized as follows [18]:

$$w(t) = \left( \pm b \pm k J_t^{\alpha} z(t) \right) z(t), \tag{1}$$

where $J_t^{\alpha}$ is the fractional integral operator, $\alpha$ is an arbitrary number $\in [0, 1]$. $z(t)$ and $w(t)$ are the normalized input and output signal, respectively, $b$ is the initial value, and $k$ is a




(a) (b)

Fig. 2. Numerical simulations of memductance for $b = 90\mu\Omega$ and $k = 9mA^{-1}s^{-\alpha}$ at (a) $\alpha = 0.7$, and (b) different orders at $f = 0.16Hz$.

scaling constant. The $(+,+),(+,-)$ and $(-,-),(-,+)$ mean the positively and negatively inclined loop as shown in Fig.1, respectively. When $z(t)$ and $w(t)$ are defined by a current and a voltage, the result is a current-controlled memristor. Whereas the memristor is voltage-controlled at $w(t)$ is characterized by a current, and $x(t)$ is represented by a voltage. The memductance and memristance are linearly proportional to the fractional accumulated voltage and current, respectively. One of the main characteristics of the memristor is the hysteresis loop in the $I-V$ plane, which decreases with increasing the applied frequency, as depicted in Fig. 2(a). Also, the hysteresis loop of the memristor is introduced in Fig.2(b) at different values of $\alpha$ where the hysteresis loops are symmetric at $\alpha = 1$ and asymmetric for $\alpha < 1$.

The main characteristic of the second-order fractional-order memristor is exhibiting a hysteresis behavior with two pinched points in the $I-V$ plane. The second-order voltage-controlled fractional-order memristor was firstly proposed in [7] which exhibit triple loops with two Pinched-off Points (PP). The memristor's conductance is defined as follows:

$$G_M(J^\alpha v(t)) = a + bJ^\alpha v(t) + h(J^\alpha v(t))^2, \tag{2}$$

where triple loops with two PPs are achieved. The pinched hysteresis loops for the second-order memristor is introduced in Fig.3(a) at order $\alpha = 0.3$, where the hysteresis area declines with the operating frequency. In addition, the influence of changing values of $\alpha$ is presented in Fig.3(b) where the second PP position moves in the negative direction until it disappears as $\alpha$ increments.

## III. The Proposed Emulator Circuit

The implementation of the voltage-controlled emulator is presented in Fig. 4(a) using two OTAs blocks and one multiplier. The direct analysis of Fig. 4(a) reveals that the input current is defined as follows:

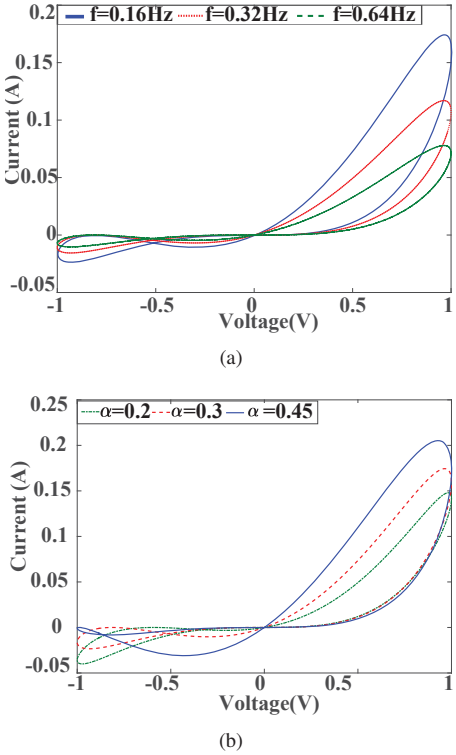
$$I_{in}(t) = g_{m0}(v_{in} - v_m), \tag{3}$$

where $v_{in}$ is the applied voltage and $v_m$ is the multiplier output voltage defined by:

$$v_m = \pm d g_{m1} \frac{\varphi_\alpha(t)}{C} v_{in}(t), \tag{4}$$

where $d$ represents the voltage multiplier gain and $\varphi_\alpha$ represents the fractional integral of the input voltage. The memductance is thus given by:

$$G_m = g_{m0} \mp d g_{m0} g_{m1} \frac{\varphi_\alpha(t)}{C}, \tag{5}$$




(a)

(b)

Fig. 3. Numerical simulations of the second-order fractional-order memristor for $a = 11k\Omega$, $b = 111\Omega^{-1}A^{-1}s^{-\alpha}$, and $c = 11\Omega^{-1}A^{-2}s^{-2\alpha}$ at (a) $\alpha = 0.3$, and (b) different orders at $f = 0.16Hz$

where the positive/negative means incremental/decremental memductor, respectively. Based on the proposed emulator, the second-order fractional-order memductance is presented in Fig.4(b). The second multiplier output and memductance can be written as follows:

$$v_m = d\left(g_{m1}\frac{\varphi_\alpha(t)}{C} + d(g_{m1}\frac{\varphi_\alpha(t)}{C})^2\right)v_{in}(t), \tag{6a}$$

$$G_m = g_{m0} + dg_{m0}\left(g_{m1}\frac{\varphi_\alpha(t)}{C} + d(g_{m1}\frac{\varphi_\alpha(t)}{C})^2\right), \tag{6b}$$

where $a = g_{m0}$, $b = \frac{dg_{m0}g_{m1}}{C}$, and $h = \frac{dg_{m0}g_{m1}^2}{C^2}$ based on Eqn.2. By applying a sinusoidal current $v_{in}(t) = v_0 sin(\omega t)$, the steady-state fractional integration of the sinusoidal voltage can be written as $J^\alpha(v_0 sin(\omega t))|_{s.st} = v_0\omega^{-\alpha}(sin(\omega t - \frac{\alpha\pi}{2}) + sin(\frac{\alpha\pi}{2}))$ [7]. The memristance at steady-state can be defined as follows:

$$G_M(J^\alpha v(t)) = a + bv_0\omega^{-\alpha}\left(sin(\omega t - \frac{\alpha\pi}{2}) + sin(\frac{\alpha\pi}{2})\right) + hv_0^2\omega^{-2\alpha}\left(sin(\omega t - \frac{\alpha\pi}{2}) + sin(\frac{\alpha\pi}{2})\right)^2. \tag{7}$$

Based on the procedure in [7], the coordinate point $(x_p, y_p)$ is calculated by equating the coefficient of $cos(\omega t)$ in Eqn.7 with zero and putting $x_p = v_0 sin(\omega t)$. The $y_p$ value is $y_p = x_p/R_M$. The coordinates of the first PP are $(0,0)$ and the other

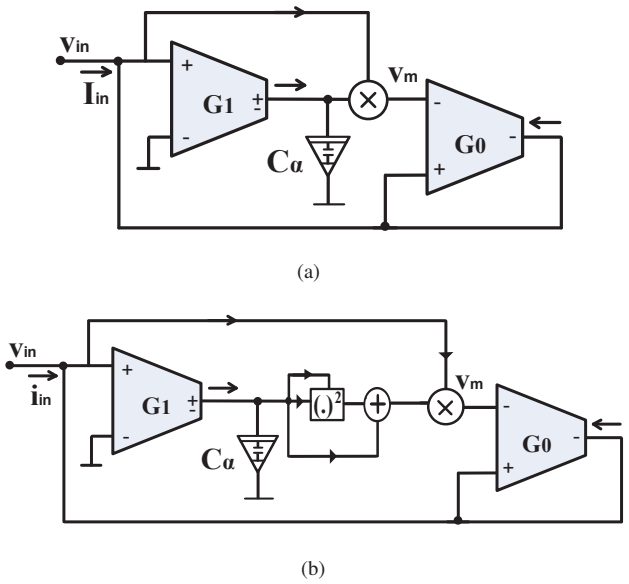



Fig. 4. The proposed voltage-controlled emulator (a) first-orderand (b) second-order.

PP can be written as follows [7]:

$$x_p = -\frac{b\omega^{\alpha} + 2hv_0 sin(\frac{\alpha\pi}{2})}{2hcos(\frac{\alpha\pi}{2})}, \tag{8a}$$

$$y_p = x_p/y, \tag{8b}$$

where

$$y = a + \frac{b}{\omega^{\alpha}}\left(x_p cos(\frac{\alpha\pi}{2}) + v_0 sin(\frac{\alpha\pi}{2})\right) + \frac{h}{\omega^{2\alpha}}\left(x_p^2 cos^2(\frac{\alpha\pi}{2}) + sin^2(\frac{\alpha\pi}{2})(2v_0^2 - x_p^2) + v_0 x_p sin(\alpha\pi)\right). \tag{9}$$

It is worth to mention that with increasing $\alpha$, the pinch-off point moves towards the origin as depicted in Fig.3(b). To obtain another pinched point, the condition $|x_p| < v_0$ must be satisfied which constrains the operating frequency to $\omega < \left(\frac{\sqrt{8}hv_0 sin(\frac{(2\alpha+1)\pi}{4})}{b}\right)^{1/\alpha}$.

## IV. Simulation and Experimental Results

PSPICE simulations and experimental results are investigated to validate the proposed emulator's performance. The RC approximation proposed in [19] is employed to synthesize the fractional-order capacitor's behavior. The proposed emulators are implemented using commercially active devices; two AD844 as OTA and AD633 as an analog multiplier.

The first-order decremental fractional-order memristor using AD844 and AD633 is presented in Fig. 5 where the paramters values are $C = 10nF/sec^{1-\alpha}$, $R_{m1} = 1k\Omega$, and $R_{m0} = 10k\Omega$. The simulation results of the proposed emulator in Fig. 4(a) is depicted in Fig.6 where the hysteresis loop area is decreased with increasing the applied frequency.

By adding another AD633, the connection of second-order FO memristor circuit is implemented in Fig. 5 with $R_0 = 10k\Omega$, $R_1 = 80k\Omega$, and $C = 10nF/sec^{1-\alpha}$. Figure 7 (a) presents the second-order FO memristor at order $\alpha = 0.3$ with different frequencies providing another PP. Clearly, the second PP moves as the order $\alpha$ changes as presented in Fig.7(b).

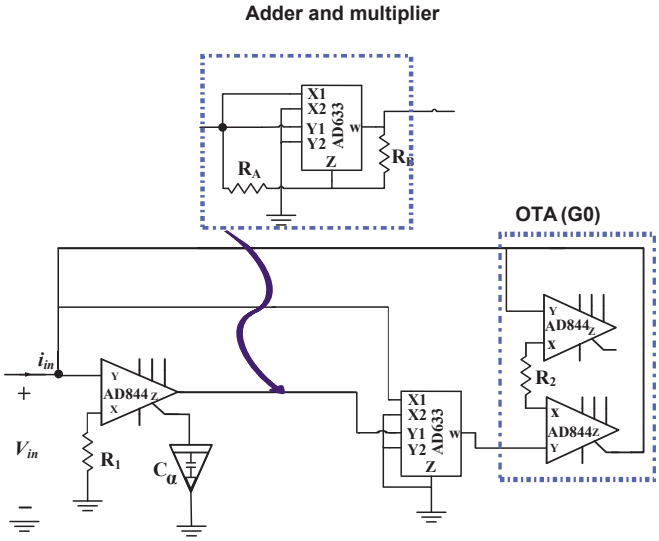



Fig. 5. The First/ second-order emulator using off-shelf components.

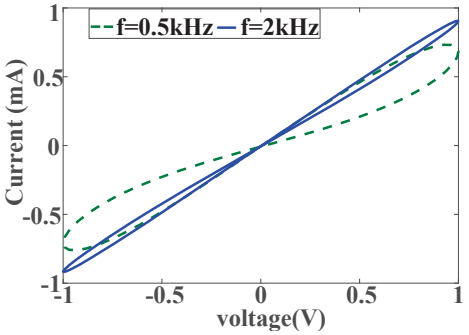



Fig. 6. The simulation results of decremental first-order memristor.

The second-order memristor is verified experimentally as depicted in Fig.8(a). The results at different frequencies are presented in Fig.8(b) and (c) where the hysteresis area decreases with increasing the applied frequency given two pinched points.

## V. Conclusion

Employing the memristor's mathematical model in the fractional-order domain, the first- and second-order voltage-controlled emulators were presented. The proposed emulators were designed using the OTA block, which made the emulator tunable and increased the pinched hysteresis area's controllability. The numerical simulations were investigated in different cases, presenting two pinched points in the $I-V$ plane for the second-order emulator. PSPICE simulation and experimental results were performed to validate the presented emulators.

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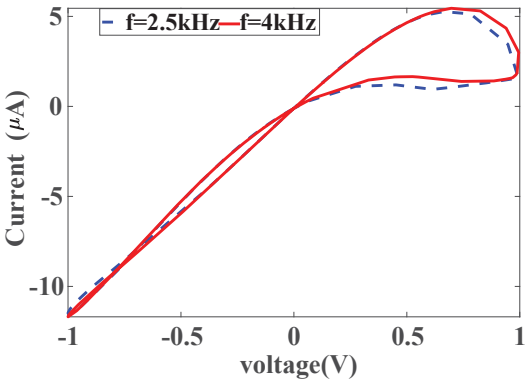
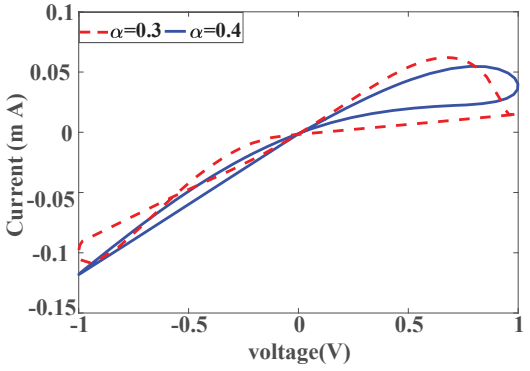
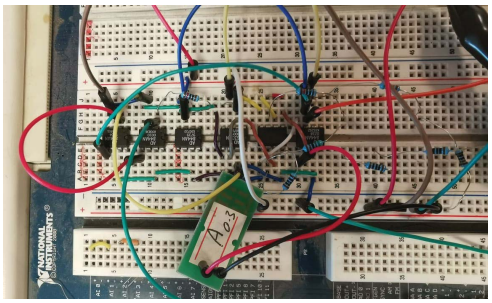



(a)

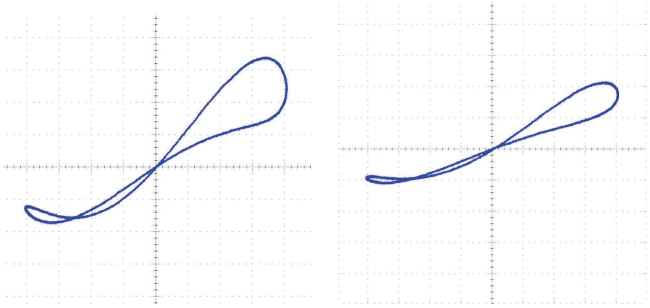



(b)

Fig. 7. The PSPICE simulation results of the second-order memristor at different (a) frequencies and (b) orders $\alpha$.



(a)



(b) (c)

Fig. 8. The experimental results of the second-order memristor (a) the circuit connections at different frequencies (b) $f = 2.5kHz$, and (c) $f = 10kHz$.

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