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Novel CMOS Linearised Balanced Output Transconductance Amplifier Based on Differential Pairs

Ein neuer linearisierter Differentialverstärker für CMOS Technologie mit symmetrischem Ausgangsübertragungsleitwert

Abstract
Time continuous filter circuits using Gm-C or MOSFET-C structures are being reported frequently for various applications [1–9]. The main issue is dynamic range because of the confined signal level handling capability of the basic differential pair. A linear transconductor circuit is presented using the MOS transistor square law characteristic. It is shown that the proposed transconductor offers high linearity and wide range compared with ordinary long tail differential pair transconductors (LTP). PSpice simulation results are given.

Übersicht
Zeitkontinuierliche Filterschaltungen mit Gm-C oder MOSFET-C Strukturen werden in der Literatur häufig für verschiedene Anwendungen [1–9] beschrieben. Schwerpunkt der Untersuchungen ist der Dynamikbereich, gegeben durch den begrenzten Signalpegel, den die Grundschaltung eines differentialen Transistorpaares bewältigen kann. Die Arbeit stellt einen linearen Schaltkeis für einen Übertragungsleitwert vor, der die quadratische Kennlinie eines MOS-Transistors nutzt. Mit PSpice-Simulationen wird gezeigt, daß der vorgeschlagene Schaltkreis im Vergleich zu üblichen Schaltungen mit einer Stromquelle im gemeinsamen Emitterzweig (LTP, Long Tail Pair) eine hohe Linearität über einen weiten Bereich bietet.

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Für die Dokumentation
Übertragungsleitwert / CMOS-Realisierung

1. Introduction

Most of the reported G_m-C structures linearise a differential pair by source/emitter degeneration or by multiple pair structures [2-9]. Some use the transistor square law characteristics.

The square law CMOS model is given by

$$I = \frac{K_n}{2}\left(V_{GS} - V_T\right)^2, \tag{1}$$

$$K_n = \left(\mu_n C_{OX}\right)\left(\frac{W}{L}\right), \tag{2}$$

where K_n is the transconductance parameter, V_T the threshold voltage, μ_n the effective carrier mobility, C_{OX} the gate oxide capacitance per unit area, W the channel width and L the channel length.

Consider the circuit shown in **Fig. 1**. Assuming that all body terminals are connected to the proper supply voltages. The currents I_1 and I_2, respectively, are given by

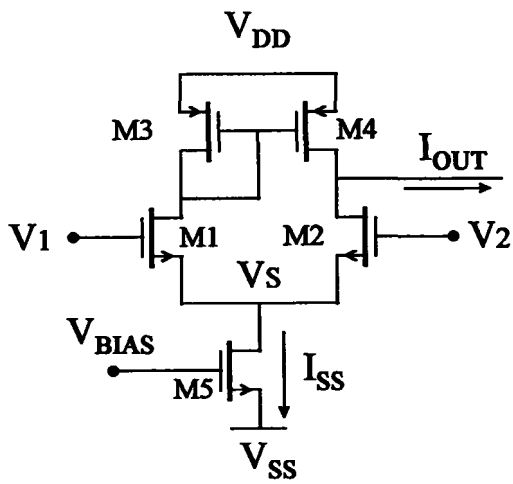

Fig. 1: The ordinary long tail differential pair CMOS transconductor

$$I_1 = \frac{K_n}{2}\left(V_1 - V_S - V_T\right)^2, \tag{3}$$

$$I_2 = \frac{K_n}{2}\left(V_2 - V_S - V_T\right)^2. \tag{4}$$

The current I_{SS} is given by

$$I_{SS} = \frac{K_n}{2}\left(V_1 - V_S - V_T\right)^2 + \frac{K_n}{2}\left(V_2 - V_S - V_T\right)^2, \tag{5}$$

and the output current is

$$I_{OUT} = I_1 - I_2 = \frac{K_n}{2}\left(V_1 - V_2\right)\left(V_1 + V_2 - 2\left(V_S + V_T\right)\right). \tag{6}$$

This simple differential pair would have a perfectly linear characteristic if V_S tracks the common mode input voltage. But in a CMOS differential pair the common source node voltage increases and decreases as the differential input is driven over the full range ending when one of the transistors is running at full tail current and the other one is off [1].

The output current as a function of the two input voltages V_1 and V_2 and the current tail I_{SS} is obtained as

$$I_{OUT} = \sqrt{K_n I_{SS}}\left(V_1 - V_2\right)\sqrt{1 - \frac{K_n\left(V_1 - V_2\right)^2}{4I_{SS}}}. \tag{7}$$

Therefore, the differential input voltage range $V_i = V_1 - V_2$ corresponds to

$$-\sqrt{\frac{2I_{SS}}{K_n}} \le V_i \le \sqrt{\frac{2I_{SS}}{K_n}}. \tag{8}$$

From (7) and (8) it is seen that the linearity range of the transconductor increases as the ratio (I_{SS}/K_n) increases.

One major problem is the effect on the common mode input voltage which limits the operating range of the circuit. Setting $V_1 - V_2 = V_{CM}$, the current in each of the differential pair branches is given by

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$$\frac{K_n}{2}\left(V_{CM}-V_S-V_T\right)^2=\frac{1}{2}I_{SS}, \tag{9}$$

$$V_{CM\,min}=V_{S\,min}+V_T+\sqrt{\frac{I_{SS}}{K_n}}. \tag{10}$$

For the Long Tail differential Pair (LTP) the following condition must be valid to operate properly:

$$V_{S\,min}+V_T \geq V_{BIAS}. \tag{11}$$

Hence:

$$V_{CM} \geq V_{BIAS}+\sqrt{\frac{I_{SS}}{K_n}}. \tag{12}$$

From (12), it is seen that as the ratio (I_{SS}/K_n) increases V_{CM} increases; hence the common mode range of operation decreases. The compromise between the degree of linearity and the range of operation limits the performance of the transconductor.

To linearise the differential pair, V_S was clamped to a fixed DC level tracking the common mode (CM) voltage of V_1 and V_2. This was easily done by means of an amplifier as in **Fig. 2** [1].

As V_S shifts upwards under the differential drive condition, the amplifier A will increase the differential pair tail current I_{ss} to pull V_s down to the reference level again as far as the loop gain is capable and for as long as the loop bandwidth is sufficient to follow the V_1 - V_2 signal frequency. By applying the amplifier control loop presented in [1], the linearised transconductance G_m is given by:

$$G_m = D\left(V_{CONTROL}-V_T\right) \tag{13}$$

where D is a constant and $V_{CONTROL}$ is a control voltage.

Although the circuit seems to satisfy the requirements, it uses excessive hardware due to the usage of a high gain amplifier and the use of resistors which are unavailable in ordinary CMOS technology. In addition, the circuit suffers from body effect. In this paper, a linearised CMOS transconductance amplifier totally free of body effect is presented.

2. Transconductor circuit description

The main idea is to clamp V_S to a certain DC level tracking the common mode voltage of V_1 and V_2. In this case, the current tail

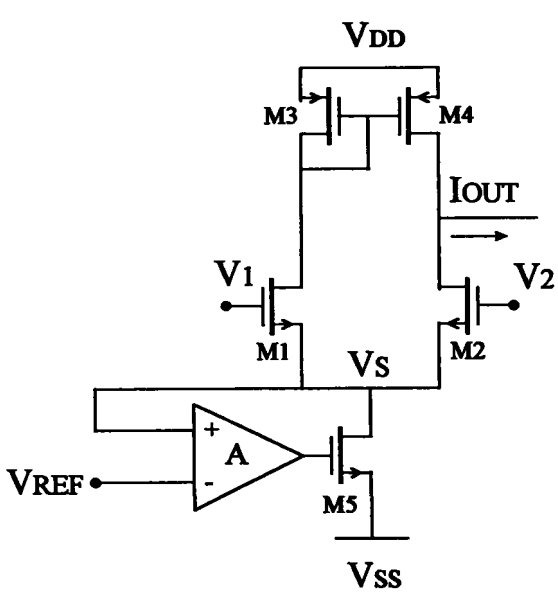

Fig. 2: The linearised long tail differential pair CMOS transconductor using an high gain amplifier

I_{SS} represents a degree of freedom that changes by feedback action in order to stabilize the value of the voltage V_S.

The proposed transconductor is composed of two blocks: the LDP (linearised differential pair) and the CMC (common mode compensator) as shown in **Figs. 3-a** and **3-b**, respectively. The two blocks are interconnected as shown in **Fig. 3-c** to obtain the complete linearised transconductor. The circuit schematics of LDP and CMC are shown in **Figs. 4-a** and **4-b** respectively.

First, consider the circuit shown in Fig.4-a, M1 and M2 form the main differential pair of the transconductor. M3 and M4 drive an equal current of half the sum of I_1 and I_2 into the drains of M1 and M2 in order to obtain a balanced output current I_{out}. M5 is responsible for fixing the voltage V_S to a constant DC value. The transistors M6–M9 perform the feedback action necessary to bias the current tail transistor M10.

All the transistors used are operating in the saturation region (neglecting the channel length modulation effect). Assuming that all body terminals are connected to the proper supply voltages.

The output current I_{OUT} is given

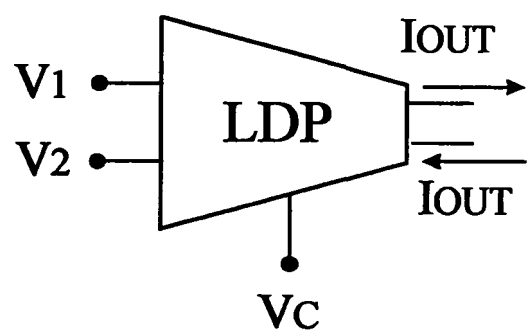

Fig. 3-a: The building block of the LDP

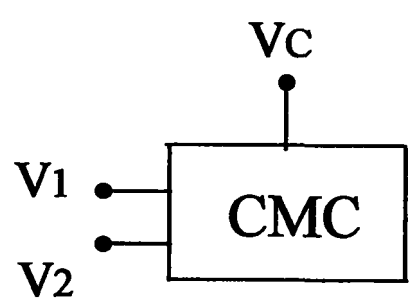

Fig. 3-b: The building block of the CMC

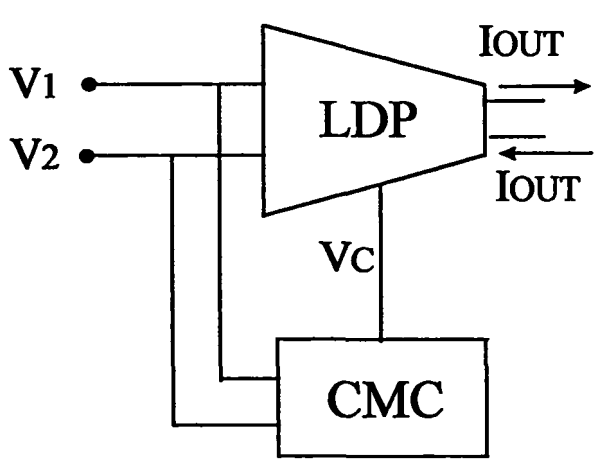

Fig. 3-c: The complete BOTA obtained by interconnecting the LDP and the CMC

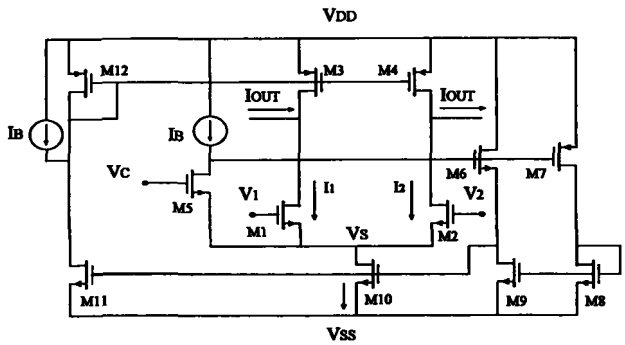

Fig. 4-a: The circuit schematic of the LDP

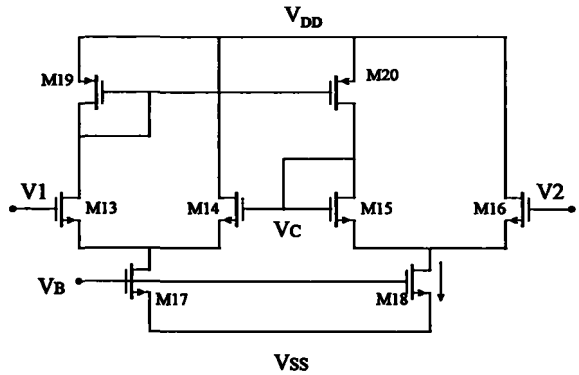

Fig. 4-b: The circuit schematic of the CMC

$$I_{OUT} = I_1 - \frac{1}{2}(I_1 + I_2). \tag{14}$$

Hence, one obtains two opposite replicas of the output current which is given by

$$I_{OUT} = \frac{1}{2}(I_1 - I_2). \tag{15}$$

By substituting for I_1 and I_2 in (15), the output current is

$$I_{OUT} = \frac{1}{2}\left(\frac{K_n}{2}(V_1 - V_S - V_T)^2 - \frac{K_n}{2}(V_2 - V_S - V_T)^2\right). \tag{16}$$

Using the square law identity, one obtains

$$I_{OUT} = \frac{K_n}{2}(V_1 - V_2)\left(\frac{V_1 + V_2}{2} V_S - V_T\right). \tag{17}$$

In addition, the current I_B flowing in transistor M5 is

$$I_B = \frac{K_{n1}}{2}(V_C - V_S - V_T)^2. \tag{18}$$

Hence, from (18), the voltage V_S is given by

$$V_S = V_C - V_T - \sqrt{\frac{2I_B}{K_{n1}}}. \tag{19}$$

Substituting for V_S in (17), one obtains

$$I_{OUT} = \frac{K_n}{2}(V_1 - V_2)\left(\frac{V_1 + V_2}{2} - \left(V_C - V_T - \sqrt{\frac{2I_B}{K_{n1}}}\right) - V_T\right). \tag{20}$$

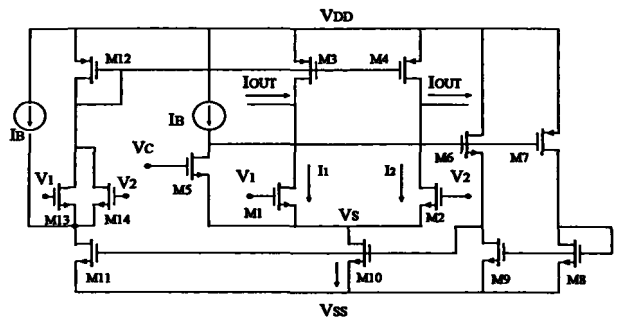

Fig. 5-a: The circuit schematic of the low voltage LDP

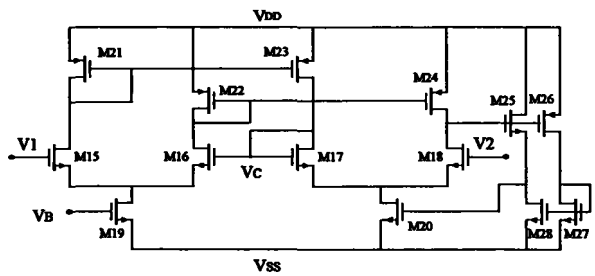

Fig. 5-b: The circuit schematic of the low voltage CMC

In order to obtain a linear transconductance circuit, the voltage V_c should be adjusted to

$$V_C = \frac{V_1 + V_2}{2}. \tag{21}$$

This is realized using the CMC circuit which is shown in Fig. 4-b. Assuming that the differential pairs M13-M14 and M15-M16 are matched, they carry the same differential voltage since they have the same current tail as well as the same currents in differential pair branches. Therefore,

$$V_1 - V_C = V_C - V_2, \tag{22}$$

which results in (21). For low voltage operation, the LDP can be modified as shown in **Fig. 5-a**. The transistors M13 and M14 are added in order to obtain proper outputs even if the transistor M10 is pushed in the ohmic region. Similarly, the CMC circuit is modified as shown in **Fig. 5b**. The two differential pairs are driven by the same currents even if the current tail transistor M19 enters the ohmic region. Transistors M23-M26 perform the feedback action necessary to ensure equal current tails for both differential pairs. In this case, the input voltage common mode region for the CMC circuit is significantly increased (since the operation is still proper, even if the current tail transistor enters the ohmic region) allowing the extension of the input voltage differential mode region by Increasing the current tail value.

By substituting for V_C in (20), the output current is finally given by

$$I_{OUT} = \frac{K_n}{2}\sqrt{\frac{2I_B}{K_{n1}}}(V_1 - V_2). \tag{23}$$

Thus the resulting circuit is a current controlled linearised transconductance amplifier. The current I_B can be used to control the value of the transconductance to appropriate values which is very useful in the design of accurate Gm-C filters.

By choosing $K_{n1} = K_n$, the output current is

$$I_{OUT} = \sqrt{\frac{K_n I_B}{2}}\left(V_1 - V_2\right). \qquad (24)$$

When comparing eqs. (7) and (24), it is noted that the resulting Balanced Output Transconductor Amplifier (BOTA) gives an output current totally free of nonlinearity terms and without limitation on the input voltage differential mode range. In addition, it has other advantages of the LTP such as immunity from body effect and simplicity in use, which gives the proposed BOTA the flexibility to replace the LTP in many applications.

3. PSpice simulations

PSpice simulations for both, the long tail differential pair and the proposed current controlled linearised BOTA, were carried out with the transistors aspect ratios as given in **Tables 1** and **2** respectively, and with ±1.5 V supply voltages and 0.7 μm Mietic CMOS process.,

Fig. 6 represents the I-V characteristics of the long tail differential pair. V_1 is scanned from −1 V to 1 V keeping V_2 at 0 V.

Fig. 7 represents the I-V characteristics of the linearised balanced output transconductance amplifier. V_1 is scanned from −1 V to 1 V for different control current values keeping V_2 at 0 V.

Table 1: Transistor aspect ratios for PSpice simulations

Transistor	Aspect Ratio
M1–M2, M5, M13, M14	1.4/1.4
M3, M4	35/3.5
M12	70/3.5
M6	1.4/1.4
M7	14/1.4
M8	1.4/1.4
M9	3.5/1.4
M10, M11	35/1.4

Table 2: Transistor aspect ratios for PSpice simulations

Transistor	Aspect Ratio
M15–M17	7/1.4
M21–M24	35/3.5
M25	1.4/1.4
M26	14/1.4
M27	1.4/1.4
M28	3.5/1.4

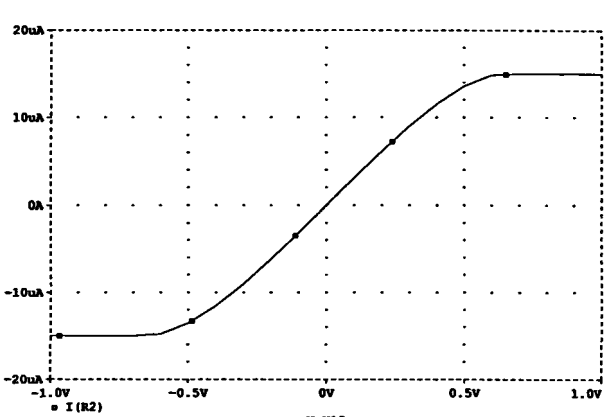

Fig. 6: The *I-V* characteristics of the ordinary long tail differential pair CMOS transconductor

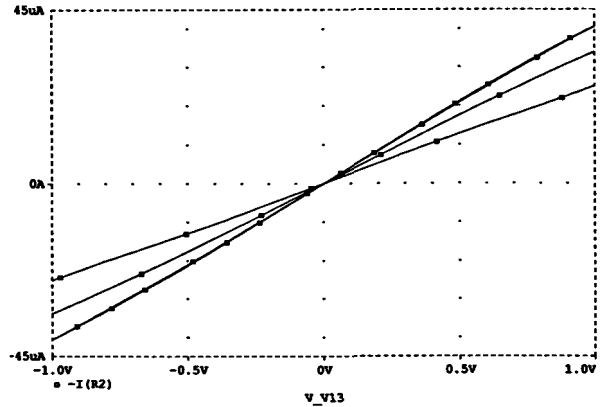

Fig.7: The *I-V* characteristics of the proposed linearized long tail differential pair CMOS transconductor

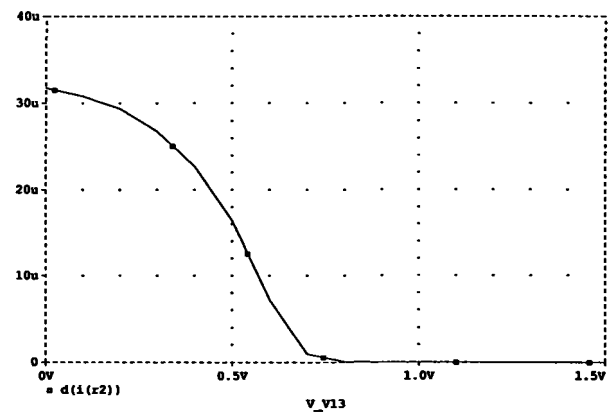

Fig.8: The transconductance Gm of the ordinary long tail differential pair CMOS transconductor versus differential input voltageV_i

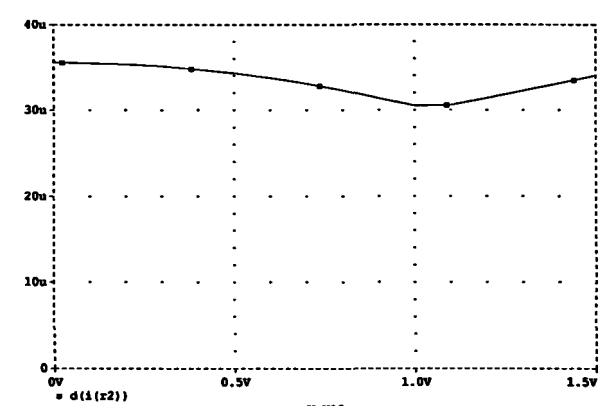

Fig. 9: The transconductance Gm of the proposed linearized long tail differential pair CMOS transconductor versus differential input voltage V_i.

The performance of the linearised balanced output transconductance amplifier is clearly demonstrated in **Fig. 8.** The transconductance of the long tail differential pair already 3 db down to 0.5 V differential peak input voltage, running on a 15 μA tail current. The linearised circuit performance in **Fig. 9** shows a 0.5 db error on the transconductance for V_i = 1.5V peak. Clearly this circuit is capable of handling 1 V peak-to-peak signal.

4. Conclusion

A linearisation technique is described that allows to extend the linear range of a CMOS differential pair up to 2 V peak using a 3 V power supply. The linearised BOTA is designed mainly for use in Gm-C filter applications.

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