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New CMOS fully differential difference transconductors and application to fully differential filters suitable for VLSI

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Abstract

New CMOS voltage controlled fully differential difference transconductors (FDDT) are presented. The basic structure of the proposed transconductors is based on the current linearization of basic MOS cells in different configurations consisting from two or four NMOS matched transistors operating in the saturation region. The proposed transconductors are used to design fully differential second order lowpass, bandpass and highpass filters suitable for VLSI. PSpice simulation results for the proposed fully differential difference transconductors and their filter applications indicating the linearity range and verifying the analytical results are also given.

Keywords: CMOS transconductors; Filters

1. Introduction

Linear transconductor circuits are useful building blocks in analog signal processing. Based on the transconductor elements, MOS-C filters and basic analog building blocks such as MOS resistors, multipliers and amplifiers or some other circuits can be built. The CMOS differential difference amplifier (DDA) and the differential difference operational floating amplifier (DDOFA) are basic building blocks yielding simple analog VLS1 circuits with low component count and are implemented by the combination of two differential transconductors or one differential difference transconductor and an output stage [1–5]. Several realizations for the CMOS transconductors have been introduced in the literature [6–15]. The realizations given in [6–9] are based on using a differential stage with MOS transistors operating in the saturation region with their sources connected to their substrates, where the drain current of an NMOS transistor operating in that region is given by:

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2 \quad (1)$$

$$\text{where } K = \mu_n C_{ox}\left(\frac{W}{L}\right) \quad (2)$$

μ_n is the electron mobility.
C_{ox} is the gate oxide capacitance per unit area.
W/L is the transistor aspect ratio.
V_T is the threshold voltage (assumed equal for all NMOS transistors).
V_{GS} is the gate to source voltage.

The CMOS transconductors given in [10, 12] are based on the use of MOS transistors operating in the non-saturation region. The use of both a differential stage and MOS transistors operating in the non-saturation region to realize CMOS transconductors are given in [13, 15]. The realization given in [15] provides a CMOS transconductor with a balanced output current based on the use of a wide input range diffierential CMOS transconductor in cascade with a voltage controlled MOS grounded resistor [16] and a balanced output transconductor stage.

In this paper, new CMOS voltage controlled fully differential difference transconductors (FDDT) are presented. Fully differential transconductor structures avoid the use of current mirror for current subtraction as in the single-ended transconductors by generating two output currents and effectively performing the subtraction by taking the output current across two nodes instead of at a single node referred to ground [17]. The structure of the proposed transconductors is based on the current linearization of basic MOS cells in different configurations consisting from two or four NMOS matched transistors operating in the saturation region. The paper indicates that there is a large number

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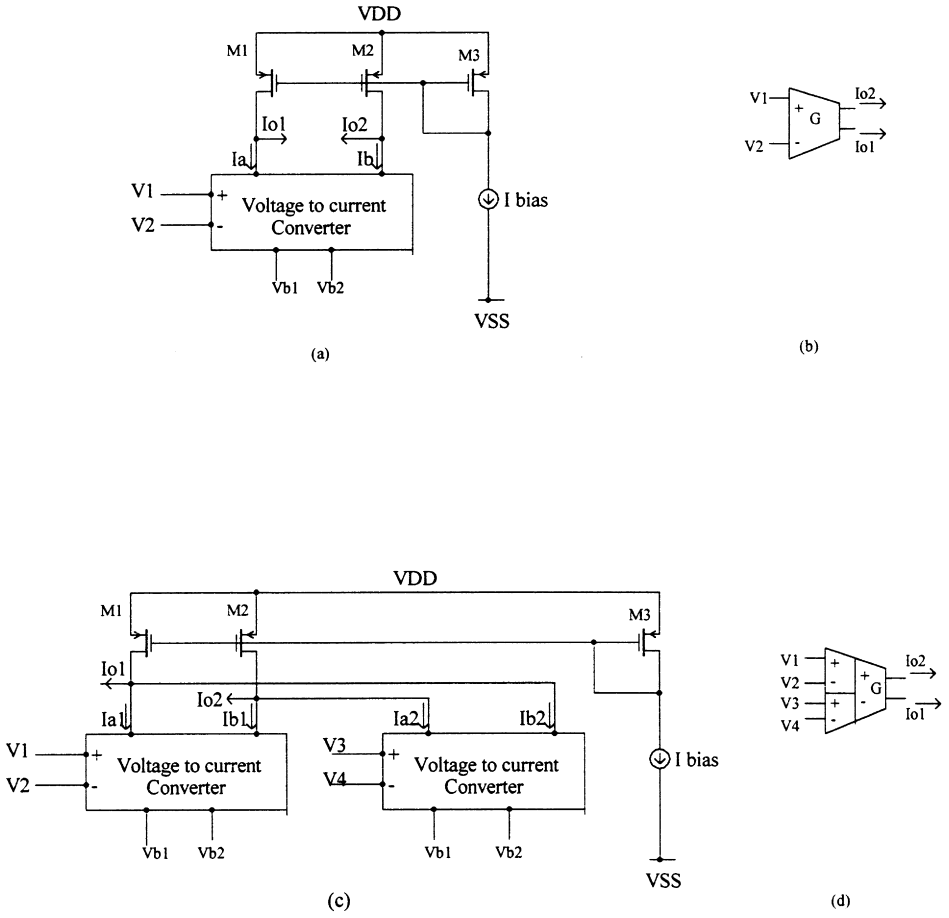


Fig. 1. (a) The basic structure of the fully differential transconductor. (b) The symbol of the fully differential transconductor. (c) The basic structure of the fully differential difference transconductor. (d) The symbol of the fully differential difference transconductor.

of CMOS transconductors depending on the configuration used and the biasing circuit used to linearize the differential current of the basic transistors.

The basic structure of the proposed fully differential transconductor and its symbols are shown in Fig. 1(a) and (b), in which the voltage to current converter (V–I) generates two output currents I_{o1} and I_{o2} where the output current I_o, is linearly proportional to the differential input voltage (V_1–V_2) such that:

$$I_o = I_{o2} - I_{o1} = I_a - I_b = G(V_1 - V_2) \tag{3}$$

where G is the equivalent transconductor which is controlled through one or two biasing control voltages V_{b1}, and V_{b2}. The structure of the fully differential difference transconductor and its symbol are shown in Fig. 1(c) and (d), where two voltage to current converters are used such that the output current I_o is given by:

$$I_o = G[(V_1 - V_2) - (V_3 - V_4)] \tag{4}$$

In Section 2 the realization of the CMOS differential difference transconductors based on the first configuration which consists of two matched NMOS transistors operating in the saturation region are presented. In Section 3 the CMOS differential difference transconductors based on the second configuration which consists of four matched transistors operating also in the saturation region connected in three different forms to represent the basic building block of the proposed transconductors are given. In Section 4, the proposed transconductors are used to design fully differential second order lowpass, bandpass and highpass filters. PSpice simulation results for the transconductor circuits indicating the linearity range and confirming the analytical results are also given.

2. The CMOS differential difference transconductors based on the first configuration

The realization of the CMOS fully differential transconductor based on the first configuration which consists of two matched transistors M1 and M2 as shown in Fig. 2(a), where the gates of the transistors are the input terminals of the voltage to current converter and the two sources represent the terminals which must be biased by biasing voltages such that the differential output current of the voltage to current converter is linear and proportional to the input differential

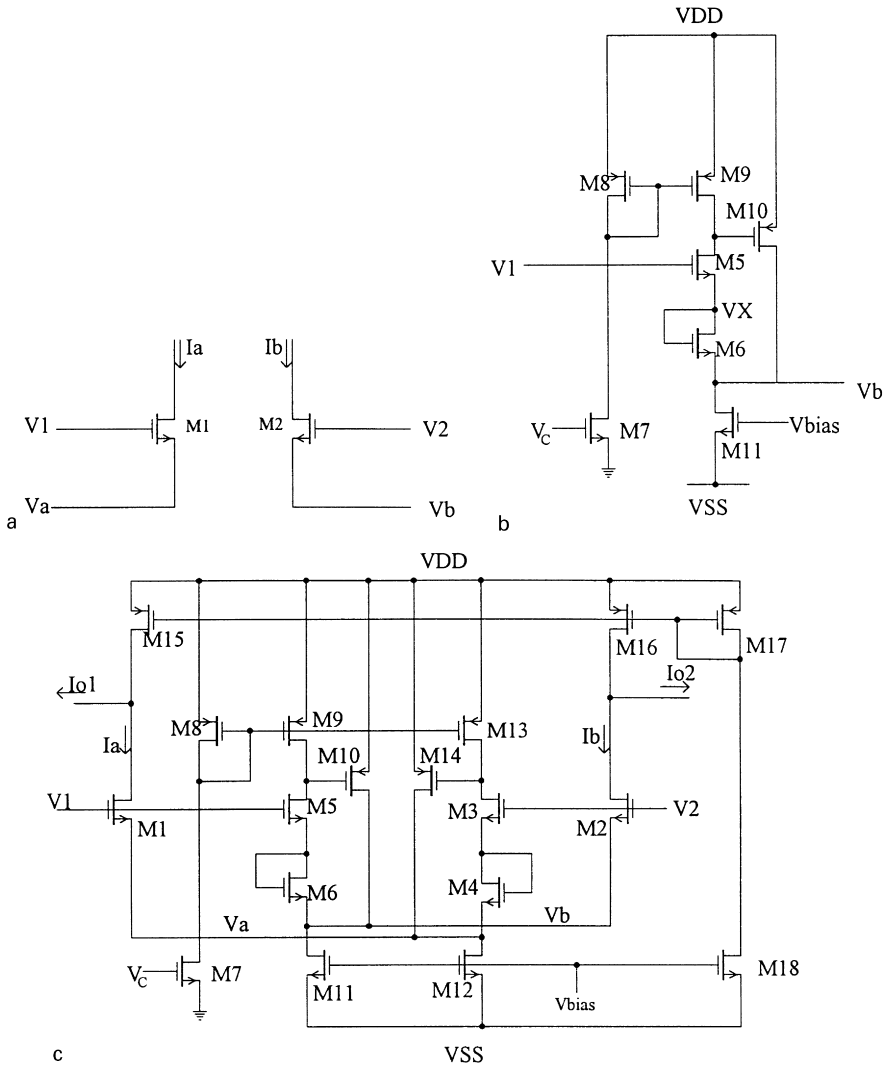


Fig. 2. (a) The basic cell of the first configuration. (b) The biasing circuit for the first proposed CMOS transconductor. (c) The first proposed fully differential CMOS transconductor.

voltage. The currents I_a and I_b are obtained using the square-law current equation and are given by:

$$I_a = \frac{K}{2}(V_1 - V_a - V_T)^2 \tag{5}$$

$$I_b = \frac{K}{2}(V_2 - V_b - V_T)^2 \tag{6}$$

Therefore the output current $I_o = I_a - I_b$ is given by:

$$I_o = \frac{K}{2}(V_1 + V_2 - V_a - V_b - 2V_T)(V_b - V_a + V_1 - V_2) \tag{7}$$

According to the previous equation, a linear relation between the output current I_o and $(V_1 - V_2)$ can be achieved if the following relations are satisfied:

$$V_b - V_a + V_1 - V_2 = 2m(V_1 - V_2) \tag{8}$$

$$V_1 + V_2 - V_a - V_b - 2V_T = 2E - 2V_C \tag{9}$$

where V_C is a control voltage used to control the transconductor of the proposed circuit and allows it to compensate for process parameter spreads in the transconductor value, m is a dimensionless constant and E is a constant voltage. From the previous two equations, the necessary biasing voltages V_a and V_b to achieve the linear relation between the output differential current and $(V_1 - V_2)$ are as follows:

$$V_a = (1 - m)V_1 + mV_2 + V_C - V_T - E \tag{10}$$

$$V_b = mV_1 + (1 - m)V_2 + V_C - V_T - E \tag{11}$$

Therefore the output current I_o is obtained as:

$$I_o = 2Km(E - V_C)(V_1 - V_2) \tag{12}$$

The equivalent transconductor G, which is given by the

output current I_o divided by the voltage difference $(V_1 - V_2)$ is expressed in terms of the dc biasing voltages E, V_C and the transistor transconductor parameter K as follows:

$$G = 2Km(E - V_C) \tag{13}$$

Therefore, a linear differential transconductor that is tuned by the voltage V_C is obtained. From the previous equations, it is clear that a large number of differential CMOS transconductors can be obtained corresponding to each value of m, E and K. These values are the design parameters of the biasing circuit used to bias the sources of the basic transistors.

2.1. The first proposed transconductor circuit based on the first configuration

For example for $m = 1$ and $E = 2V_C$, the biasing voltages V_a and V_b are given by:

$$V_a = V_2 - V_C - V_T \tag{14}$$

$$V_b = V_1 - V_C - V_T \tag{15}$$

This can be achieved by using the MOS circuit shown in Fig. 2(b). The currents of the transistors M5, M6 and M7 are equal (assuming the transistors M8 and M9 are matched) and are given, respectively, by:

$$I_5 = \frac{K_5}{2}(V_1 - V_X - V_T)^2 \tag{16}$$

Table 1
Transistor aspect ratios of the CMOS transconductor of Fig. 2(c)

MOS transistor	Aspect ratio (W μm/L μm)
M1–M2	4/16
M3–M5	4/4
M7	16/4
M8–M14	12/4
M15–M18	30/4

$$I_6 = \frac{K_6}{2}(V_X - V_b - V_T)^2 \tag{17}$$

$$I_7 = \frac{K_7}{2}(V_C - V_T)^2 \tag{18}$$

From the previous equations and with $K_5 = K_6 = 4K_7$, the desirable voltage V_b as given by Eq. (15) is obtained.

The transistor M10 together with the biasing transistor M11 form a negative feedback action which provides the necessary current from the output without changing the voltage. Similarly, the biasing voltage V_a, can be obtained using similar CMOS circuit to that shown in Fig. 2(b). Therefore, the transconductor G is given by:

$$G = 2KV_C \tag{19}$$

which can be tuned by the control voltage V_C. The overall CMOS differential transconductor circuit is shown in Fig. 2(c).

PSpice simulation results using a standard 2μm technology file for this proposed transconductor were carried out with the transistor aspect ratios as given in Table 1 and with the supply voltages equal to ±2.5 V. Fig. 3(a) represents

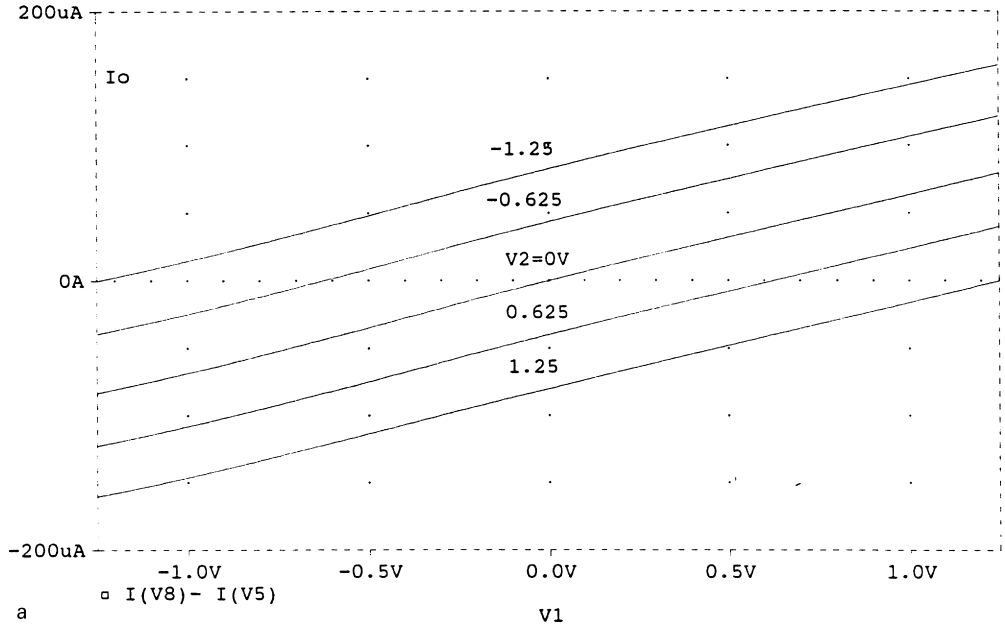


Fig. 3. (a) The I–V characteristics of the first proposed CMOS transconductor. (b) The magnitude and phase responses of the first transconductor. (c) The output-referred and input-referred noise voltage spectral densities for the first transconductor when terminated by 1 KΩ. (d) The first proposed fully differential difference transconductor.

the I–V characteristics of the first proposed transconductor with the control voltage $V_C = 1.4$ V, V_1 and V_2 scanned from -1.25 V to 1.25 V. The magnitude and phase responses of the transconductor differential output current are shown in Fig. 3(b). PSpice results in the output-referred and input-referred noise voltage spectral densities for the first proposed transconductor when terminated by 1 KΩ is shown in Fig. 3(c). The Total Harmonic Distortion (THD) is less than 0.25% for 100 KHz, 1 V peak-to-peak sinusoidal input. The mismatches between the basic MOS transistors M1 and M2 produce harmonic distortion and offset of the transfer curve therefore the input range for the same

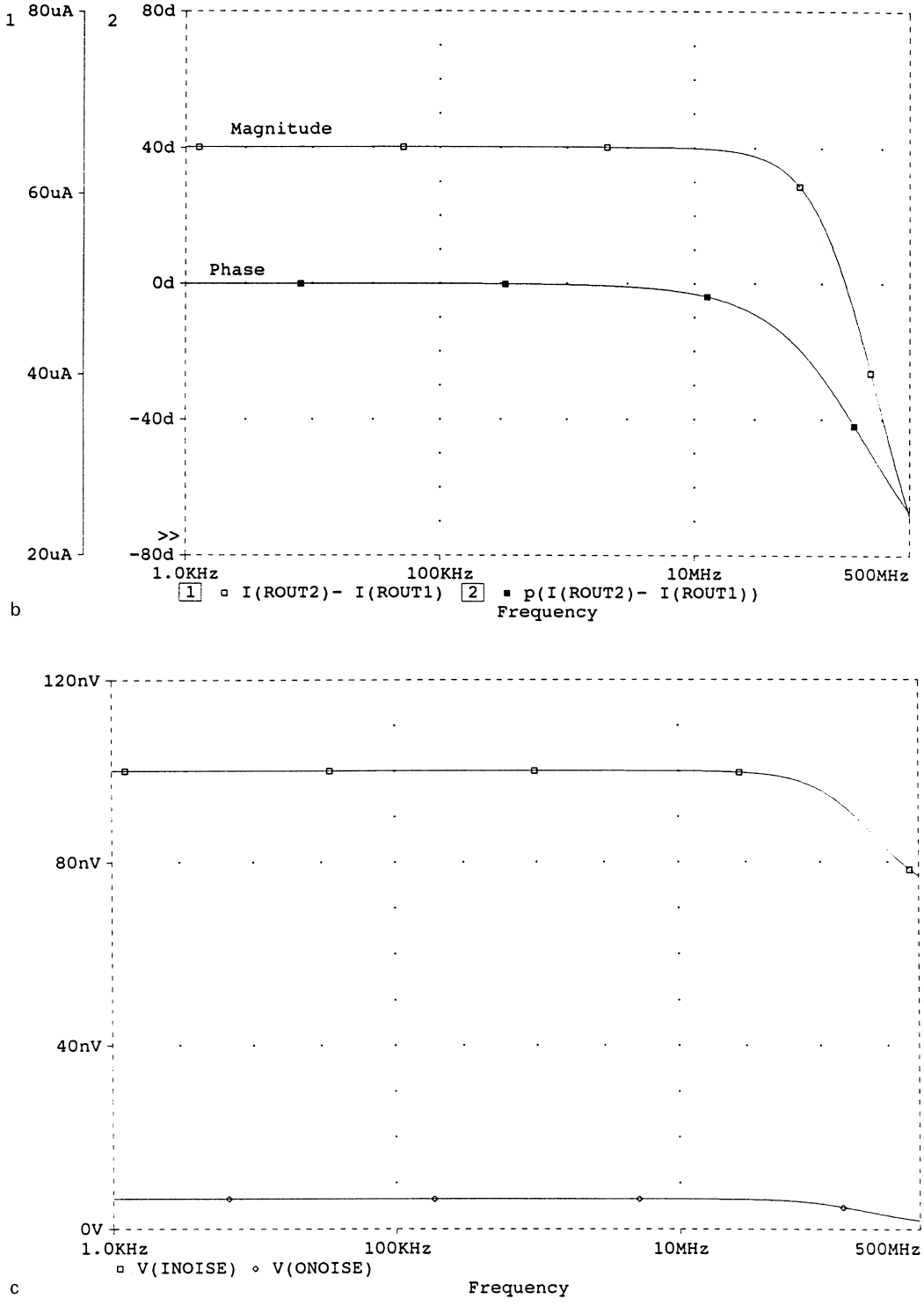
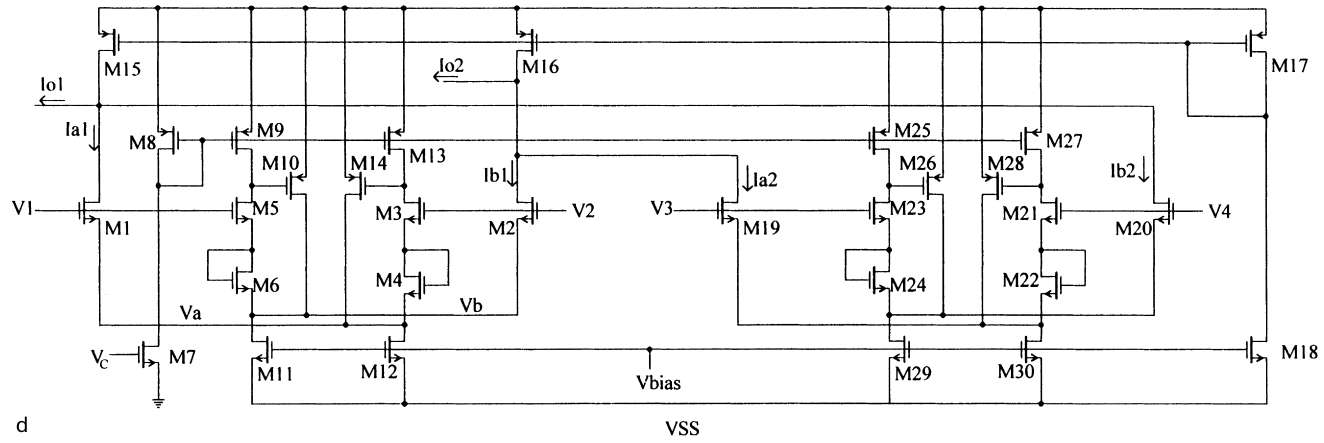


Fig. 3. *Continued.*



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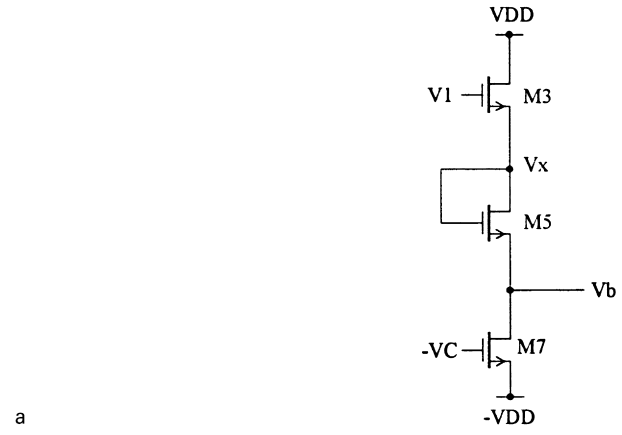


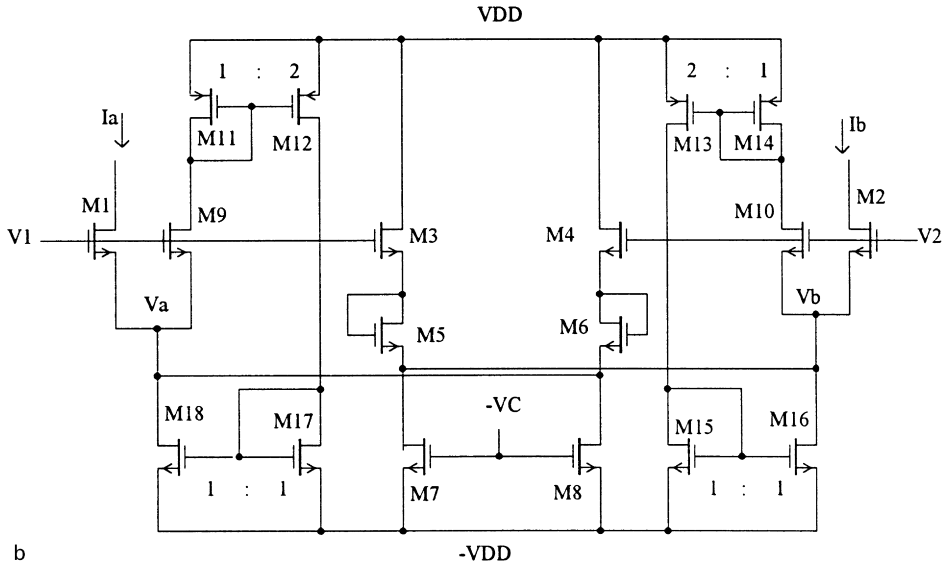


Fig. 4. (a) The biasing circuit for the second solution. (b) The CMOS transconductor of the second solution.

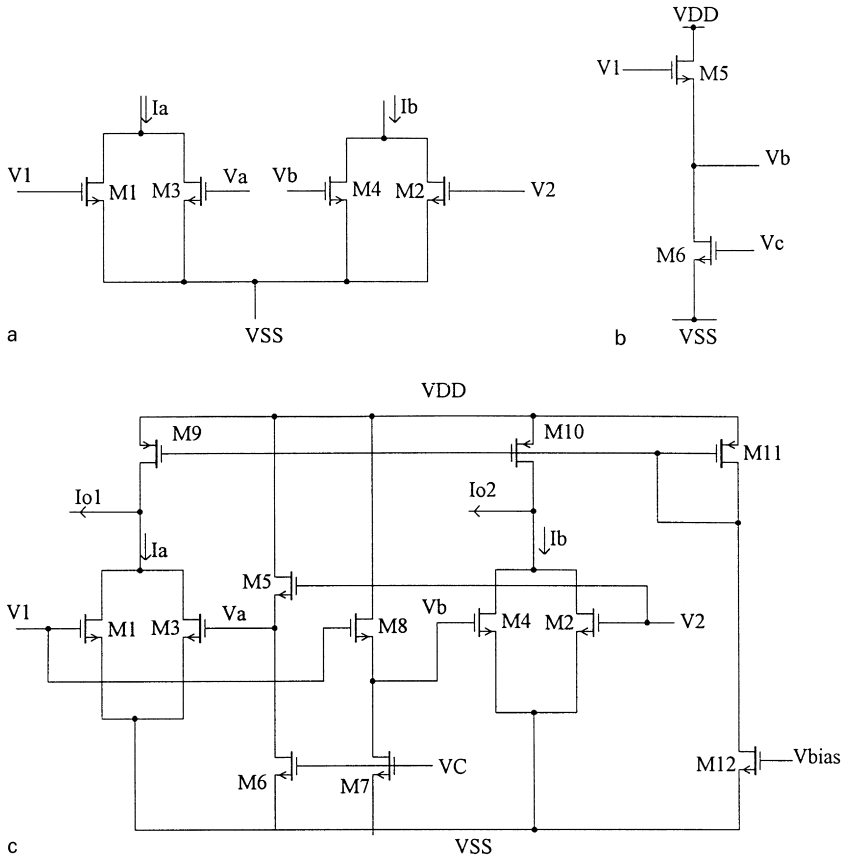


Fig. 5. (a) The basic cell of the second transconductor circuit. (b) The biasing circuit for the second proposed CMOS transconductor. (c) The second proposed fully CMOS differential transconductor.

previous THD is decreased consequently. For $V_{DD} = 2.5$ V and $V_C = 1.4$ V, the input common mode range for THD less than 0.25% at 100KHz is 1.25 V. When the mismatch between the M1 and M2 is increased to 5%, 10% and 20%, the input common mode range for the same THD is reduced to 1.25 V, 1.05 V, 0.825 V, respectively. The Power Supply Rejection Ratio (PSRR) from the positive supply to the output is 98dB and from the negative supply to the output is 98 dB. The overall CMOS differential difference transconductor using the first proposed transconductor is shown in Fig. 3(d).

2.2. The second proposed transconductor circuit based on the first configuration

A second example for $m = 1$ and $E = V_{DD}$, the biasing voltages V_a and V_b are given by:

$$V_a = V_2 + V_C - V_T - V_{DD} \tag{20}$$

$$V_b = V_1 + V_C - V_T - V_{DD} \tag{21}$$

This can be achieved by using the MOS circuit shown in Fig. 4(a). The currents of the transistors M3, M5 and M7 are equal and are given, respectively, by

$$I_3 = \frac{K_3}{2}(V_1 - V_X - V_T)^2 \tag{22}$$

$$I_5 = \frac{K_5}{2}(V_X - V_b - V_T)^2 \tag{23}$$

$$I_7 = \frac{K_7}{2}(V_{DD} - V_C - V_T)^2 \tag{24}$$

From the previous equations and with $K_3 = K_5 = 4K_7$, the desirable voltage V_b as given by Eq. (21) is obtained. Similarly, the biasing voltage V_a can be obtained using a similar CMOS circuit to that shown in Fig. 4(a). Therefore, the transconductor G is given by:

$$G = 2K(V_{DD} - V_C) \tag{25}$$

The overall CMOS fully differential transconductor circuit is shown in Fig. 4(b). The transistors M1 and M2 are the basic transistors, M3–M8 perform the basic nonlinearity cancellation which generates the necessary biasing voltages V_a and V_b and the rest of the circuit consisting from M9 through M18 are current mirrors or constitute a part of a current mirror. These current mirrors ensure that the sources of the transistors M1 and M2 do not draw a current from their respective biasing circuit. It is clear that this solution (which corresponds to $m = 1$ and $E = V_{DD}$) requires a large

number of transistors compared to the first solution (which corresponds to $m = 1$ and $E = 2V_C$). This solution is added only to indicate the main disadvantage of the first configuration, this is the requirement to a large number of transistors and is solved by the second proposed configuration in the following section.

3. The CMOS differential difference transconductors based on the second configuration

One of the basic problems in the first configuration is the biasing of the sources of the transistors with biasing circuits which must provide buffered output voltages since the sources of the transistors are low impedance nodes. This problem is avoided through the use of a new configuration based on four matched transistors connected in three different forms. It may appear that the new CMOS circuit may require a large number of transistors since it is based on four transistors not on two as in the first one. The proposed transconductors of this section employ a smaller number of transistors since these transconductors need a simple biasing circuit for the first transconductor circuit and simple control biasing voltages for the other transconductor circuits as indicated in the following subsections.

3.1. The first four NMOS transistor transconductor circuit

Fig. 5(a) shows the first four NMOS transistor circuit where the input voltages are the gate voltages of M1 and M2 and also the biasing voltages are also the gates of M3 and M4. The difficulty of the first two NMOS transistor configuration in biasing the sources is avoided by biasing two gates (high impedance nodes). The currents of the four

Table 2
Transistor aspect ratios of the CMOS transconductor of Fig. 5(b)

MOS transistor	Aspect ratio (W μm/L μm)
M1–M8	4/4
M9–M12	30/4

NMOS transistors are given by:

$$I_1 = \frac{K}{2}(V_1 - V_{SS} - V_T)^2 \tag{26}$$

$$I_2 = \frac{K}{2}(V_2 - V_{SS} - V_T)^2 \tag{27}$$

$$I_3 = \frac{K}{2}(V_a - V_{SS} - V_T)^2 \tag{28}$$

$$I_4 = \frac{K}{2}(V_b - V_{SS} - V_T)^2 \tag{29}$$

The output current I_o, is given by:

$$I_o = I_a - I_b = (I_1 + I_3) - (I_2 + I_4) \tag{30}$$

therefore

$$I_o = \frac{K}{2}[(V_1 + V_2 - 2V_{SS} - 2V_T)(V_1 - V_2) - (V_a + V_b - 2V_{SS} - 2V_T)(V_b - V_a)] \tag{31}$$

From the previous equation, the necessary conditions on the biasing voltages V_a and V_b for the output current to be linear with $(V_1 - V_2)$ can be easily obtained and are given as follows:

$$V_a = V_2 - V_C + V_{SS} \tag{32}$$

$$V_b = V_1 - V_C + V_{SS} \tag{33}$$

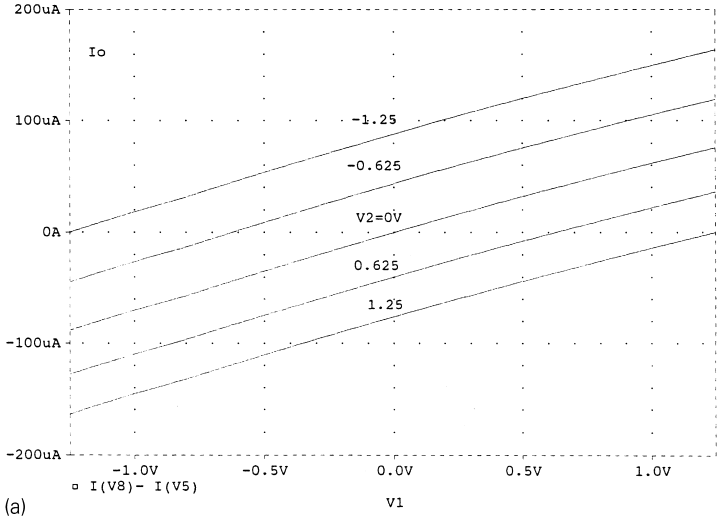
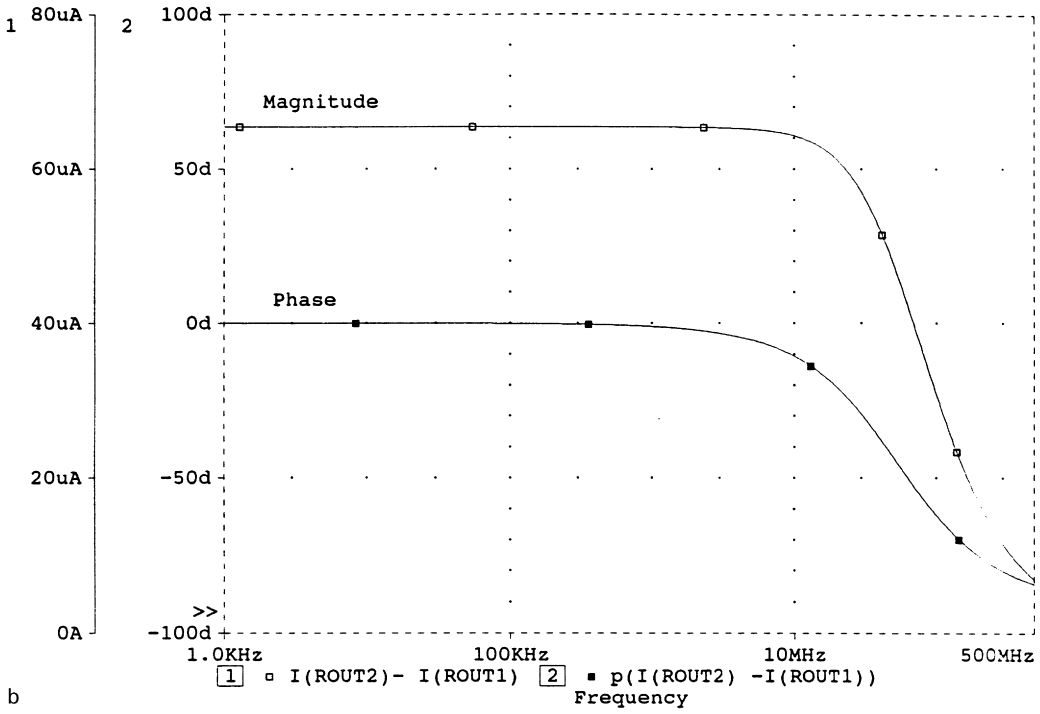


Fig. 6. (a) The I–V characteristics of the second proposed CMOS transconductor. (b) The magnitude and phase responses of the second transconductor (c) The output-referred and input-referred noise voltage spectral densities for the second transconductor when terminated by 1 KΩ. (d) The second proposed fully differential difference transconductor.



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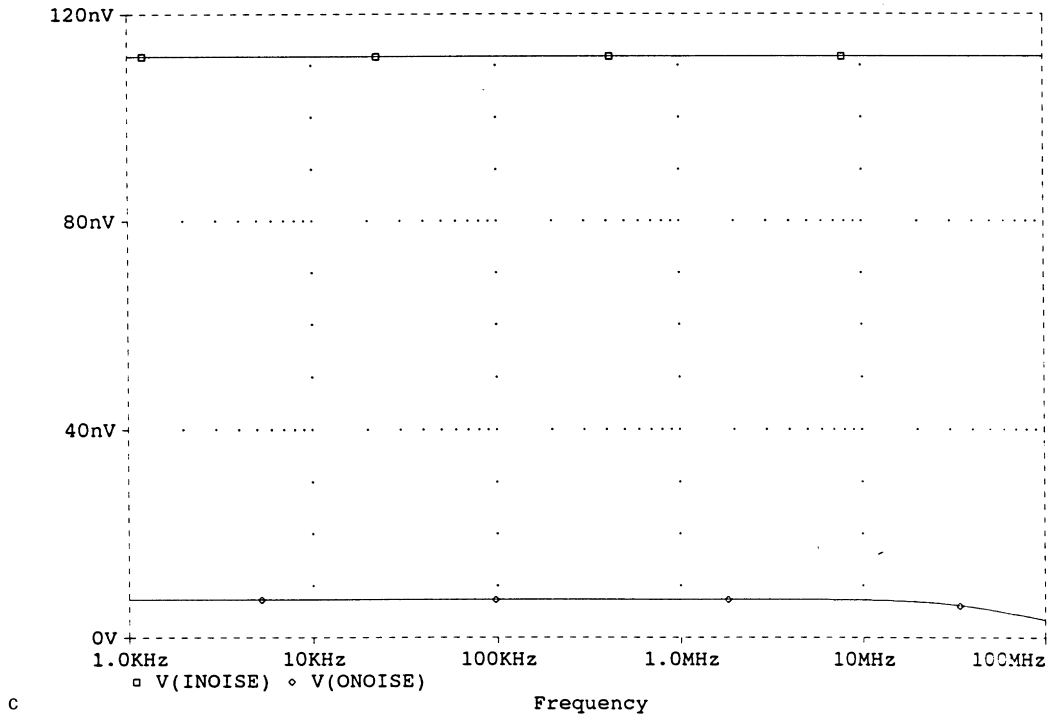

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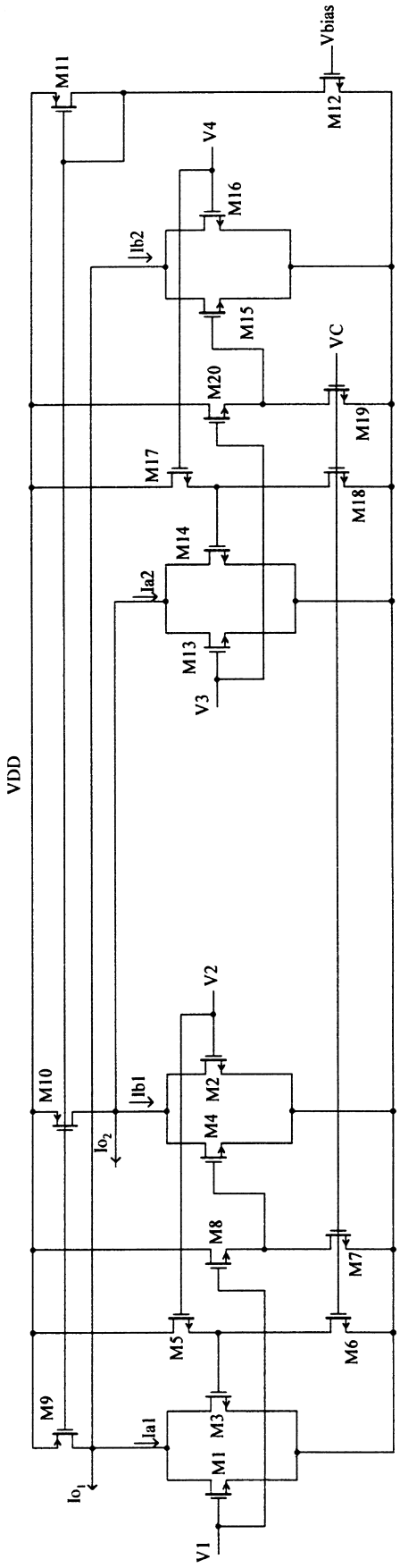
Fig. 6. *Continued.*



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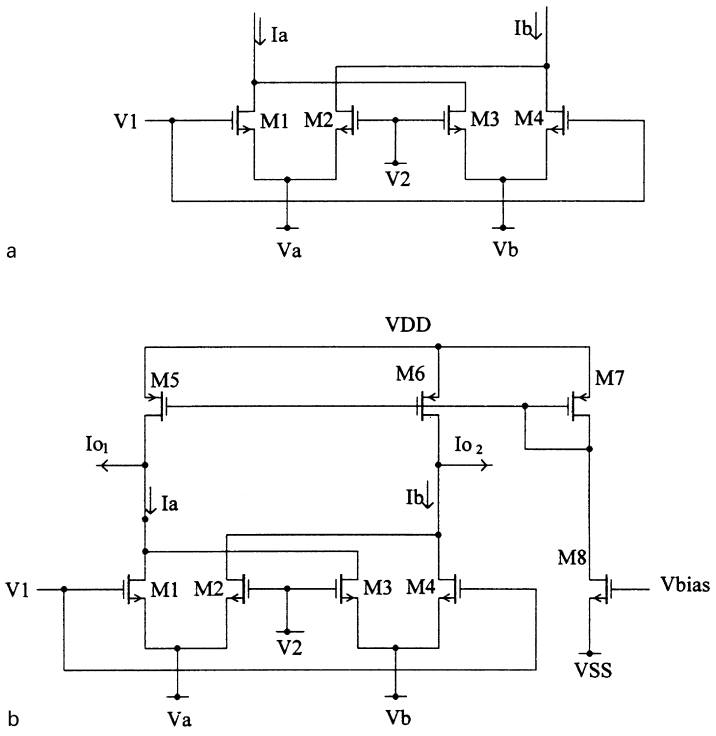


Fig. 7. (a) The basic cell of the third transconductor circuit. (b) The third proposed full differential CMOS transconductor.

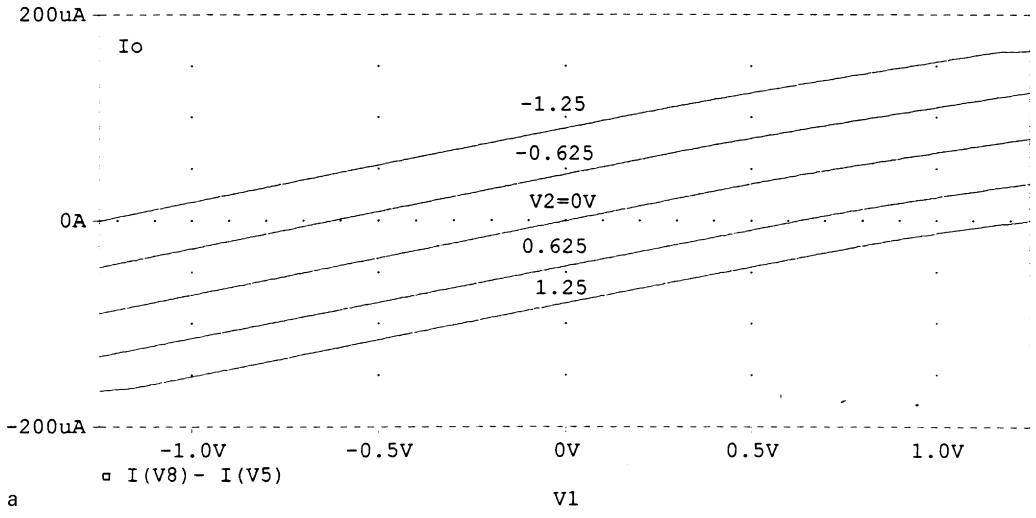


Fig. 8. (a) The I–V characteristics of the third proposed CMOS transconductor. (b) The magnitude and phase responses of the third transconductor. (c) The output-referred and input-referred noise voltage spectral densities for the third transconductor when terminated by 1 KΩ. (d) The third proposed fully differential difference transconductor.

The biasing voltage V_b can be realized, by using the MOS circuit shown in Fig. 5(b). The currents of the transistors M5 and M6 are equal and are given respectively by:

$$I_5 = \frac{K_5}{2}(V_1 - V_b - V_T)^2 \tag{34}$$

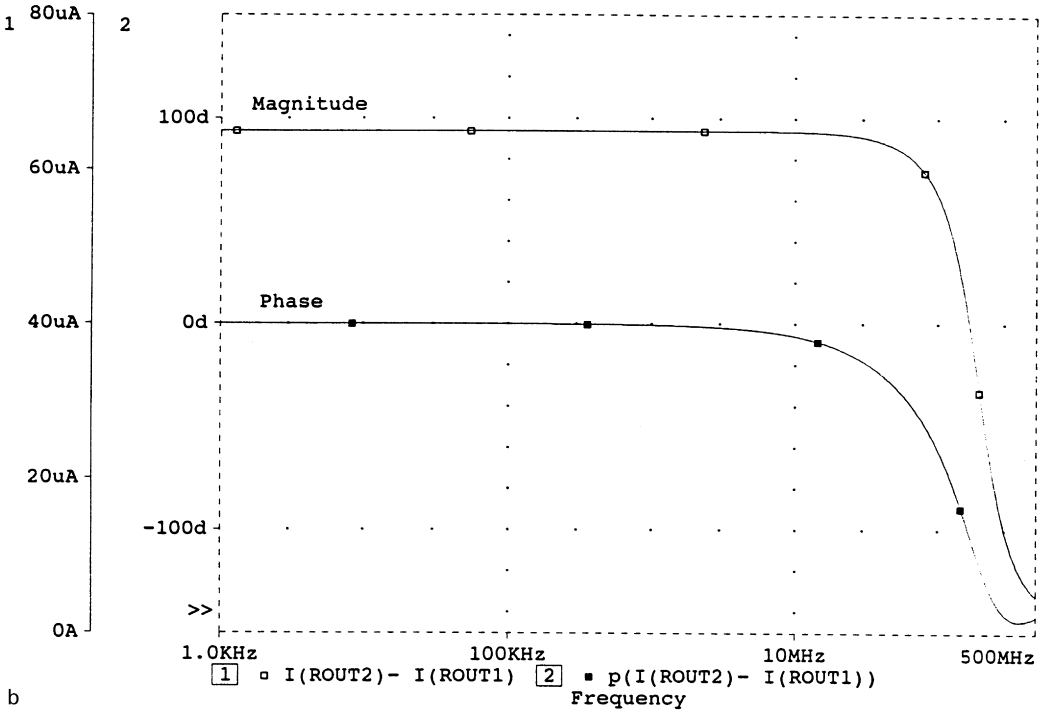
$$I_6 = \frac{K_6}{2}(V_C - V_{SS} - V_T)^2 \tag{35}$$

From the previous two equations and taking $K_5 = K_6$, the desirable biasing voltage V_b as given by Eq. (33) is obtained.

Similarly, the biasing voltage V_a can be realized using similar CMOS circuit to that shown in Fig. 5(b).

Substituting from Eqs. (32) and (33) into Eq. (31) the output current I_o is given:

$$I_o = K(V_C - V_{SS})(V_1 - V_2) \tag{36}$$



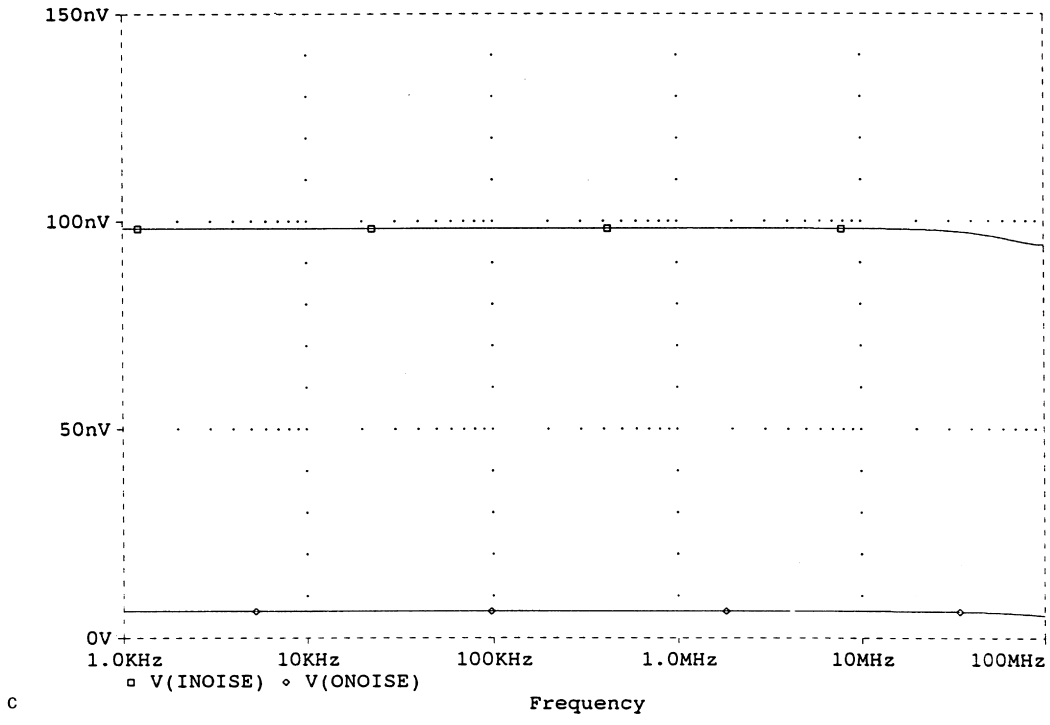


Fig. 8. *Continued.*

Table 3
Transistor aspect ratios of the CMOS transconductor of Fig. 7(a)

MOS transistor	Aspect ratio ($\mu m/L$ μm)
M1–M4	16/4
M5–M8	30/4

Thus, the transconductor G is given by:

$$G = K(V_C - V_{SS}) \tag{37}$$

Therefore, a linear differential transconductor that is tuned by the voltage V_C is obtained. The overall CMOS fully differential transconductor circuit is shown in Fig. 5(c).

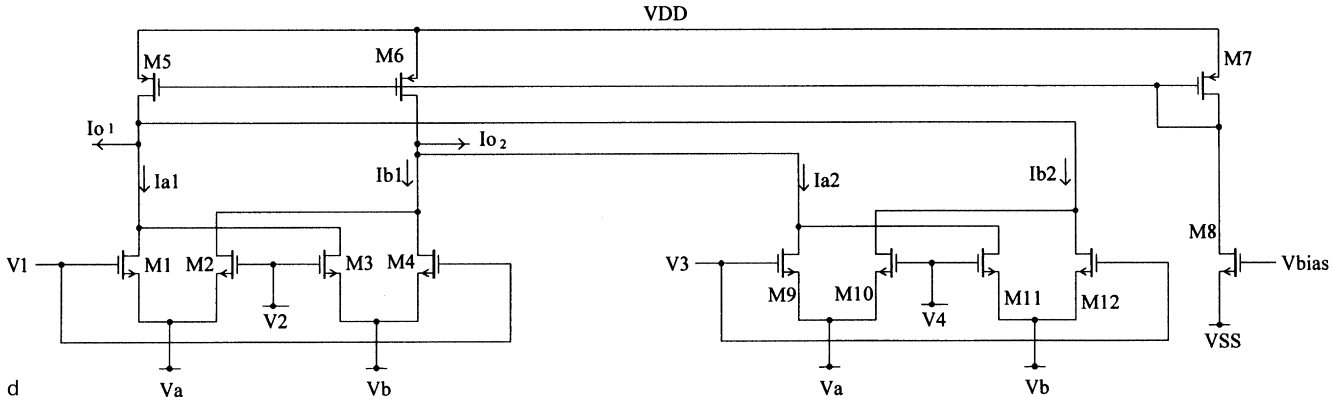


Fig. 8. *Continued.*

PSpice simulation results for this transconductor were carried out with the transistor aspect ratios as given in Table 2 and with the supply voltages equal to ±2.5 V.

Fig. 6(a) represents the I–V characteristics of this transconductor with the control voltage $V_C = -0.8$V, V_1 and V_2 scanned from −1.25 V to 1.25 V.

The magnitude and phase responses of the transconductor differential output current are shown in Fig. 6(b).

PSpice results in the output-referred and input-referred noise voltage spectral densities for this transconductor when terminated by 1 KΩ is shown in Fig. 6(c).

The THD is less than 0.3066% for 100 KHz, 1 V peak-to-peak sinusoidal input. The mismatches between the basic MOS transistors M1 to M4 produce harmonic distortion and offset of the transfer curve, therefore the input range for the same previous THD is decreased consequently. For $V_{DD} =$ 2.5 V and $V_C = -0.8$ V, the input common mode range for THD less than 0.3066% at 100 KHz is 1.25 V. When the mismatch of M1, M3 and M2, M4 is increased to 5%, 10% and 20%, the input common mode range for the same THD is reduced to 1.25 V, 1.1 V, 0.7 V, respectively. The PSRR from the positive supply to the output is 96 dB and from the negative supply to the output is 92 dB. The overall CMOS fully differential difference transconductor using the first proposed four NMOS transistor circuit is shown in Fig. 6(d).

3.2. The second four NMOS transistor transconductor circuit

Fig. 7(a) shows the second four NMOS transistor circuit in which the input voltage V_1 is connected to the gates of M1 and M4 and the input voltage V_2 is connected to the gates of the transistors M2 and M3. These four NMOS transistor cells were first used by Hyogo et al. [19] to realize an analog multiplier. The biasing voltages V_a and V_b now bias the sources of M1, M2 and M3, M4 respectively. The currents of the four NMOS transistors are given by

$$I_1 = \frac{K}{2}(V_1 - V_a - V_T)^2 \tag{38}$$

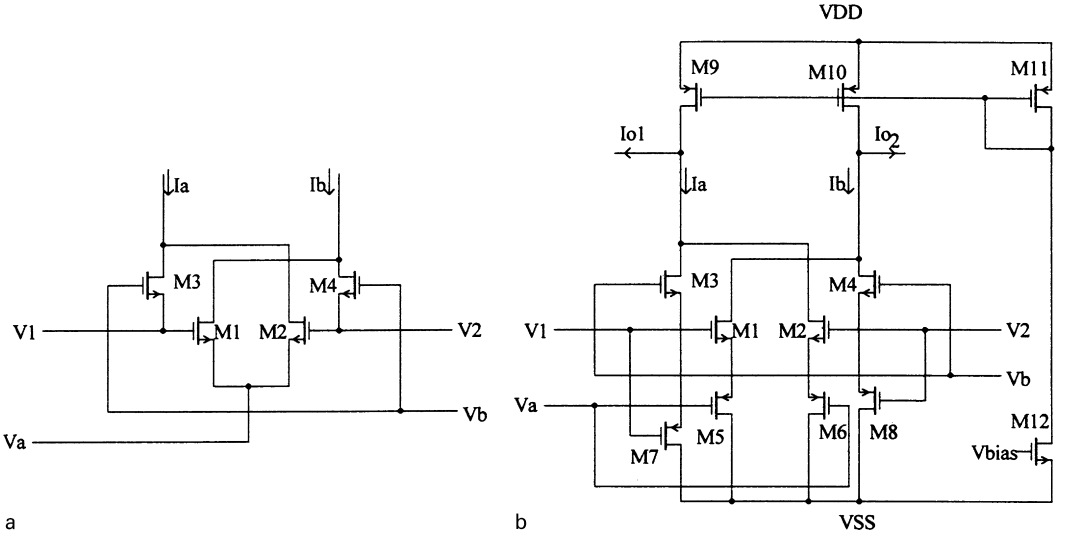


Fig. 9. (a) The basic cell of the fourth transconductor circuit. (b) The fourth proposed fully differential CMOS transconductor using composite transistors.

Table 4
Transistor aspect ratios of the transconductor of Fig. 9(b)

MOS transistor	Aspect ratio (W μm/L μm)
M1–M4	2/4
M5–M8	2/16
M9–M12	30/4

$$I_2 = \frac{K}{2}(V_2 - V_a - V_T)^2 \tag{39}$$

$$I_3 = \frac{K}{2}(V_2 - V_b - V_T)^2 \tag{40}$$

$$I_4 = \frac{K}{2}(V_1 - V_b - V_T)^2 \tag{41}$$

The output differential current I_o is given by

$$I_o = I_a - I_b = K(V_b - V_a)(V_1 - V_2) \tag{42}$$

Therefore, a linear relation between the output differential current I_o and $(V_1 - V_2)$ can be obtained with V_a and V_b being independent of V_1 and V_2.

Therefore the transconductor G is given by:

$$G = K(V_b - V_a) \tag{43}$$

which can be tuned by the differential voltage $(V_b - V_a)$. The overall CMOS fully differential transconductor circuit is shown in Fig. 7(b).

PSpice simulation results for this transconductor were carried out with the transistor aspect ratios as given in Table 3 and with the supply voltages equal to ±2.5V.

Fig. 8(a) represents the I–V characteristics with the control voltages $V_b = -2.75$ V and $V_a = -3.2$ V, V_1 and V_2 scanned from −1.25 V to 1.25 V.

The magnitude and phase responses of the transconductor differential output current are shown in Fig. 8(b).

PSpice results in the output-referred and input-referred noise voltage spectral densities for this transconductor when terminated by 1 KΩ is shown in Fig. 8(c). The THD is less than 0.309% for 100 KHz 1 V peak-to-peak sinusoidal input. The mismatches between the basic MOS transistors M1 to M4 produce harmonic distortion and offset of the transfer curve, therefore the input range for the same previous THD is consequently decreased. For $V_{DD} = 2.5$ V and $V_{ba} = 0.45$ V, the input common mode range for THD less than 0.309% at 100KHz is 1.25V. When the mismatch of M 1, M3 and M2, M4 is increased to 5%, 10% and 20%, the input common mode range for the same THD is reduced to 1.25 V, 1V, 0.5V, respectively. The PSRR from the positive supply to the output is 96 dB and from the negative supply to the output is 98 dB. The overall CMOS fully differential difference transconductor using the second proposed four NMOS transistor circuit is shown in Fig. 8(d).

3.3. The third four NMOS transistor transconductor circuit

The third four NMOS circuit with the input voltages and the biasing voltages is shown in Fig. 9(a). The currents of the four NMOS transistors are given as follows:

$$I_1 = \frac{K}{2}(V_1 - V_a - V_T)^2 \tag{44}$$

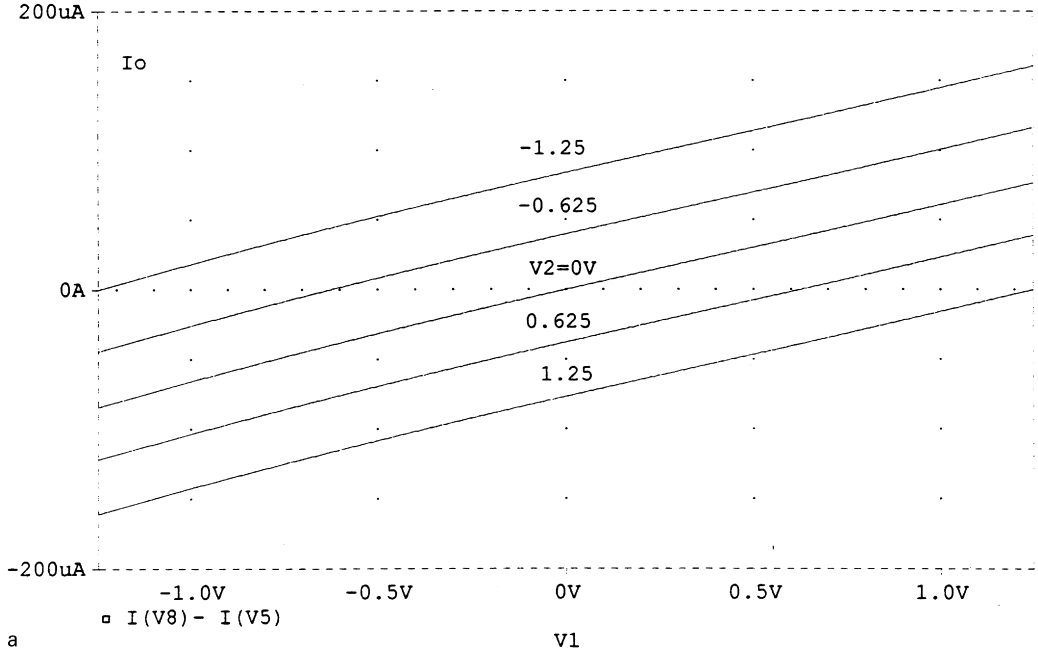
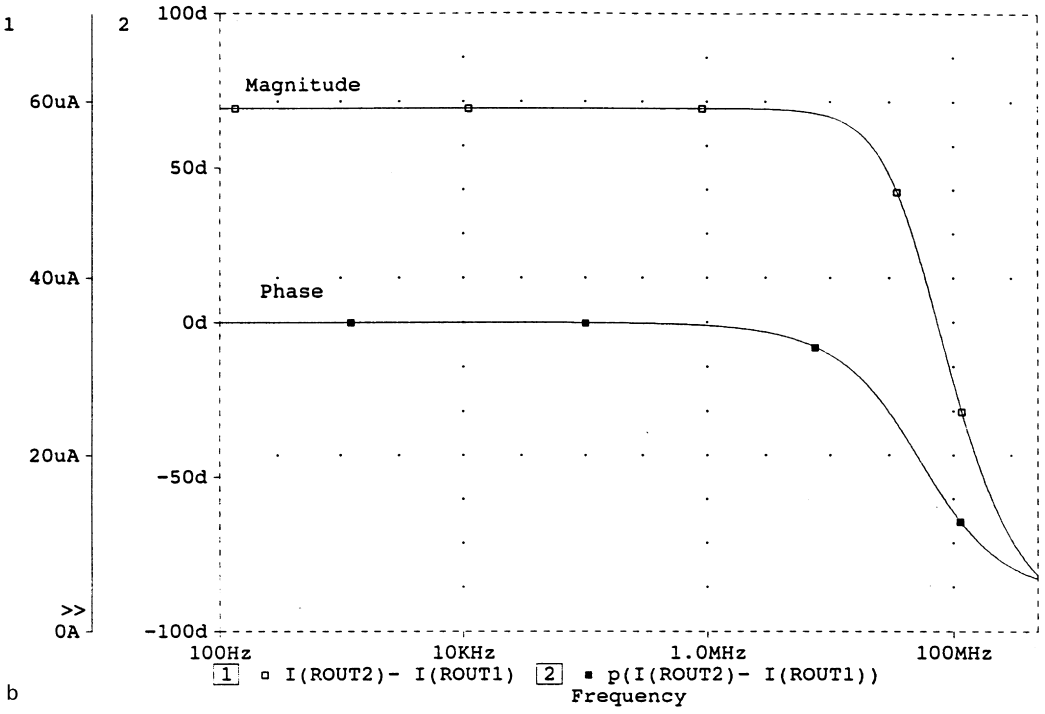
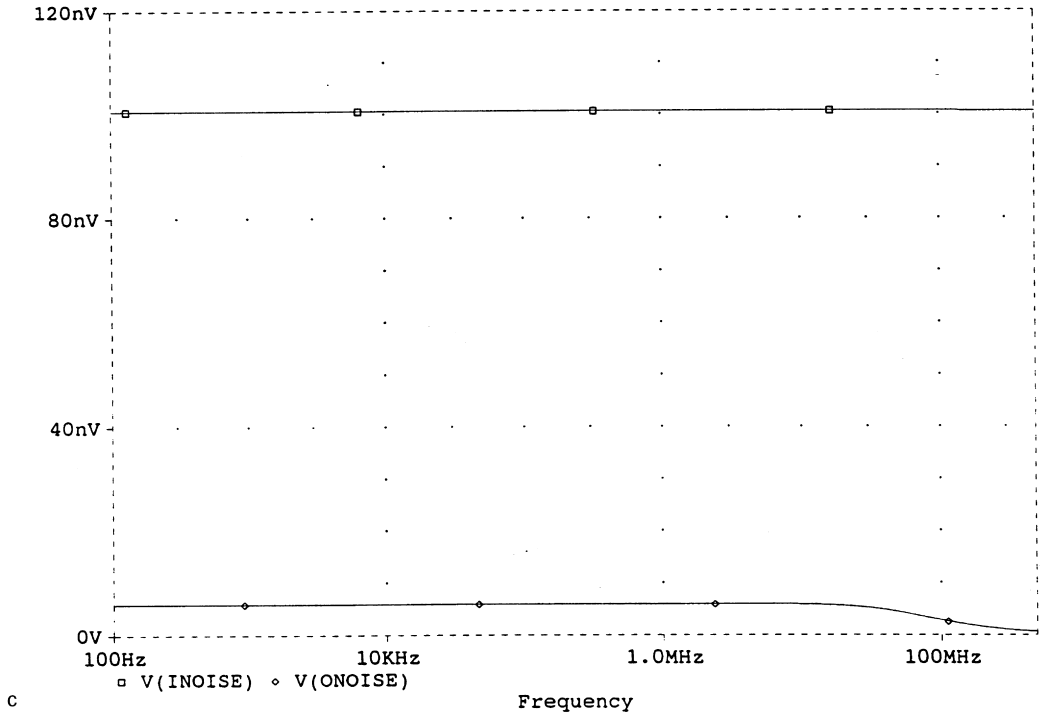


Fig. 10. (a) The I–V characteristics of the fourth proposed CMOS transconductor. (b) The magnitude and phase responses of the fourth transconductor. (c) The output-referred and input-referred noise voltage spectral densities for the fourth transconductor when terminated by 1 KΩ. (d) The fourth proposed fully differential difference transconductor.



b



c

Fig. 10. *Continued.*

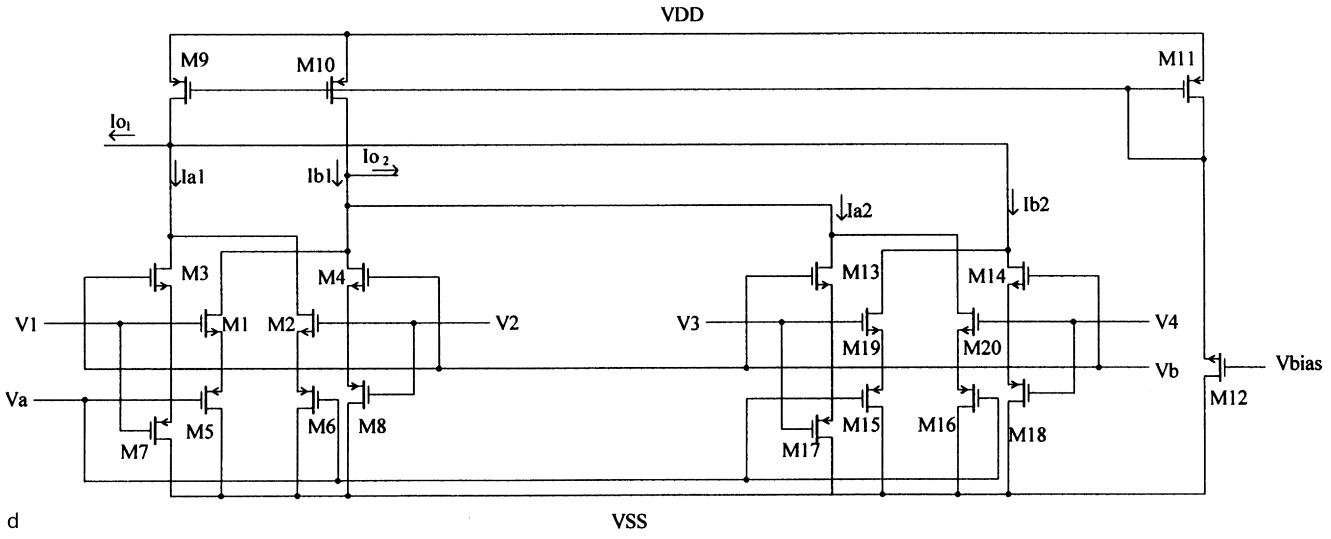


Fig. 10. *Continued.*

$$I_2 = \frac{K}{2}(V_2 - V_a - V_T)^2 \tag{45}$$

$$I_3 = \frac{K}{2}(V_b - V_1 - V_T)^2 \tag{46}$$

$$I_4 = \frac{K}{2}(V_b - V_2 - V_T)^2 \tag{47}$$

The differential output current I_o is given by:

$$I_o = I_a - I_b = K(V_a - V_b + 2V_T)(V_1 - V_2) \tag{48}$$

Therefore, a linear relation between the differential output current I_o and $(V_1 - V_2)$ can be obtained with V_a and V_b being independent of V_1 and V_2. The transconductor G is given by:

$$G = K(V_a - V_b + 2V_T) \tag{49}$$

Thus, the transconductor G can be controlled by the differential voltage $V_a - V_b$. The main disadvantage of this circuit is that the input voltages V_1 and V_2 are not buffered. This problem is overcame by replacing each transistor with its equivalent composite transistor as shown in Fig. 9(b). The main disadvantage of the composite transistor [18] which provides two high input impedance terminals is the high equivalent threshold voltage. Recently, new CMOS composite transistors are presented [19] with low threshold voltage. The transconductor value now after using the composite transistor is given by:

$$G = K_{\text{eff}}(V_a - V_b + 2V_{\text{Teff}}) \tag{50}$$

where

$$K_{\text{eff}} = \frac{K_n K_p}{\left(\sqrt{K_n} + \sqrt{K_p}\right)^2} \tag{51}$$

and

$$V_{\text{Teff}} = V_{Tn} + |V_{Tp}| \tag{52}$$

PSpice simulation results for this transconductor were carried out with the transistor aspect ratios as given in Table 4 and with the supply voltages equal to ±2.5 V.

Fig. 10(a) represents the I–V characteristics with the control voltages $V_a = -2$ V and $V_b = 2$ V and V_1, V_2 scanned from -1.25 V to 1.25 V. The magnitude and phase responses of the transconductor differential output current are shown in Fig. 10(d).

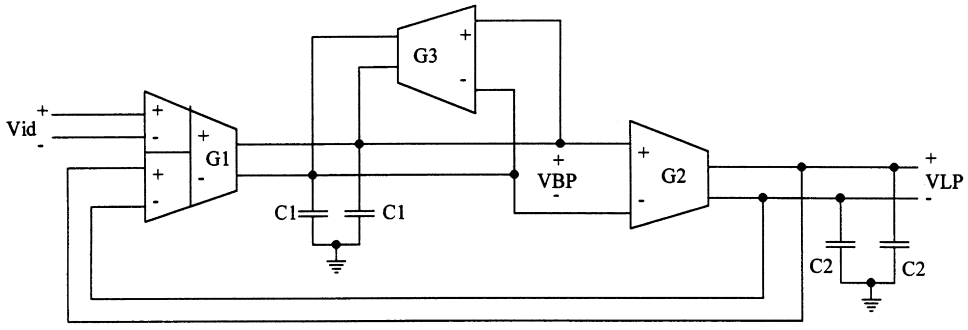
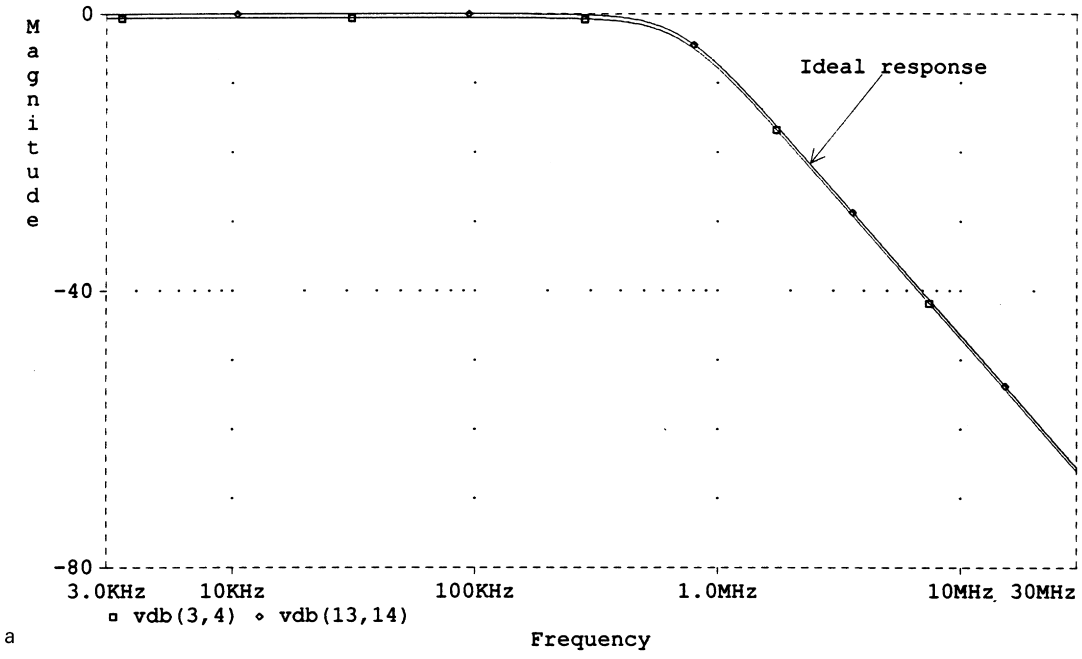
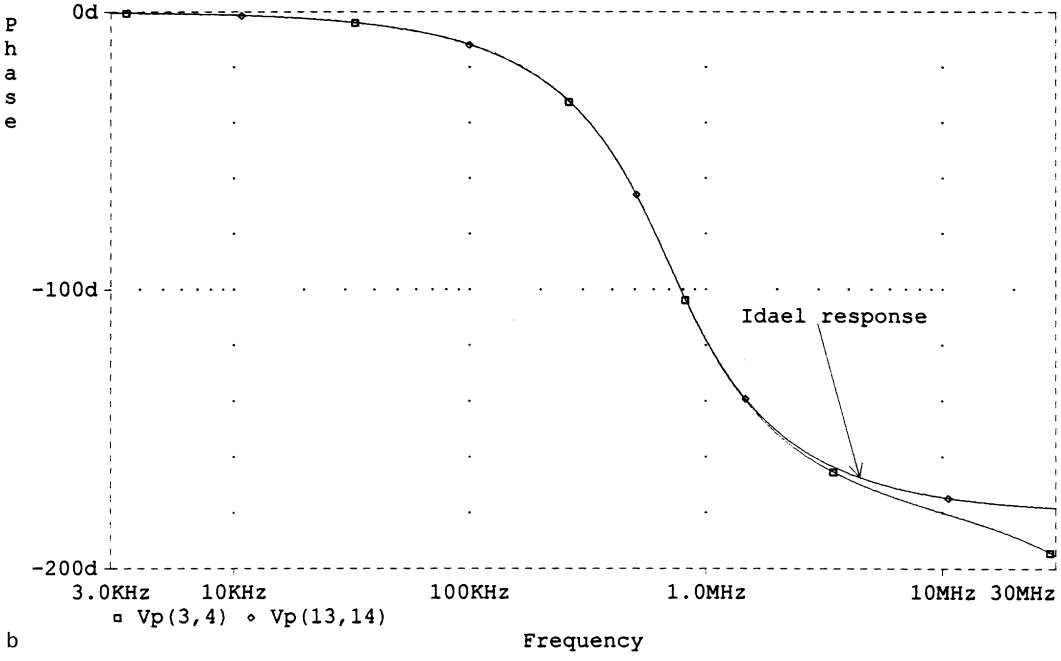


Fig 11. The fully differential bandpass–lowpass filter.

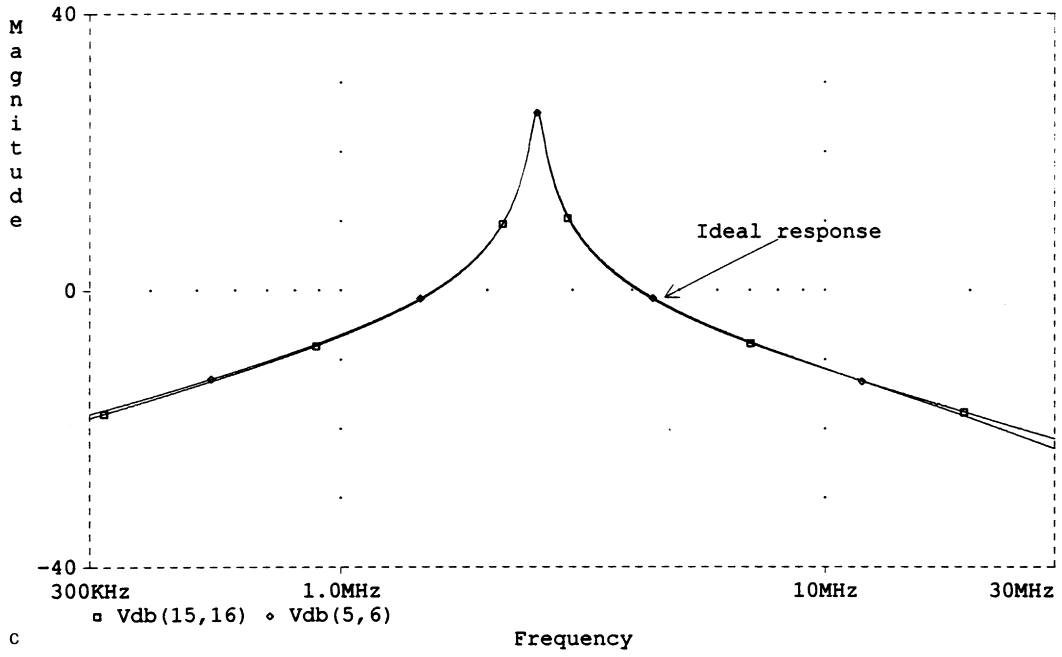


a

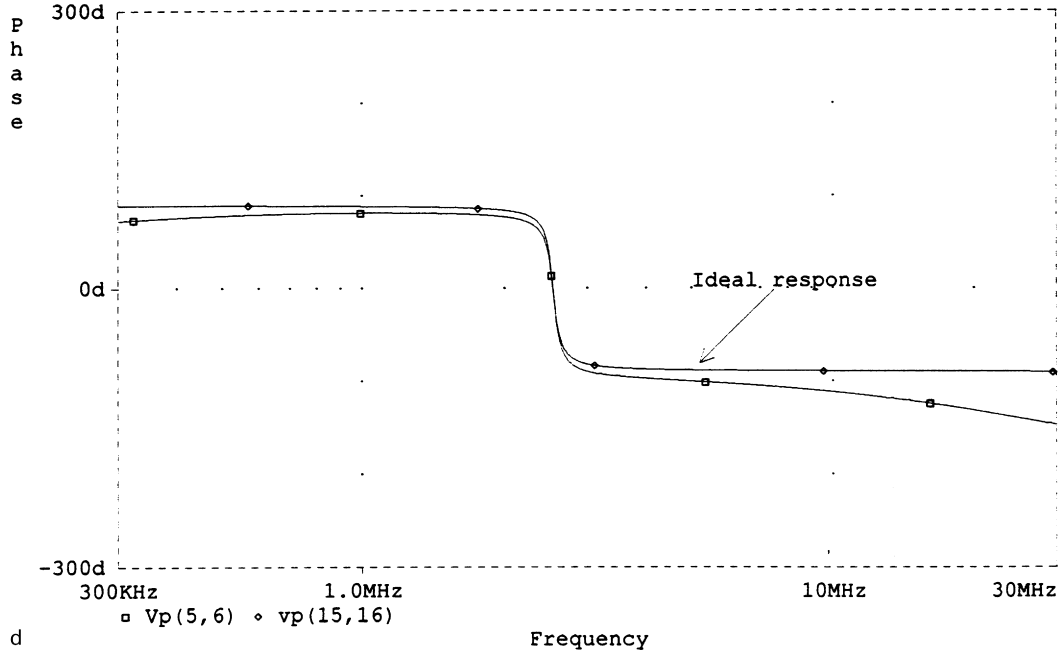


b

Fig. 12. (a) The magnitude response of the lowpass filter output. (b) The phase response of the lowpass filter output. (c) The magnitude response of the bandpass filter output. (d) The phase response of the bandpass filter output.



c



d

Fig. 12. *Continued.*

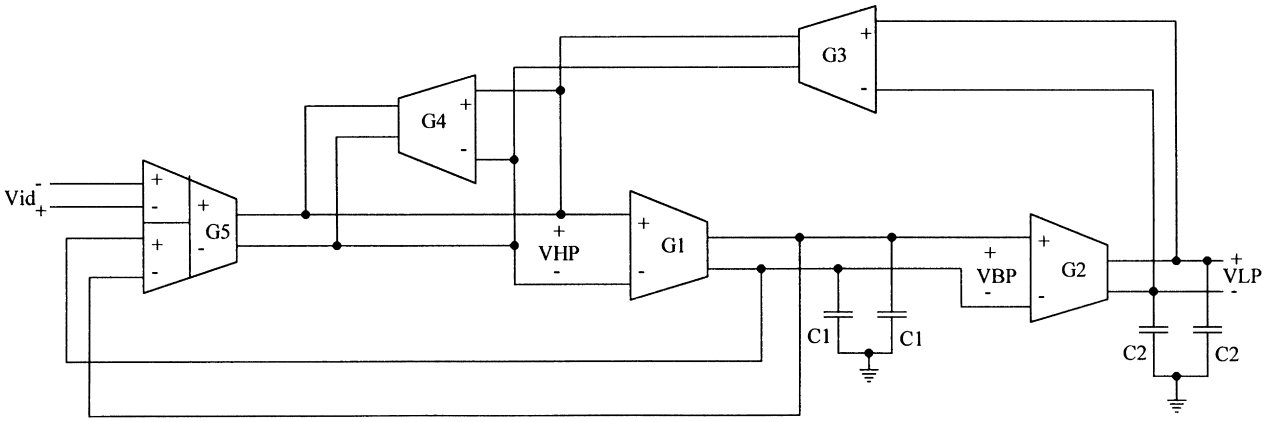


Fig. 13. The fully differential lowpass–bandpass–highpass filter.

PSpice results in the output-referred and input-referred noise voltage spectral densities for this transconductor when terminated by 1 KΩ is shown in Fig. 10(c). The THD is less than 0.32% for 100 KHz, 1 V peak-to-peak sinusoidal input. The mismatches between the basic MOS transistors M1–M4 produce harmonic distortion and offset of the transfer curve, therefore the input range for the same previous THD is consequently decreased. For $V_{DD} = 2.5$ V and $V_{ba} = 4$ V, the input common mode range for THD less than 0.32% at 100 KHz is 1.25 V. When the mismatch of M1, M4 and M2, M3 is increased to 5%, 10% and 20%, the input common mode range for the same THD is reduced to 1.25 V, 0.9 V, 0.6 V, respectively. The PSRR from the positive supply to the output is 96 dB and from the negative supply to the output is 94 dB. The overall CMOS fully differential difference transconductor using third proposed four NMOS transistor circuit is shown in Fig. 10(d).

4. The proposed fully differential filters

Any active filter implementation requires basic functions such as integration, lossy integration and addition [20]. The addition subtraction in the filters based on the differential transconductors is achieved by simply connecting the output of the transconductors that deliver the signals to be summed. In this section the applications of the proposed transconductors to realize fully differential second order lowpass-bandpass filter and lowpass–bandpass–highpass filter with independent control on Q are given.

4.1. Fully differential lowpass and bandpass biquad circuit

An example of the use of the proposed differential transconductors in the realization of an active filter is shown in Fig. 11. The filter has bandpass and lowpass outputs in a differential form. The circuit includes three transconductors and four grounded capacitors, which makes the filter suitable for VLSI implementation. The transfer functions of the bandpass and the lowpass outputs are given by:

$$\frac{V_{BP}}{V_{id}} = \frac{\frac{sG_1}{C_1}}{D(s)} \tag{53}$$

$$\frac{V_{LP}}{V_{id}} = \frac{\frac{G_1G_2}{C_1C_2}}{D(s)} \tag{54}$$

where

$$D(s) = s^2 + s\frac{G_3}{C_1} + \frac{G_1G_2}{C_1C_2} \tag{55}$$

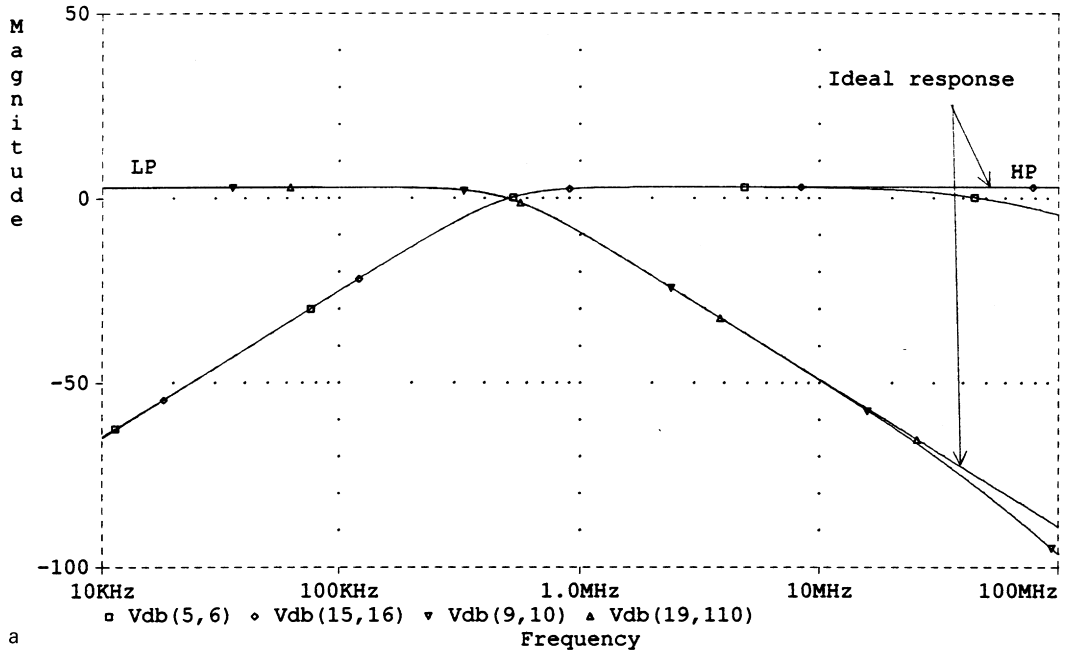
$$\omega_o = \sqrt{\frac{G_1G_2}{C_1C_2}} \tag{56}$$

and

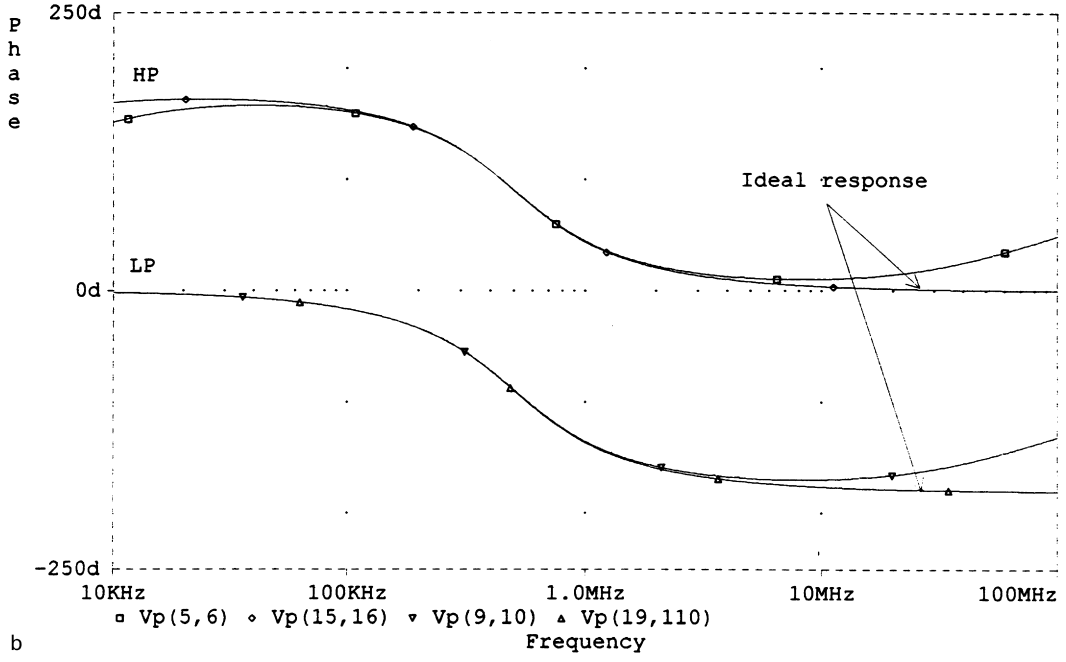
$$Q = \frac{\sqrt{\frac{C_1}{C_2}G_1G_2}}{G_3} \tag{57}$$

To simplify the design, let $G_1 = G_2 = G$ and $C_1 = C_2 = C$. As a result $\omega_o = G/C$ and $Q = G/G_3$. Therefore, high Q can be realized by increasing the G/G_3 ratio which can be achieved by programming G_3 through the control voltage of the transconductor circuit.

The PSpice simulation results of the active filter using the first proposed transconductor shown in Fig. 2(c) with $G_1 = G_2 = G_3/\sqrt{2} = 62.8$ μA/V and $C_1 = C_2 = 20$ pF to obtain a maximally flat magnitude lowpass response designed for a DC gain of 1 and $f_o = 500$ KHz is shown in Figs. 12(a) and (b) indicating both the magnitude and phase of the lowpass output. The simulation results of the bandpass response with $G_1 = G_2 = 20G_3 = 315$ μA/V and $C_1 = C_2 = 20$ pF to obtain a bandpass filter with centre frequency $f_o = 2.5$ MHz, $Q = 20$ and $|T_{BP}(\omega_o)| = 20$ is shown in Fig. 12(c) and (d) indicating both the magnitude and phase of the bandpass output.

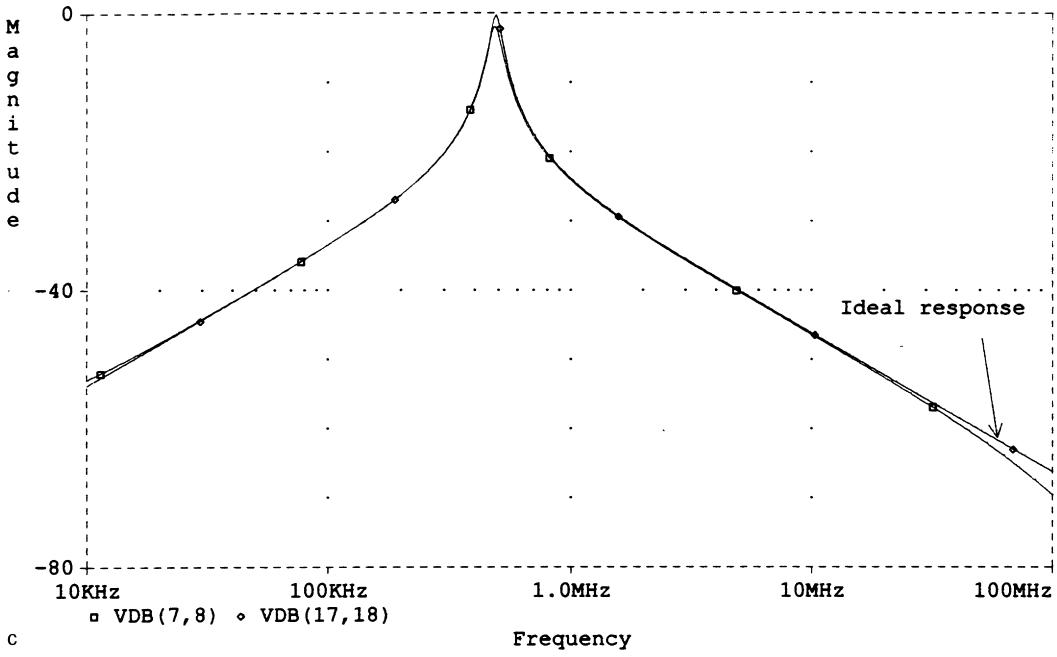


a

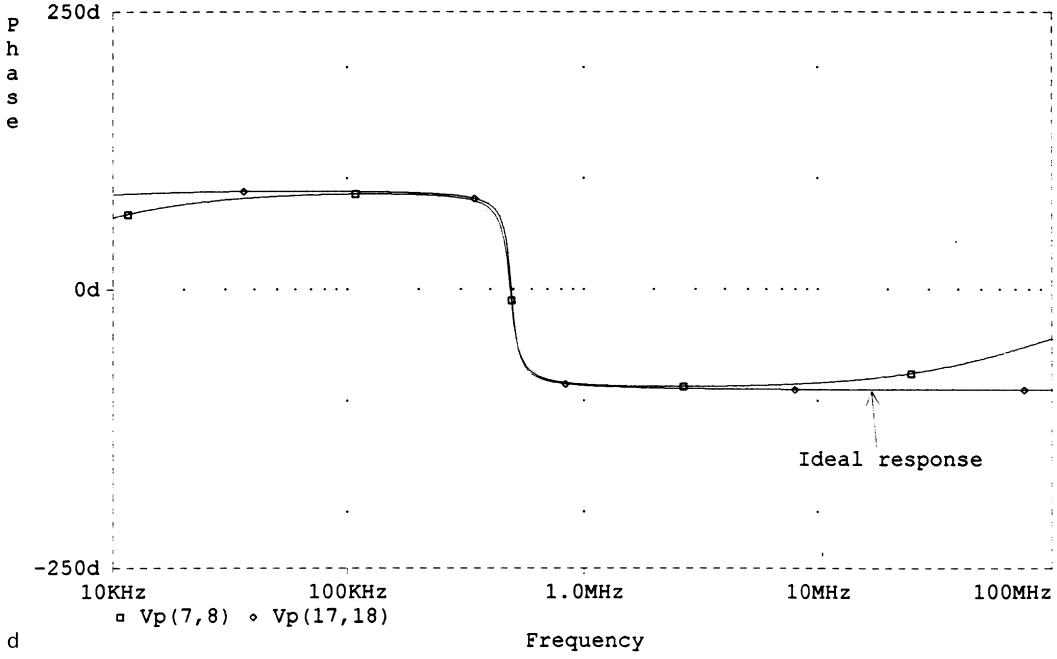


b

Fig. 14. (a) The magnitude response of the lowpass and highpass filter outputs. (b) The phase response of the lowpass and highpass filter outputs. (c) The magnitude response of the bandpass filter output. (d) The phase response of the bandpass filter output.



c



d

Fig. 14. *Continued.*

Table 5
A summary of the basic features of the four fully differential difference CMOS transconductors

Fully differential difference transconductor	Fig.	Configuration	No. of transistors	Transconductance G	THD for 1 V pp, 100 KHz sinusoidal input	Input common mode range (V) for different percentage mismatch			Cut frequency f_{3db} (MHz)
						5%	10%	20%	
First proposed circuit	3(d)	The two NMOS transistors	30	$2KV_C$	0.25%	1.25	1.05	0.83	186
Second proposed circuit	6(d)	The first four NMOS transistors	20	$K(V_C - V_{SS})$	0.3066%	1.25	1.1	0.7	53
Third proposed circuit	8(d)	The second four NMOS transistors	12	$K(V_b - V_a)$	0.309%	1.25	1	0.5	146.5
Fourth proposed circuit	10(d)	The third four NMOS transistors	20	$K_{eff}(V_b - V_a + 2V_{eff})$	0.32%	1.25	0.9	0.6	53.8

4.2. Fully differential lowpass, bandpass and highpass biquad circuit

Fig. 13 represents the new filter circuit which realizes second order lowpass, bandpass and highpass outputs in a differential form. The circuit includes five transconductors and four grounded capacitors, which makes the filter suitable for VLSI implementation. The transfer functions of the lowpass, bandpass and highpass outputs are given by:

$$\frac{V_{HP}}{V_{id}} = \frac{\frac{G_5}{G_4}s^2}{D(s)} \tag{58}$$

$$\frac{V_{BP}}{V_{id}} = \frac{\frac{G_5G_1}{G_4C_1}s}{D(s)} \tag{59}$$

$$\frac{V_{LP}}{V_{id}} = \frac{\frac{G_5G_1G_2}{G_4C_1C_2}}{D(s)} \tag{60}$$

where

$$D(s) = s^2 + \frac{G_5G_1}{G_4C_1}s + \frac{G_3G_1G_2}{G_4C_1C_2} \tag{61}$$

$$\omega_o = \sqrt{\frac{G_3G_1G_2}{G_4C_1C_2}} \tag{62}$$

and

$$Q = \frac{1}{G_5}\sqrt{\frac{C_1G_2}{C_2G_1}G_3G_4} \tag{63}$$

To simplify the design, let $G_1 = G_2 = G$, $G_3 = G_4 = G_Q$ and $C_1 = C_2 = C$. As a result $\omega_o = G/C$ and $Q = G_Q/G_5$. Therefore, high Q can be realized by increasing the ratio G_Q/G_5, which can be achieved by programming G_5 through the control voltage of the transconductor circuit.

The PSpice simulation results of the active filter using the first proposed transconductor shown in Fig. 2(c) with $G = G_5 = \sqrt{2}G_Q = 63\ \mu$A/V and $C_1 = C_2 = 20$ pF to obtain a maximally flat magnitude lowpass and highpass responses designed for a DC and high frequency gain of $\sqrt{2}$ and $f_o = 500$ KHz is shown in Fig. 14(a) and (b) indicating both the magnitude and phase of the lowpass and the highpass outputs.

The simulations results of the bandpass response with $G = G_5 = G_Q/10 = 63\ \mu$A/V and $C_1 = C_2 = 20$ pF to obtain a bandpass filter with a centre frequency $f_o = 500$ KHz, $Q = 10$ and $|T_{BP}(\omega_o)| = 1$ is shown in Fig. 14(c) and (d) indicating both the magnitude and phase of the bandpass output.

5. Conclusions

Four new CMOS fully differential difference transconductors based on MOS transistors operating in the saturation region were presented. The realizations of the proposed circuits are based on two different configurations of basic MOS cells consisting, of two or four matched NMOS transistors. The basic features of the four CMOS transconductors discussed are summarized in Table 5, indicating the configuration used, the number of transistors used, the transconductor G, the cut off frequency f_{3db}, and the input common mode range variation with different percentage mismatch between the basic transistors of the proposed configurations to achieve a certain THD. The aspect ratios of the basic transistors in the different configuration are chosen such that the equivalent transconductor G of each circuit is approximately the same. The application of the proposed transconductors to realize fully differential filters with independent control on Q is also introduced.

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