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Refereed paper

Generation of CMOS voltage-controlled floating resistors

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A new generation method to implement CMOS floating resistors is presented. The generation method depends on the linearization of the differential current of two matched NMOS transistors in two alternative configurations. The CMOS floating resistors implemented are based on using MOS transistors operating in the saturation region with their sources connected to their substrates. New CMOS floating resistors using the proposed design method are given. The magnitude of each of the proposed CMOS floating resistors is tuned by a control voltage. PSpice simulation results of the new proposed CMOS floating resistors indicating the linearity range are also given. © 1997 Elsevier Science Ltd.

1. Introduction

The MOS resistor is a basic circuit element in analogue MOS circuits. Extensive research has been proposed for replacing the resistors in analogue circuits by MOS transistors, such that the circuit is fully integrated. The function of the resistor can be implemented using MOS transistors to realize voltage-controlled transconductances as in [1–3] and [4] or by linearizing the transistor operating in the non-saturation region by suitable biasing circuit on the gate such that the non-linear terms are cancelled out [1]. The direct implementation of resistors in analogue MOS circuits is usually avoided because of the low sheet resistance and accuracy limitations [5]. Several circuit techniques are available for realizing floating resistors based on the operation of the MOS transistors in either the ohmic region as given by Wang [6], Czarnul [7], Banu and Tsividis [8] and by Wilson and Chan [9], or in the saturation region as proposed by Singh *et al.* [10], Sakurai and Ismail [11] and Elwan *et al.* [12].

In this paper, a generation method for implementing CMOS voltage-controlled floating resistors is presented. The CMOS floating resistor circuits described in [11] and [12] are obtained as special cases from the proposed generation method; other new realizations of CMOS floating resistors are also given. The generation method indicates that there is a large number of MOS circuits that realize floating resistors depending on the MOS biasing circuit. In Section 2, the realization idea of the CMOS floating resistors is presented. In Section 3, the generation of the CMOS floating resistors described in [11] and [12] alongside the genera-

tion of two new CMOS floating resistors are given. Simulation results of the newly proposed CMOS floating resistors to indicate the linearity range are given.

2. The realization idea of the CMOS floating resistors

The realization of the CMOS floating resistor is basically based on two matched transistors operating in the saturation region with their sources connected to their substrates, and configured in one of two forms. In the first configuration, the two gates of the transistors are the two terminals of the resistor as shown in Fig. 1a and the two sources are biased such that the current flowing through the resistor is linear with the voltage across the resistor. In the second configuration, the two sources of the transistors are the two terminals of the resistor as shown in Fig. 1b and the two gates are biased to achieve the desirable linearity.The differential current of the two transistors is forced to be the current flowing through the resistor I_i=I_o as shown in Fig. 1.

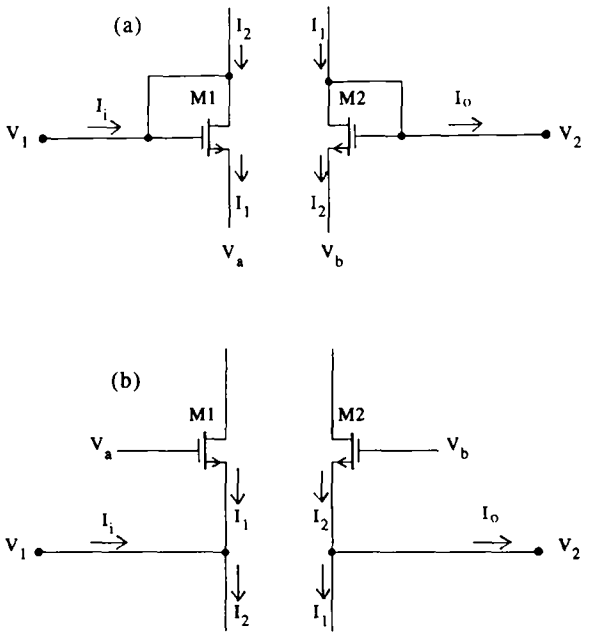

Fig. 1. The two basic configurations of the two NMOS transistors to realize a floating resistor.

The drain current of the NMOS transistor in the saturation region is given by:

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2 \tag{1}$$

where

$$K = \mu_n C_{ox} \frac{W}{L}$$

W/L is the transistor aspect ratio, C_{ox} is the gate-oxide capacitance per unit area, μ_n is the electron mobility and V_T is the threshold voltage (assumed equal for all NMOS transistors).

For the first configuration, the current flowing through the resistor is given by:

$$I_i = I_o = I_1 - I_2 \tag{2}$$

The currents I_1 and I_2 are obtained using the square-law drain current equation described above and are given by:

$$I_1 = \frac{K}{2}(V_1 - V_a - V_T)^2 \tag{3}$$

$$I_2 = \frac{K}{2}(V_2 - V_b - V_T)^2 \tag{4}$$

Therefore, the current flowing through the resistor is given by:

$$I_i = I_o = \frac{K}{2}(V_1 + V_2 - V_a - V_b - 2V_T)(V_b - V_a + V_1 - V_2) \tag{5}$$

According to the above equation, linear relation between the current flowing through the resistor and (V_1-V_2) can be achieved if the following relations are satisfied:

$$V_b - V_a + V_1 - V_2 = 2m(V_1 - V_2) \tag{6}$$

$$V_1 + V_2 - V_a - V_b - 2V_T = 2E - 2V_C \tag{7}$$

V_C is a control voltage used to control the magnitude of the resistor and allows one to compensate for process parameter spreads in the resistor value. m is a dimensionless constant and E is a constant voltage.

From the above two equations, the necessary biasing voltages V_a and V_b to achieve the linear relation between the current flowing through the resistor and $(V_1 - V_2)$ are as follows:

$$V_a = (1-m)V_1 + mV_2 + V_C - V_T - E \quad (8)$$

$$V_b = mV_1 + (1-m)V_2 + V_C - V_T - E \quad (9)$$

Therefore, the resistor current is obtained as:

$$I_i = I_o = 2Km(E - V_C)(V_1 - V_2) \quad (10)$$

Therefore, the equivalent resistance R, which is given by the voltage difference $(V_1 - V_2)$ divided by the current I_i (or I_o) is expressed in terms of the transistor parameters, the dc biasing and the control voltage as follows:

$$R = \frac{(V_1 - V_2)}{I_i} = \frac{1}{2Km(E - V_C)} \quad (11)$$

Therefore a MOS linear resistor which is tuned by the voltage V_C is obtained.

Similarly, the differential current of the two MOS transistors shown in Fig. 1b can be obtained, and is given by:

$$I_i = I_o = I_2 - I_1 \quad (12)$$

$$I_i = I_o = \frac{K}{2}(V_a + V_b - V_1 - V_2 - 2V_T)(V_b - V_a + V_1 - V_2) \quad (13)$$

A linear relation between the current flowing through the resistor and $(V_1 - V_2)$ can be achieved if the following relations are satisfied:

$$V_a + V_b - V_1 - V_2 - 2V_T = 2E - 2V_C \quad (14)$$

$$V_b - V_a + V_1 - V_2 = 2m(V_1 - V_2) \quad (15)$$

From the above two equations, the necessary biasing voltages V_a and V_b to achieve the linear relation between the current of the resistor and $(V_1 - V_2)$ are as follows:

$$V_a = (1-m)V_1 + mV_2 - V_C + V_T + E \quad (16)$$

$$V_b = mV_1 + (1-m)V_2 - V_C + V_T + E \quad (17)$$

Therefore, the resistor current is obtained as:

$$I_i = I_o = K = 2Km(E - V_C)(V_1 - V_2) \quad (18)$$

Therefore, the equivalent resistance R is given by:

$$R = \frac{1}{2Km(E - V_C)} \quad (19)$$

From eqs. (8), (9), (16) and (17) it is clear that for each value of m, a new MOS floating resistor can be implemented by biasing the gates (or sources) by the proper biasing voltages generated using a MOS circuit.

3. The generation of the CMOS floating resistors

From Section 2 it is clear that a large number of CMOS floating resistor realizations can be obtained corresponding to each value of m and E. These values are the design parameters of the biasing circuit used to bias either the gates or the sources according to the type of configuration used. In this section, the CMOS floating resistors described in [11] and [12] are generated as special cases. Two new CMOS floating resistors are also given. The generated CMOS floating resistor circuit requires a twin-well process to eliminate the body effect.

3.1. Sakurai and Ismail CMOS floating resistor

A CMOS floating resistor can be realized by using the basic configuration of Fig. 1a with m=1 and E=V_{DD} to obtain the floating resistor

described in [11], in which the biasing voltages V_a and V_b are given by:

$$V_a = V_2 + V_C - V_T - V_{DD} \quad (20)$$

$$V_b = V_1 + V_C - V_T - V_{DD} \quad (21)$$

and the resistor magnitude is given by:

$$R = \frac{1}{2K(V_{DD} - V_C)} \quad (22)$$

The overall CMOS floating resistor is implemented by using 20 transistors as shown in Fig. 2.

3.2. Elwan, Mahmoud and Soliman CMOS floating resistor

A CMOS floating resistor can be realized by using the basic configuration of Fig. 1b with m=1 and E=V_{DD} to obtain the CMOS floating resistor described in [12], in which the biasing voltages V_a and V_b are given by:

$$V_a = V_2 - V_C + V_T + V_{DD} \quad (23)$$

$$V_b = V_1 - V_C + V_T + V_{DD} \quad (24)$$

and the magnitude of the resistor is given by:

$$R = \frac{1}{2K(V_{DD} - V_C)} \quad (25)$$

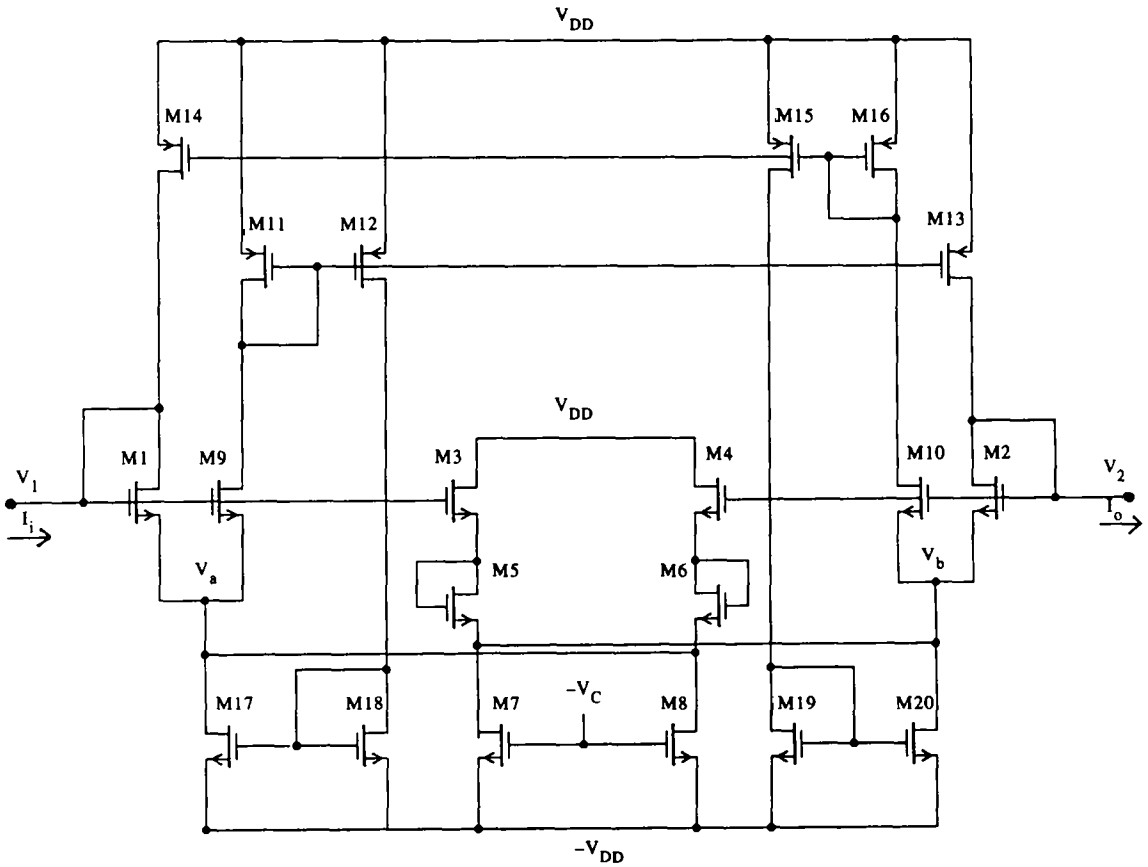

Fig. 2. Sakurai and Ismail CMOS floating resistor.

The overall CMOS floating resistor is implemented by using 15 transistors as shown in Fig. 3.

3.3. The first proposed CMOS floating resistor

A new CMOS floating resistor can be implemented by using also the basic configuration of Fig. 1b with the biasing voltages chosen to be equal by taking m=1/2 and E=V_{DD}−0.5V_T and are given by:

$$V_a = V_b = \frac{V_1 + V_2}{2} + V_{DD} - V_C + \frac{1}{2}V_T \quad (26)$$

The MOS circuit used to achieve this is shown in Fig. 4 and the above design equation for the biasing voltages can be obtained as follows.

The currents I_3 and I_4 in the transistors M3 and M4 are equal, therefore:

$$\frac{K_3}{2}(V_{DD} - V_x - V_T)^2 = \frac{K_4}{2}(V_1 + V_{DD} - V_T)^2 \quad (27)$$

Taking K_3=4K_4,

$$V_x = \frac{V_{DD} - V_T - V_1}{2} \quad (28)$$

Consider the currents in the transistors M5 and M6 and taking K_5=K_6,

$$I_5 = I_6 \quad (29)$$

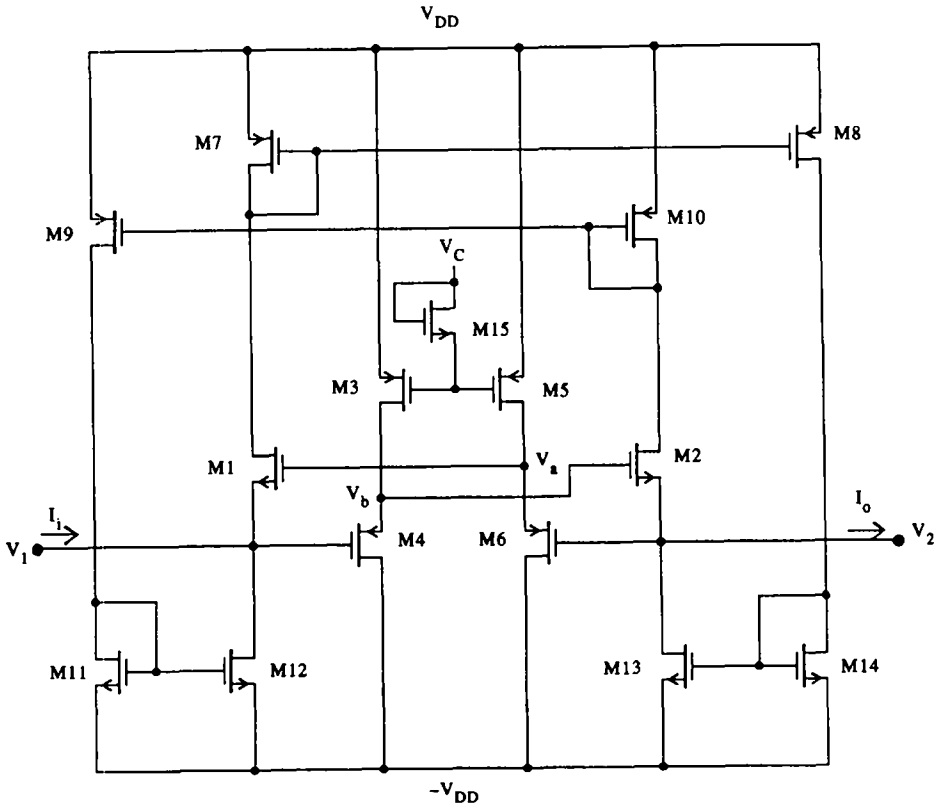

Fig. 3. Elwan, Mahmoud and Soliman CMOS floating resistor.

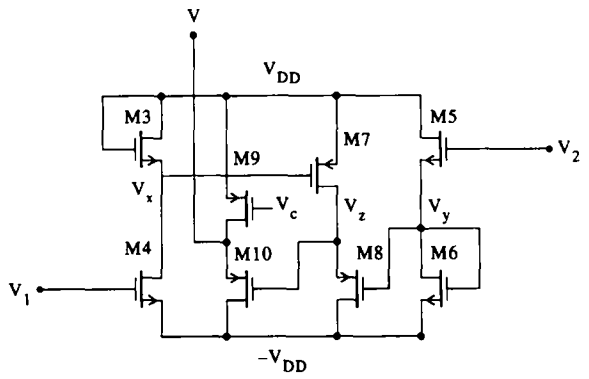

Fig. 4. The biasing circuit for the first proposed CMOS floating resistor.

$$\frac{K_5}{2}(V_2 - V_y - V_T)^2 = \frac{K_6}{2}(V_y + V_{DD} - V_T)^2 \tag{30}$$

Therefore

$$V_y = \frac{V_2 - V_{DD}}{2} \tag{31}$$

Similarly, consider the currents in the transistors M7 and M8 and take K_7=K_8; we thus have:

$$I_7 = I_8 \tag{32}$$

$$\frac{K_7}{2}(V_x - V_{DD} - V_{Tp})^2 = \frac{K_8}{2}(V_y - V_z - V_{Tp})^2 \tag{33}$$

Therefore

$$V_z = V_{DD} - V_x + V_y \tag{34}$$

Substituting eqs. (28) and (31) in eq. (34), we have:

$$V_z = \frac{V_1 + V_2 + V_T}{2} \tag{35}$$

Finally, consider the transistors M9 and M10, with K_9=K_{10}. Since the currents I_9 and I_{10} are equal:

$$\frac{K_9}{2}(V_C - V_{DD} - V_{Tp})^2 = \frac{K_{10}}{2}(V_z - V - V_{DD})^2 \tag{36}$$

From the above equation, we have:

$$V = V_z + V_{DD} - V_C \tag{37}$$

From eq. (35) in eq. (37):

$$V = \frac{V_1 + V_2}{2} + V_{DD} - V_C + \frac{V_T}{2} \tag{38}$$

The above equation gives an expression of the biasing voltage which biases the gates of the basic transistors M1 and M2 in Fig. 1b. By substitution from eq. (38) into eq. (13) of the resistor current after replacing both V_a and V_b by the biasing voltage V given in eq. (38), the resistor current is given by:

$$I_i = I_o = K\left(V_{DD} - V_C - \frac{V_T}{2}\right)(V_1 - V_2) \tag{39}$$

Therefore, the magnitude of the resistor is given by:

$$R = \frac{1}{K(V_{DD} - V_C - (V_T/2))} \tag{40}$$

The overall CMOS floating resistor circuit, which employs 18 transistors, is shown in Fig. 5, where M1 and M2 are the basic matched transistors, transistors M3–M10 represent the MOS biasing circuit for the basic transistors, and the remaining transistors perform the current transfer from the input port to the output port and vice versa.

3.3.1. Range of operation

The above analysis of the proposed CMOS floating resistor circuit is based on the assumption that all the transistors are operating in the saturation region. In this section the range of operation in which this assumption is valid is given.

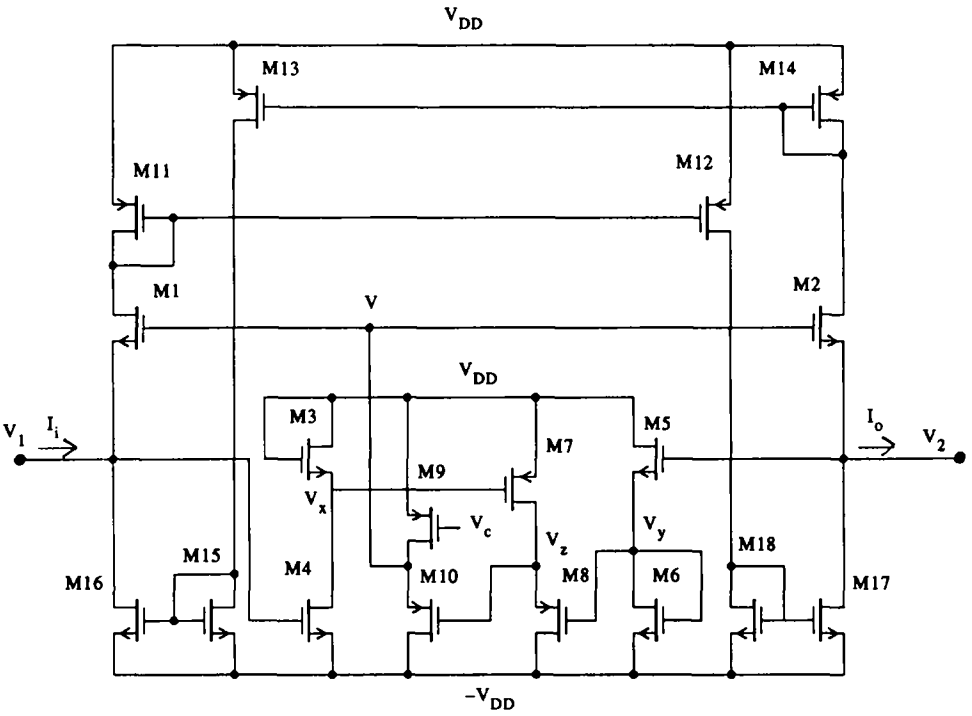

Fig. 5. The first proposed CMOS floating resistor circuit.

For the NMOS transistor to be operating in the saturation region, the following two conditions must be satisfied:

$$V_{GS} > V_T \tag{41}$$

$$V_{GD} < V_T \tag{42}$$

and for the PMOS transistor:

$$V_{SG} > |V_{Tp}| \tag{43}$$

$$V_{DG} < |V_{Tp}| \tag{44}$$

The CMOS floating resistor circuit can be divided into three basic parts, the basic transistors M1 and M2, the biasing transistors formed from M3–M10 and the current mirrors formed from transistors M11–M18. The range of operation is obtained provided that every MOS transistor in these basic parts satisfies the above conditions, and the necessary conditions needed for all transistors to operate in the saturation region can be summarized as:

$$-(V_{DD} - V_T) < V_1 < \frac{V_{DD} + V_T}{3} \tag{45}$$

$$-(V_{DD} - 2V_T) < V_2 < V_{DD} + V_T \tag{46}$$

And in terms of differential and common mode inputs:

$$-2\left(V_{DD} - V_C - \frac{V_T}{2}\right) < V_2 - V_1 < 2\left(V_{DD} - V_C - \frac{V_T}{2}\right) \tag{47}$$

$$-\left(V_{DD} + \frac{V_T}{2} + |V_{Tp}|\right) < \frac{V_2 + V_1}{2} < \left(V_{DD} - \frac{V_T}{2} - |V_{Tp}|\right) \tag{48}$$

and

$$2V_1 + V_2 < V_{DD} + 2|V_{Tp}| - 2V_T \quad (49)$$

$$V_C < V_{DD} - |V_{Tp}| \quad (50)$$

For the supply voltage V_{DD}=3.3 V, $V_T = |V_{Tp}| = 1$ V and the control voltage V_C=2 V, the range of operation in which the CMOS circuit behaves as a linear floating resistor is given by:

$$-1.6\,V < V_2 - V_1 < 1.6\,V \quad (51)$$

The above equation sets the limit on the linear range of operation of the MOS resistor circuit. For symmetrical and equal inputs the above equation results in the following two equations controlling the range of operation:

$$-0.8\,V < V_1 < 0.8\,V \quad (52)$$

and

$$-0.8\,V < V_2 < 0.8\,V \quad (53)$$

Of course, as expected the range of operation can be varied by adjusting the control voltage V_C, which makes the circuit capable of operating in many regions depending on the desirable application.

3.3.2. Simulation results

PSpice simulation results for the first proposed CMOS floating resistor were carried out with the transistor aspect ratios as given in Table 1 and with the supply voltages equal to ±3.3 V. The SPICE model parameters for the NMOS and PMOS transistors are listed in Table 3 below. Figure 6a represents the *I–V* characteristic of the resistor with control voltage V_C=2 V. V_1 and V_2 are scanned from −1 to 1 V. Figure 6c represents the magnitude response of the maximally flat magnitude Sallen and Key lowpass filter shown in Fig. 6b with C1=0.1414 nF and C2=0.0707 nF. The resistor magnitudes are controlled by the control voltage which is scanned from 1.6 to 2.2 V. The THD is less than 0.25% for a 1 MHz 1 V peak-to-peak sinusoidal input. The power consumption of each of the MOS resistors is less than 1 mW.

3.4. The second proposed CMOS floating resistor

Another new CMOS floating resistor can be implemented by using the basic configuration of Fig. 1a with the biasing voltages chosen such that the magnitude of the resistor is independent of the threshold voltage and also the supply voltage. This is achieved if m=1 and E=2V_C and the biasing voltages V_a and V_b are given by:

$$V_a = V_2 - V_C - V_T \quad (54)$$

$$V_b = V_1 - V_C - V_T \quad (55)$$

This can be obtained by using the MOS circuit shown in Fig. 7.

TABLE 1

MOS transistor	Aspect ratio (W μm/l μm)
M1, M2	10/20
M3	32/32
M4	8/32
M5, M6, M7, M8, M9, M10	4/16
M11, M12, M13, M14, M15, M16, M17, M18	30/20

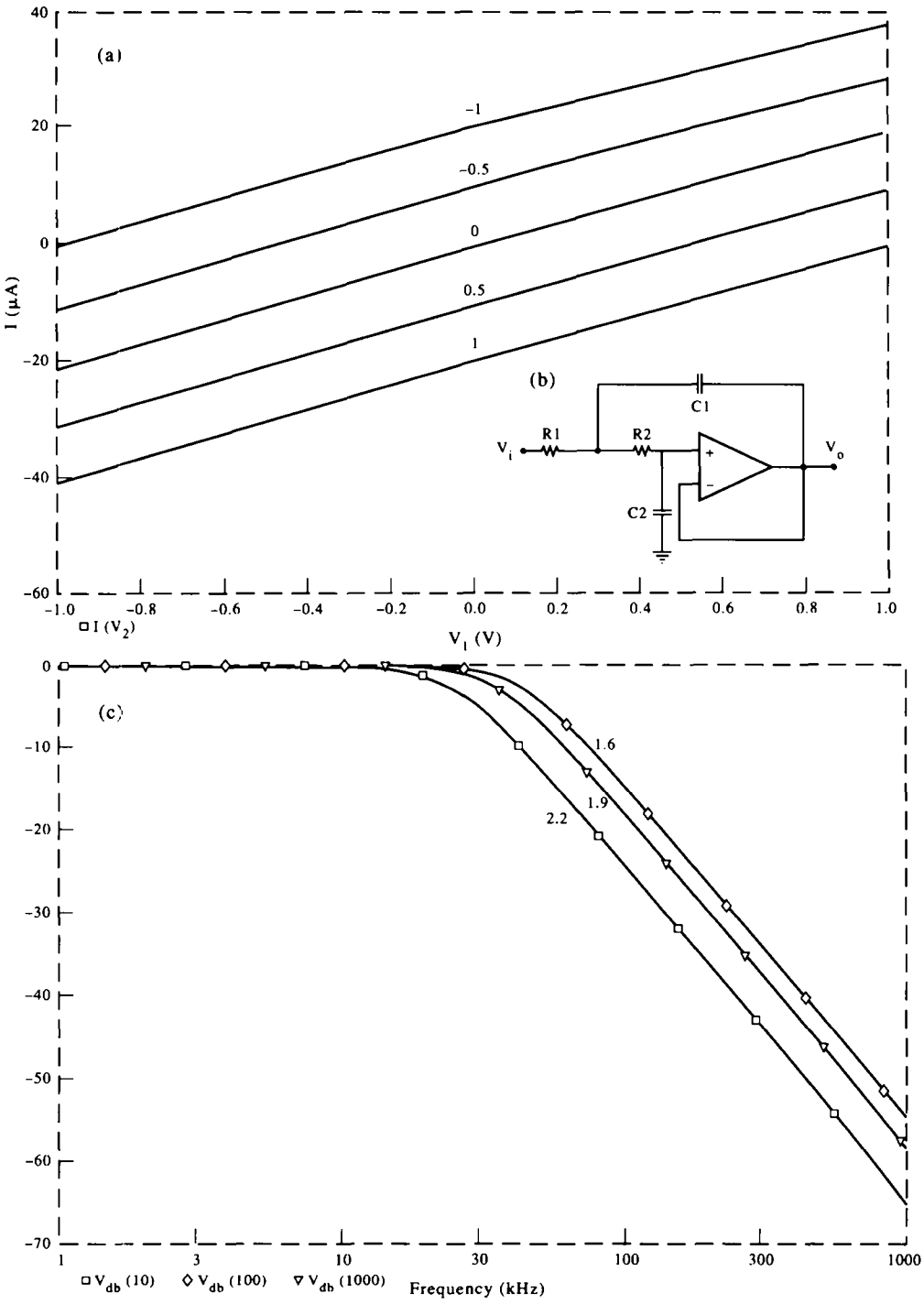

Fig. 6. (a) The *I–V* characteristics of the first proposed CMOS floating resistor. (b) Sallen and Key lowpass filter. (c) The magnitude response of the Sallen–Key lowpass filter with V_C as a parameter.

The currents of the transistors M5, M6 and M7 are equal and are given, respectively, by:

$$I_5 = \frac{K_5}{2}(V_1 - V_x - V_T)^2 \quad (56)$$

$$I_6 = \frac{K_6}{2}(V_x - V_b - V_T)^2 \quad (57)$$

$$I_7 = \frac{K_7}{2}(V_C - V_T)^2 \quad (58)$$

From the above equations and with K_5=K_6=$4K_7$, the output voltage is given by:

$$V_b = V_1 - V_C - V_T \quad (59)$$

The transistor M11 together with the biasing current from M10 form a negative feedback action which provides the necessary current from the output without changing the voltage.

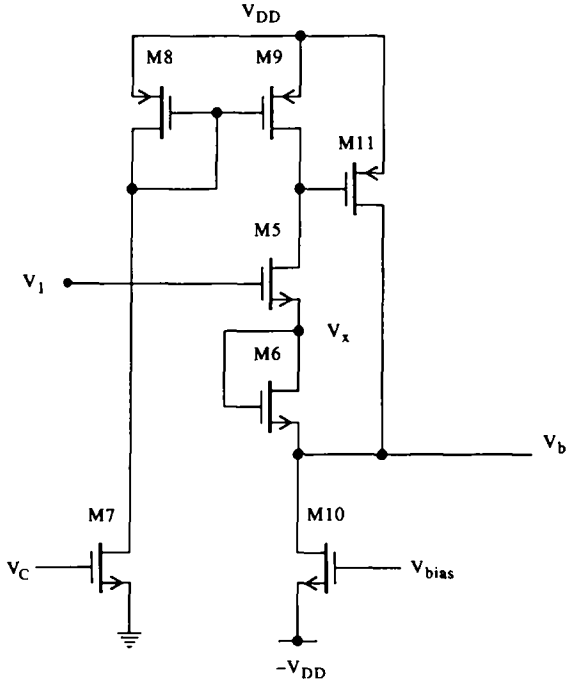

Fig. 7. The biasing circuit for the second proposed CMOS floating resistor.

Similarly, the biasing voltage V_a can be obtained using a similar MOS circuit to that shown in Fig. 7, and is given by:

$$V_a = V_2 - V_C - V_T \quad (60)$$

Therefore, the resistor current is obtained as:

$$I_i = I_o = 2KV_C(V_1 - V_2) \quad (61)$$

Therefore, the magnitude of the resistor is independent of the threshold voltage and the supply voltage and is given by:

$$R = \frac{1}{2KV_C} \quad (62)$$

The overall CMOS floating resistor circuit is shown in Fig. 8.

3.4.1. Range of operation

The range of operation of the second proposed CMOS floating resistor can be obtained provided that every MOS transistor in the CMOS resistor circuit satisfies eqs. (41) and (42) for NMOS transistors and eqs. (43) and (44) for PMOS transistors. The necessary conditions needed for all transistors to operate in the saturation region can be summarized as:

$$-V_C < V_1 - V_2 < V_C \quad (63)$$

For symmetrical and equal inputs, the above equation results in the following two equations controlling the range of operation:

$$\frac{-V_C}{2} < V_1 < \frac{V_C}{2} \quad (64)$$

$$\frac{-V_C}{2} < V_2 < \frac{V_C}{2} \quad (65)$$

and the condition on V_C is:

$$V_C > V_T \quad (66)$$

It is interesting to note that the magnitude of the resistor and its range of operation are controlled only by the control voltage.

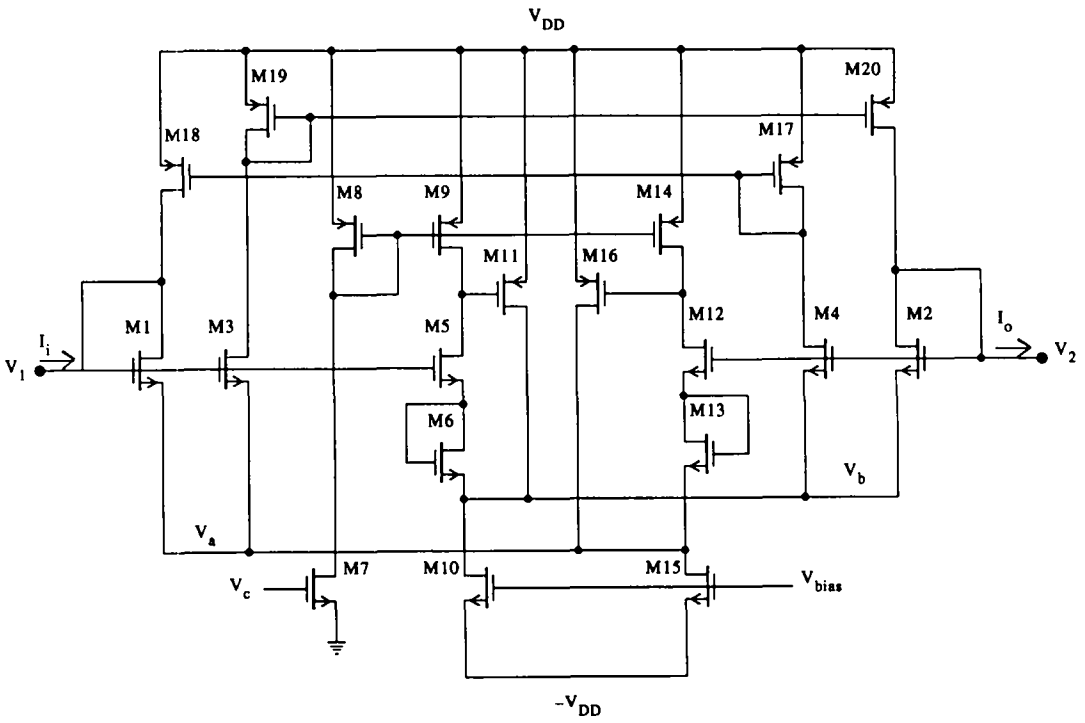

Fig. 8. The second proposed CMOS floating resistor circuit.

TABLE 2

MOS transistor	Aspect ratio (W μm/l μm)
M1, M2, M3, M4	4/25
M5, M6, M11, M12, M13, M16	16/4
M7	4/4
M8, M9, M14, M16, M17, M18, M19, M20	26/8
M10, M15	40/8

TABLE 3 Model parameters set for 2 μm CMOS technology (obtained through MOSIS)

.MODEL NMOS NMOS LEVEL-2 LD=0.225112U TIX=405.000001E−10 NSUB=2.256421E+15 VTO=0.77227
KP=4.954000E−05 GAMMA=1.0151 PHI=0.66 UO=581 UEXP=0.217142 UCRIT=115146 DELTA=1.360440
VMAX=68535.3 XJ=0.250000U NFS=2.85E+12 NEFF=1 NSS=1.000000E+10 TPG=1.000000 RSH=27.020000
CGDO=2.873845E−10 CGSO=2.880845E−10 CGBO=3.840832E−10 CJ=4.100000E−04 MJ=0.4650
CJSW=4.803300E−10 MJSW=0.351 PB=0.800000
.MODEL PMOS PMOS LEVEL−2 LD=0.177432U TOX=405.000001E−10 NSUB=3.956006E+15 VTO=−0.74048
KP=2.526000E−05 GAMMA=0.41251 PHI=0.6 UO=299.253 UEXP=0.1933 UCRIT=5462.67 DELTA=0.91285
VMAX=29720.9 XJ=0.250000U NFS=1.00E+11 NEFF=1 NSS=1.000000E+10 TPG=1.000000 RSH=107.40000
CGDO=2.262940E−10 CGSO=2.268940E−10 CGBO=3.471103E−10 CJ=1.898000E−04 MJ=0.439556
CJSW=2.2676E−10 MJSW=0.207266 PB=0.700000

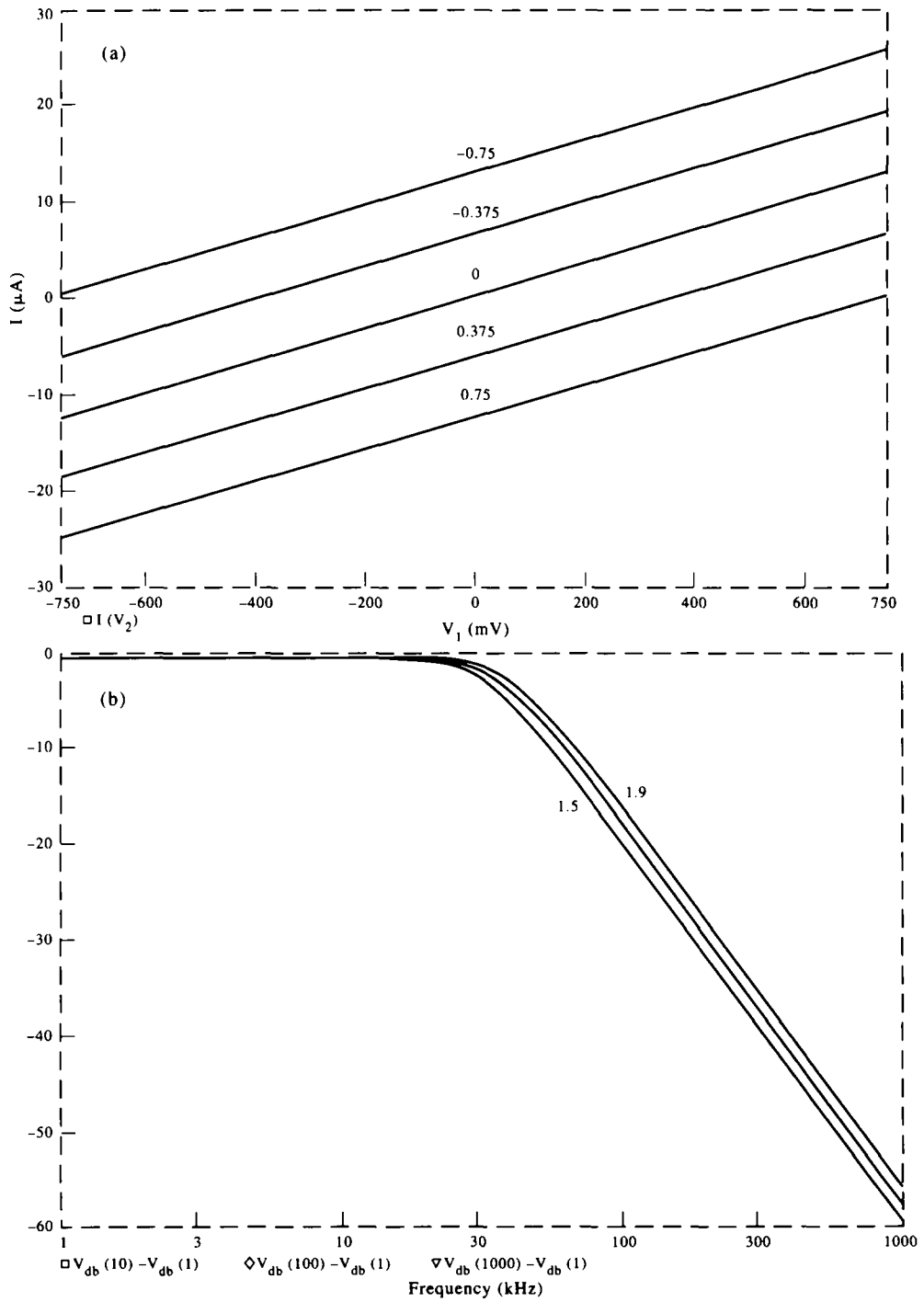

Fig. 9. (a) The I–V characteristics of the second proposed CMOS floating resistor. (b) The magnitude response of the Sallen-Key lowpass filter with V_C as a parameter.

TABLE 4

Floating resistor circuit	Figure	Reference	Configuration	m	E	No. of wells		No. of transistors		G
						N well	P well	NMOS	PMOS	
Sakurai–Ismail	2	11	1(a)	1	V_{DD}	0	7	14	6	$2K(V_{DD}-V_C)$
Elwan–Mahmoud–Soliman	3	12	1(b)	1	V_{DD}	3	4	7	8	$2K(V_{DD}-V_C)$
First proposed circuit	5	—	1(b)	0.5	$V_{DD}-\frac{V_T}{2}$	3	5	10	8	$K\left(V_{DD}-V_C-\frac{V_T}{2}\right)$
Second proposed circuit	8	—	1(a)	1	$2V_C$	0	6	11	9	$2KV_C$

3.4.2. Simulation results

PSpice simulation results for the second proposed CMOS floating resistor were carried out with the transistor aspect ratios as given in Table 2 and with supply voltages equal to ±3.3 V. The SPICE model parameters for the NMOS and PMOS transistors are listed in Table 3. Figure 9a represents the I–V characteristic of the resistor with control voltage V_C=1.25 V. V_1 and V_2 are scanned from −0.75 to 0.75 V. Figure 9c represents the magnitude response of the maximally flat magnitude Sallen and Key lowpass filter shown in Fig. 6b with C1=0.1414 nF and C2=0.0707 nF. The resistor magnitudes are controlled by the control voltage which is scanned from 1.5 to 1.9 V. The THD is less than 0.25% for a 1 MHz 1 V peak-to-peak sinusoidal input. The power consumption of each of the MOS resistors is less than 1.33 mW.

4. Conclusions

A method for generating voltage-controlled CMOS floating resistors is given. The CMOS floating resistors implemented are based on using MOS transistors operating in the saturation region with their sources connected to their substrates. The two CMOS floating resistors described in [11] and [12] are obtained as special cases based on the proposed generation method. Two other new CMOS floating resistors are proposed. The basic features of the four CMOS floating resistors discussed are summarized in Table 4, indicating the configuration used, the corresponding m and E values, the number of transistors used, the number of wells and the conductance value. The second proposed CMOS floating resistor is supply and threshold voltage independent. PSpice simulations of the two proposed CMOS floating resistors are included.

Acknowledgment

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