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A new CMOS realization of the differential difference amplifier and its application to a MOS-C oscillator

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A new CMOS realization of the differential difference amplifier (DDA) circuit is proposed. The DDA circuit is realized using a wide input range differential difference transconductor (DDT) and a complementary folded cascode (CFC) gain stage. The DDA circuit is used to realize a MOS-C oscillator suitable for VLSI with a simple circuit to control the amplitude of oscillation. PSpice simulation results for the proposed DDA circuit and the DDA based MOS-C oscillator are also given.

1. Introduction

The differential difference amplifier (DDA), first introduced by Sackinger and Guggenbuhl (1987), is a useful building block for continuous-time analogue signal processing, and was realized using the differential pair transconductors. In a closed loop operation, the DDA forces two differential voltages to the same value. A wide range DDA has been reported by Huang *et al.* (1993) using voltage to current converters with large signal handling capabilities. The DDA whose symbol is shown in Fig. 1(*a*), is an extension to the concept of the op.-amp, the main difference is that instead of two single-ended inputs, it has two differential input ports ($V_1 - V_2$) and ($V_3 - V_4$). The output voltage of the DDA can be written as

$$V_o = A_o\left[(V_1 - V_2) - (V_3 - V_4)\right] \tag{1}$$

where A_o is the open-loop gain of the DDA. When a negative feedback is introduced to V_2 and/or V_3, the basic equation that characterizes the operation of the DDA is obtained as

$$V_1 - V_2 = V_3 - V_4 \quad \text{with } A_o \to \infty \tag{2}$$

For a finite open-loop gain A_o, the difference between the two differential voltages increases as A_o decreases. Therefore, the open-loop gain should be as large as possible in order to achieve high performance operation. The proposed block diagram of the DDA is shown in Fig. 1(*b*) where the differential difference transconductor (DDT) converts the two differential voltages into a differential current, which is then amplified by the complementary folded cascode (CFC) gain stage introduced by Vallee and Elmasry (1994).

In this paper, a new CMOS realization of a programmable linear DDT circuit with large signal handling capabilities is given in § 2. In § 3, the overall DDA circuit using the proposed DDT circuit and the CFC gain stage is given. The application of

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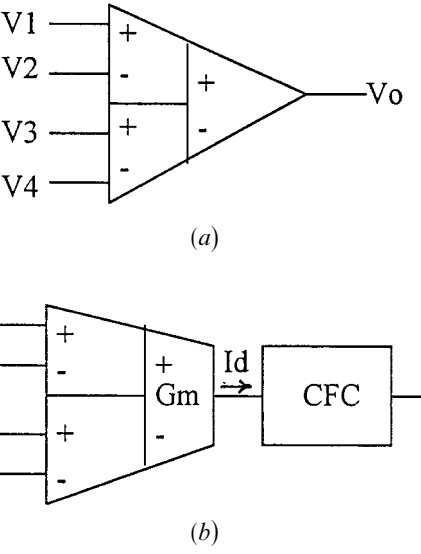


Figure 1. (*a*) The symbol of the DDA; (*b*) the block diagram of the DDA circuit.

the DDA circuit to realize a MOS-C oscillator suitable for VLSI with a simple circuit to control the amplitude of oscillation is presented in § 4. Simulation results using PSpice for the DDA circuit and the DDA-based MOS-C oscillator are also given.

2. The proposed DDT circuit

In this section, a new realization of the linear differential difference transconductor (DDT) whose transconductance can be tuned by a bias voltage V_B is introduced. The proposed design of the linear transconductor is based on the generation of intermediate voltages linearly proportional to the primary inputs, such that these voltages aid achieving a full linearity between the differential current of the basic transistors in the transconductor circuit and the input differential voltages.

Figure 2 represents the proposed DDT circuit with all transistors assumed to be operating in the saturation region with their sources connected to their substrates. The drain current of the NMOS transistor in the saturation region is given by

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2 \tag{3}$$

where $K = \mu_n C_{ox}(W/L)$; (W/L) is the transistor aspect ratio; μ_n is the electron mobility; C_{ox} is the gate oxide capacitance per unit area; and V_T is the threshold voltage (assumed the same for all MOS transistors).

Transistors M1 to M4 are assumed to be matched transistors and their currents are linearized using the four biasing circuits formed from the transistors M5 to M26.

First, expressions for the biasing voltages V_a, V_b, V_c and V_d in terms of V_1, V_2, V_3 and V_4 respectively are obtained.

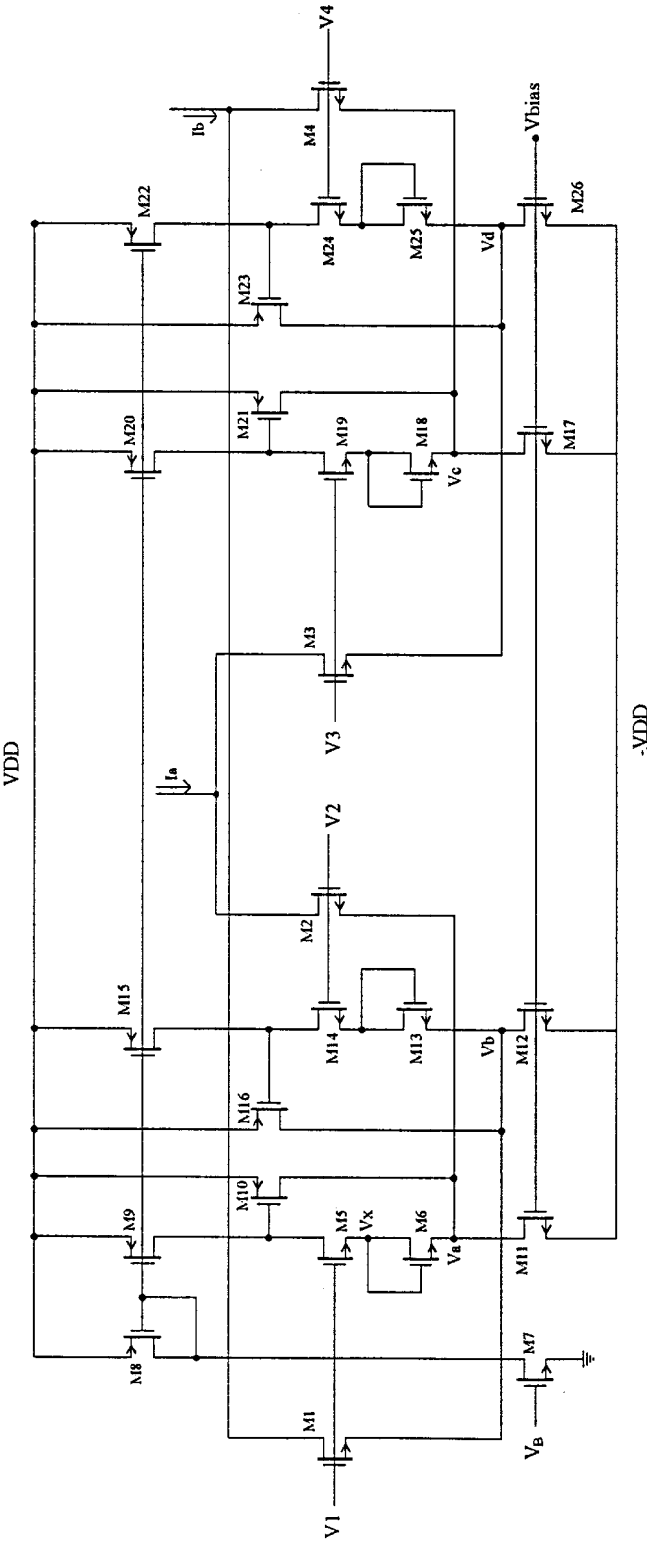


Figure 2. The proposed DDT circuit.

Consider the biasing circuit formed from M5 to M11, the currents of the transistors M5, M6 and M7 are equal and are given by

$$I_5 = \frac{K_5}{2}(V_1 - V_x - V_T)^2 \tag{4}$$

$$I_6 = \frac{K_6}{2}(V_x - V_a - V_T)^2 \tag{5}$$

$$I_7 = \frac{K_7}{2}(V_B - V_T)^2 \tag{6}$$

From the above equations and with $K_5 = K_6 = 4K_7$, the voltage V_a is given by

$$V_a = V_1 - V_B - V_T \tag{7}$$

The transistor M10 together with the biasing current from M11 form a negative feedback action which provides the necessary current from the output without changing the output voltage V_a.

Similar expressions for the biasing voltages V_b, V_c and V_d can be obtained and are given by

$$V_b = V_2 - V_B - V_T \tag{8}$$

$$V_c = V_3 - V_B - V_T \tag{9}$$

$$V_d = V_4 - V_B - V_T \tag{10}$$

Therefore, the currents flowing through M1 to M4 can be obtained and are given respectively by

$$I_1 = \frac{K}{2}(V_1 - V_2 + V_B)^2 \tag{11}$$

$$I_2 = \frac{K}{2}(V_2 - V_1 + V_B)^2 \tag{12}$$

$$I_3 = \frac{K}{2}(V_3 - V_4 + V_B)^2 \tag{13}$$

$$I_4 = \frac{K}{2}(V_4 - V_3 + V_B)^2 \tag{14}$$

The transconductor output current is given by

$$I_d = I_b - I_a = (I_1 + I_4) - (I_2 + I_3) \tag{15}$$

Substituting from (11) to (14) in (15), the transconductor output current is given as follows

$$I_d = G_m[(V_1 - V_2) - (V_3 - V_4)] \tag{16}$$

where

$$G_m = 2KV_B \tag{17}$$

Therefore, the CMOS circuit shown in Fig. 2 operates as a differential difference transconductor with a programmable transconductance G_m which is controlled by the bias voltage V_B.

Figure 3 shows the PSpice simulation results of the differential current of the DDT when (V1 and V4) are shorted and (V2 and V3) are also shorted and scanned

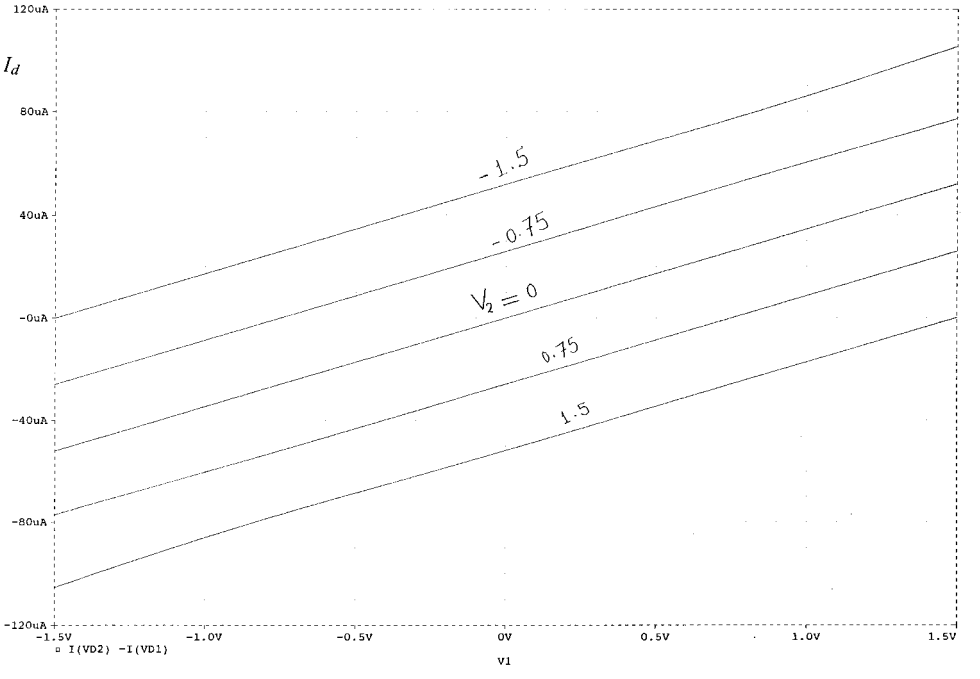


Figure 3. The differential current I_d of the proposed DDT circuit.

from - 1·5 V to 1·5 V with V_B = 1·8 V and the supply voltage V_{DD} = 5 V. The THD of a 1 V peak-to-peak 10 kHz input signal applied to DDT is less than 0·25%.

3. The overall DDA circuit

The overall DDA circuit using the proposed DDT circuit shown in Fig. 2 is shown in Fig. 4, where the two output currents of the DDT are subtracted and converted into a voltage with a high gain by using the complementary folded cascode amplifier (CFC). Transistors M35 and M36 provide a buffer with a low-output impedance. The buffer stage makes the operating point independent of the output current.

A simplified circuit model for the DDA is given in Fig. 5, as in the case of the op-amp (Sakurai and Ismail 1995) which is composed of ideal circuit elements, the input signal is the differential difference voltage $V_{id} = (V_2 - V_1) - (V_4 - V_3)$, which is applied across R_{in} (considered to be infinity). This voltage is converted into a current $G_m V_{id}$, where G_m is the transconductance of the DDT circuit. This current is converted into a voltage V_o by the gain stage whose equivalent output resistance and capacitance are R_o and C_o, respectively. The frequency dependent output voltage of the DDA is given by

$$V_o = \frac{\omega_t}{S + \omega_p}\left[(V_1 - V_2) - (V_3 - V_4)\right] \tag{18}$$

where $\omega_t = A_o \omega_p$ and ω_p and A_o for the DDA circuit are given by

$$\omega_p = \frac{1}{\{[g_{m30} r_{ds30} r_{ds28}] // [g_{m32} r_{ds32} r_{ds34}]\} C_{o1}} \tag{19}$$

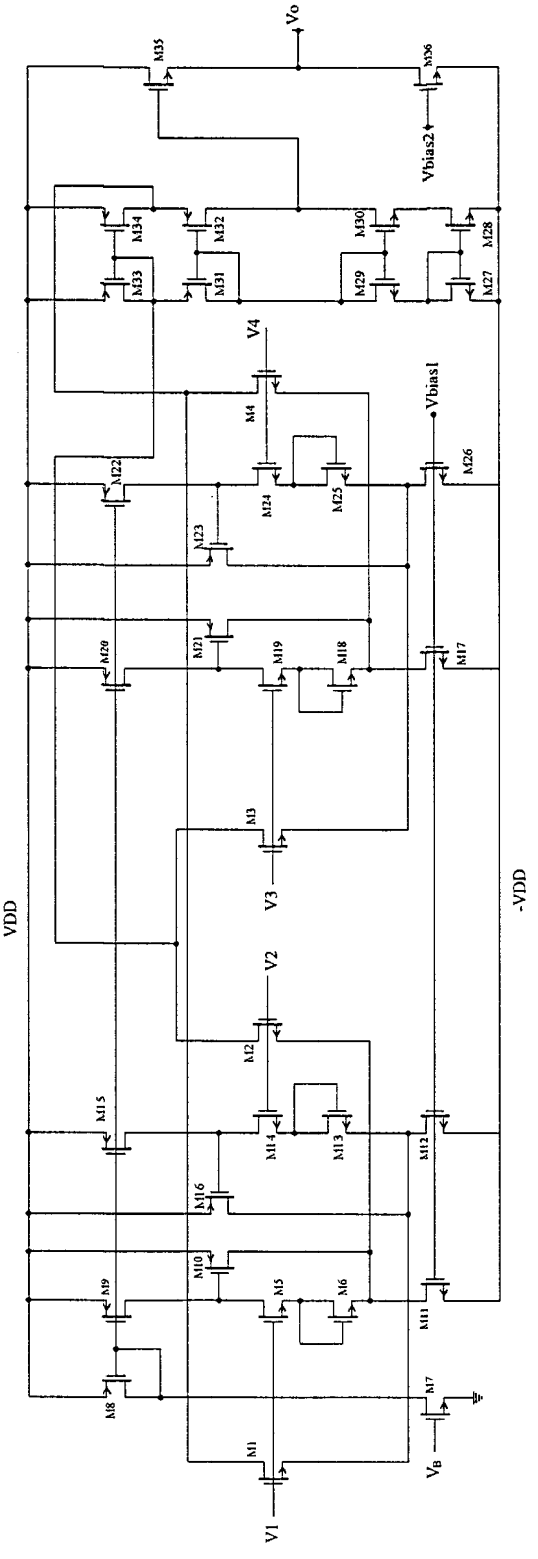


Figure 4. The proposed DDA circuit.

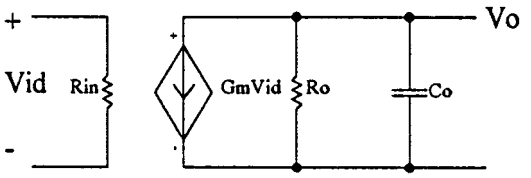


Figure 5. Simplified circuit model of the DDA circuit.

and

$$A_o = G_m \{[g_{m30} r_{ds30} r_{ds28}] // [g_{m32} r_{ds32} r_{ds34}]\} \quad (20)$$

The PSpice simulation results for the proposed DDA circuit with the transistor aspect ratios as given in Table 1, and the SPICE parameters given in Table 2 are summarized in Table 3.

MOS transistor	Aspect ratio (W μm/L μm)
M1, M2, M3, M4	2/20
M5, M6, M13, M14, M18, M19, M24, M25	16/4
M7	4/4
M10, M11, M12, M16, M17, M21, M23, M26	20/4
M8, M9, M15, M20, M22	30/4
M27-M34	160/10
M35, M36	200/4

Table 1. Transistor aspect ratios.

.MODEL NENH1 NMOS LD= 0·250000U TOX= 408·000001E- 10 NSUB= 6·264661E+ 15 VTO= 0·77527 KP= 5·518000E- 05 GAMMA= 0·5388 PHI= 0·6 UO= 652 UEXP= 0·100942 CRIT= 93790·5 DELTA= 1·000000E- 06 VMAX= 100000 XJ= 0·250000U LAMBDA= 2·752568E-03+ NFS= 2·06E+ 11 NEFF= 1 NSS= 1·000000E+ 10 TPG= 1·000000 RSH= 31·020000 CGDO= 3·173845E- 10 CGSO= 3·173845E- 10 CGBO= 4·260832E- 10 CJ= 1·038500E- 04 MJ= 0·649379 CJSW= 4·743300E- 10 MJSW= 0·326991 PB= 0·800000

.MODEL PENH1 PMOS LD= 0·213695U TOX= 408·000001E- 10+ NSUB= 5·574486E+ 15 VTO= - 0·77048 KP= 2·226000E- 05 GAMMA= 0·5083 PHI= 0·6 UO= 263·253 UEXP= 0·169026 UCRIT= 23481·2 DELTA= 7·31456 VMAX= 17079·4 XJ= 0·250000U LAMBDA= 1E- 02+ NFS= 2·77E+ 11 NEFF= 1·001 NSS= 1·000000E+ 10 TPG= - 1.000000 RSH= 88·940000 CGDO= 2·712940E- 10 CGSO= 2·712940E- 10 CGBO= 3·651103E- 10 CJ= 2·375000E- 04 MJ= 0·532556 CJSW= 2·707600E- 10 MJSW= 0·252466 PB= 0·800000

Table 2. SPICE parameters.

Parameter	Simulation results
DC power dissipation	10 mW
Input offset voltage	0·5 mV
DC gain	70 dB
Unity gain BW	10 MHz
Slew rate	16 V μS^{-1}
Input voltage range	- 2 V to 2 V
Output voltage range	- 2 V to 2 V

Table 3. PSpice simulation results.

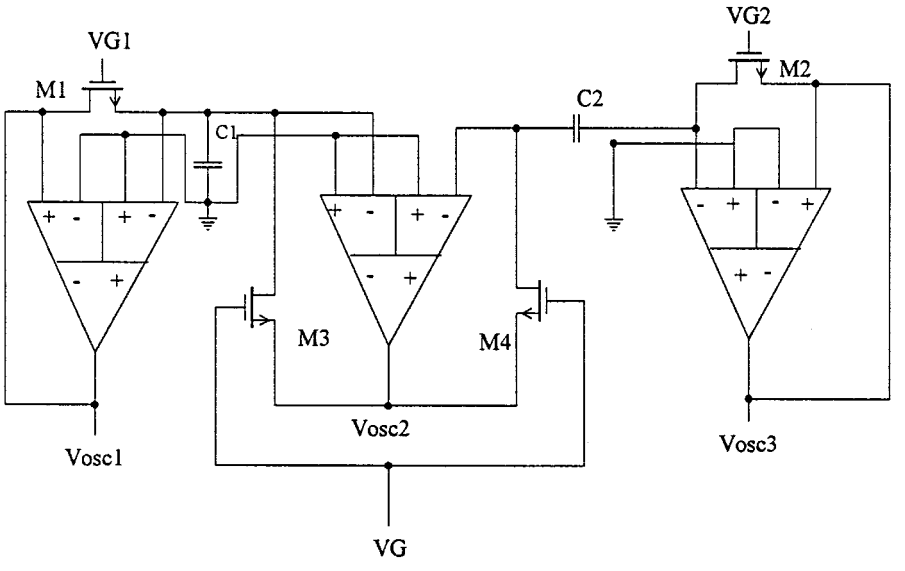


Figure 6. The DDA based MOS-C oscillator.

4. The DDA based MOS-C oscillator

According to Sackinger and Guggenbuul (1987), Zarabadi *et al.* (1992) and Huang *et al.* (1993) many interesting circuits can be realized with the DDA and without using components or matched components external to the DDA. In this section, the application of the DDA in realizing the MOS-C oscillator is presented. The DDA-MOS-C oscillator shown in Fig. 6 consists of a negative impedance converter (NIC), realized using a single DDA and two MOS transistors, two DDA-based voltage controlled resistors each realized using a single DDA and a MOS transistor operating in the non-saturation region, and two capacitors; where the condition of oscillation is given by

$$\frac{R_2}{R_1} + \frac{C_1}{C_2} = 1 \tag{21}$$

taking

$$\frac{R_2}{R_1} = \frac{C_1}{C_2} = \frac{1}{2} \tag{22}$$

The radian frequency of oscillation is given by

$$\omega_{osc} = \frac{1}{R_1 C_1} \tag{23}$$

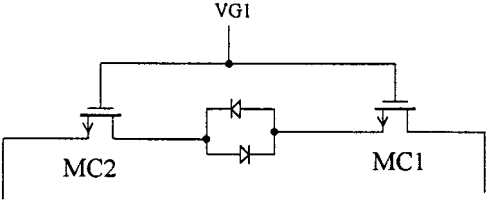
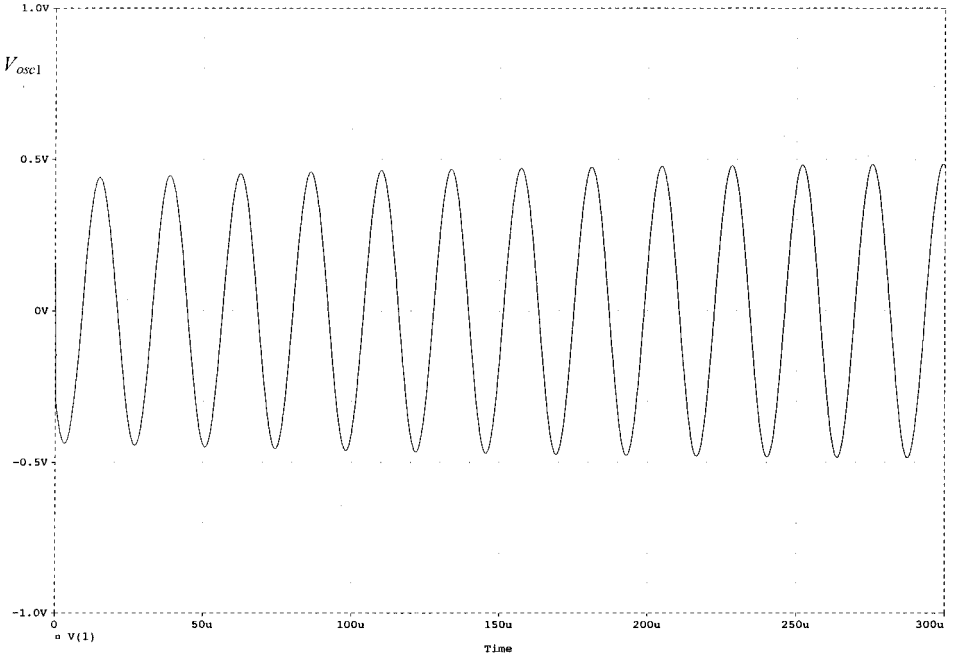
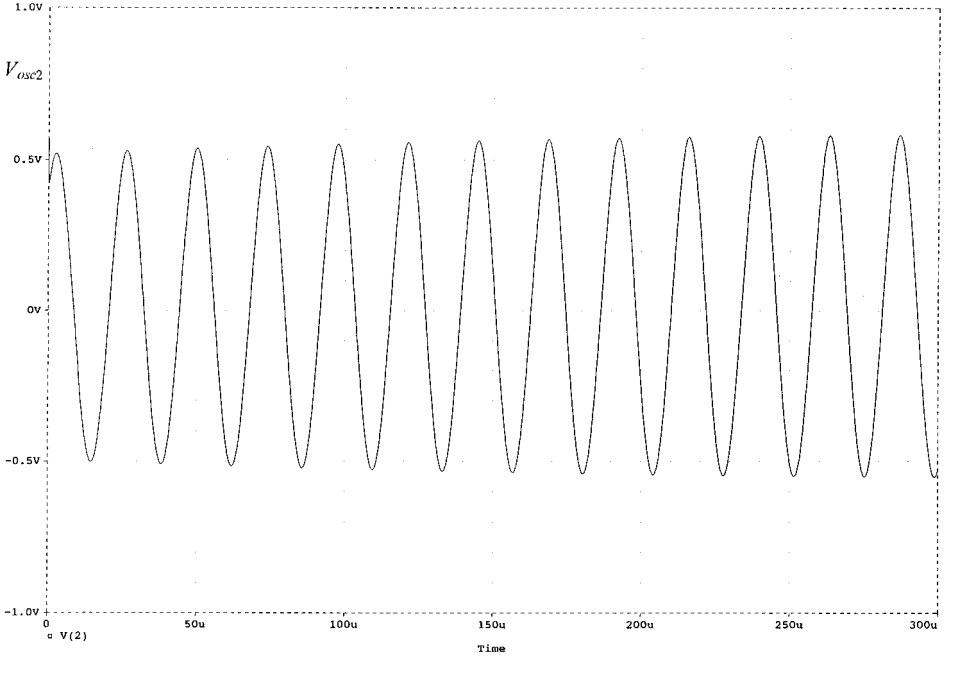


Figure 7. The control circuit.



8(*a*)



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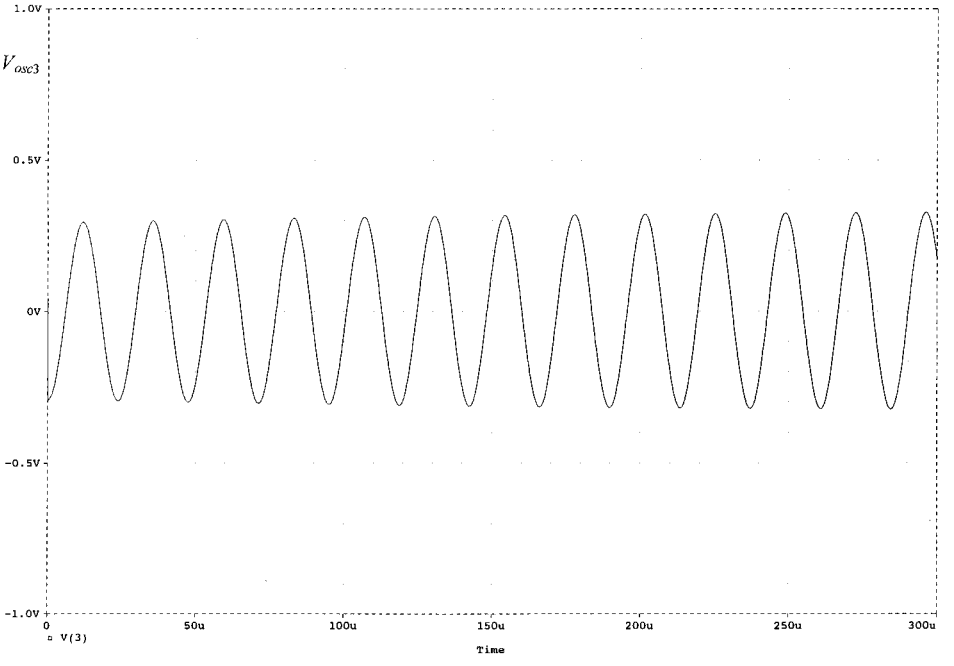

(*c*)

Figure 8. (*a*) The output waveform V_{osc1}; (*b*) the output waveform V_{osc2}; (*c*) the output waveform V_{osc3}.

where

$$R_1 = \frac{1}{2K_1(V_{G1} - V_T)} \quad \text{and} \quad R_2 = \frac{1}{2K_2(V_{G2} - V_T)} \tag{25}$$

Methods of amplitude control of voltage mode oscillators have been considered by some authors (Reddy 1972, Pyara *et al.* 1983). The main objective was to limit the amplitude of the voltage waveform in order to reduce the total harmonic distortion. In the DDA-MOS-C oscillator a simple method to control the amplitude of oscillation is proposed. Figure 7 represents the amplitude control circuit. The circuit employs two diodes and two MOS transistors operating in the ohmic region. The circuit is placed in parallel with the transistor M1. The amplitude of the output waveform can be controlled either by using a number of diodes in series or by changing the gate voltage V_G of the transistors M3 and M4 of the NIC.

MOS transistor	Aspect ratio ($W\,\mu m/L\,\mu m$)
M1	2/6
M2	2/3
M3, M4	28/6
MC1, MC2	2/5

Table 4. Aspect ratios.

Figures 8(*a*), 8(*b*) and 8(*c*) show the output waveforms of the oscillator given in Fig. 6 where the oscillation frequency is adjusted to 45·45 kHz. The aspect ratios of the DDA-based MOS-C oscillator transistors are given in Table 4. The capacitor's values are C1 = 0·5 nF and C2 = 1 nF and $V_{G1} = V_{G2} = V_G = 5$ V. Note that, V_{osc1} and V_{osc2} are out of phase and shifted only in magnitude by the voltage V_{DS3}.

5. Conclusions

A new CMOS realization of the DDA circuit has been proposed. The DDA is realized using a DDT circuit with large signal handling capabilities. Applications of the DDA in realizing the DDA-based MOS-C oscillator with a simple circuit to control the amplitude of oscillation have also been included.

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