INT. J. ELECTRONICS, 1997, VOL. 82, NO. 6, 605–620

A CMOS programmable balanced output transconductor for analogue signal processing

SOLIMAN A. MAHMOUD† and AHMED M. SOLIMAN†

A new CMOS programmable balanced output transconductor (BOTA) is introduced. The BOTA is a useful block for continuous-time analogue signal processing. A new CMOS realization of the BOTA is given. The proposed realization is based on the cascaded connection of a new voltage controlled differential transconductor, a voltage controlled MOS grounded resistor and a balanced output transconductor stage. Applications of the BOTA in realizing a floating resistor, a balanced output differential integrator, a continuous-time balanced output bandpass–lowpass filter, a floating inductor and the active realization of the RLC filters using a minimum number of the BOTA are given. PSpice simulation results for the BOTA circuit and for its applications are also given.

1. Introduction

Several realizations for the CMOS transconductors have been introduced in the literature. The realizations given by Khorramabadi and Gray (1984), Nedungadi and Viswanthan (1984), Seevink and Wassenaar (1987), Krummenacher and Joehl (1988), and Silva-Martinez *et al.* (1991) are based on using a differential stage with MOS transistors operating in the saturation region. The CMOS transconductors given by Pennock (1985), Tsividis *et al.* (1986), Wang (1989), Gopinathan *et al.* (1990) and Gatti *et al.* (1994) are based on the use of MOS transistors operating in the triode region. A transconductor with multiple outputs, which are simply current replicas obtained using current mirrors, was introduced by Ramirez-Angulo *et al.* (1992). This realization is based on using the well-known differential pair transconductor. The output current of the differential pair transconductor biased by a constant current source I_s is given by

$$I_d = \begin{cases} \left(KI_s\left(1 - K\dfrac{V_d^2}{4I_s}\right)\right)^{1/2} V_d & \text{for } |V_d| \le \left(\dfrac{2I_s}{K}\right)^{1/2} \quad (1a) \\ I_s & \text{for } |V_d| \ge \left(\dfrac{2I_s}{K}\right)^{1/2} \quad (1b) \end{cases}$$

where, V_d is the input differential voltage, and K is the transconductance parameter of each of the NMOS transistors of the differential pair transconductor.

For linear operation, I_d should be proportional to V_d only; however, the existence of the square root term results in the nonlinearity in I_d, which is defined as the percentage deviation from the ideal value $g_m V_d$, where g_m is the transconductance at $V_d = 0$ V, which is given by

Received 14 May 1996; accepted 31 October 1996.

†Electronics and Communications Engineering Department, Faculty of Engineering, Cairo University, Egypt. e-mail: asoliman@cairo.eun.eg.

$$g_m = (KI_s)^{1/2} \tag{2}$$

In addition, the magnitude of the transconductance is not controllable through a control voltage and therefore any changes in the transconductance value due to the fabrication process cannot be compensated. Also, the multiple outputs of this transconductor are obtained using current mirrors, therefore for accurate current transferring, cascode current mirrors must be used.

In this paper, a new CMOS implementation of a balanced output transconductor (BOTA), based on transistors operating in the saturation region, is given. The proposed BOTA can be programmed using two control voltages, which allows one to compensate for process parameter spreads in automatically tuned filters. The BOTA, whose symbol is shown in Fig. 1, has two input voltages and provides two balanced output currents through the two output terminals. The proposed block diagram of the BOTA is shown in Fig. 2 where the differential transconductor converts the difference between the two input voltages into a single ended current I_d which is then converted into a voltage V_d by a voltage-controlled MOS grounded resistor and then converted into two balanced currents through the balanced output transconductor stage without using current mirrors.

The CMOS realization of the BOTA is given in § 2. The applications of the BOTA in realizing a floating resistor, a balanced output differential integrator, a continuous-time bandpass–lowpass filter, a floating inductor and an active realization of a passive filter using a minimum number of the BOTAs are given in § 3. PSpice simulation results for the BOTA circuit indicating the linearity range, and for the proposed circuit applications which verify the analytical results, are also given.

2. The proposed balanced output transconductor circuit

The proposed CMOS balanced output transconductor circuit is shown in Fig. 3. Three basic parts of the transconductor can be distinguished. The first one is a new differential transconductor input stage formed from M1 to M12. This input stage

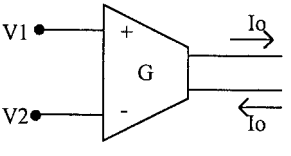

Figure 1. The proposed symbol of the BOTA.

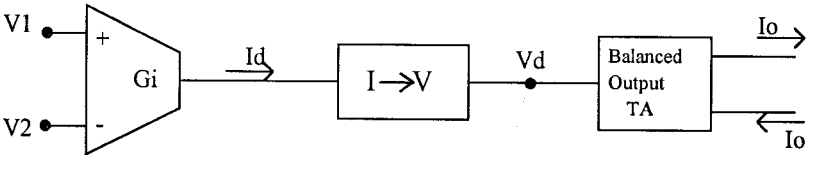

Figure 2. The proposed block diagram of the BOTA.

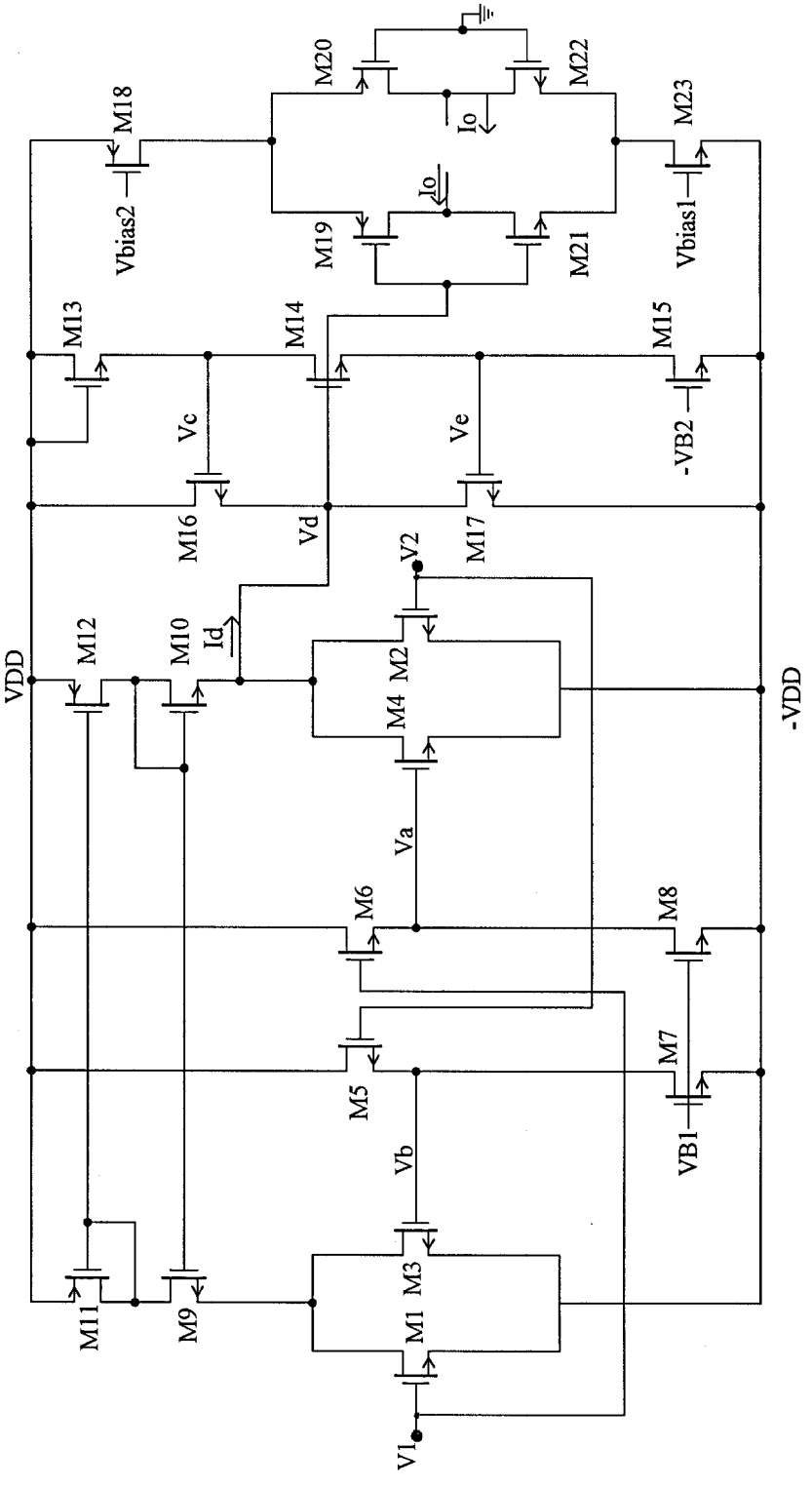

Figure 3. The BOTA circuit.

converts the difference between the two input voltages V_1 and V_2 into a single-ended current I_d. The second part of the transconductor which is formed from M13 to M17, realizes a new voltage controlled MOS grounded resistor which converts the current I_d to a voltage V_d. The voltage V_d is then converted into two balanced output currents through the transconductor output stage, which is formed from M18 to M23 and described by Arbel and Golding (1992). All transistors are assumed to be operating in the saturation region with their sources connected to their substrates. The drain current of the NMOS transistor in that region is given by

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2 \tag{3}$$

where $K = \mu_n C_{ox}(W/L)$; W/L is the transistor aspect ratio; μ_n is the electron mobility; C_{ox} is the gate oxide capacitance per unit area; and V_T is the threshold voltage (assumed the same for all NMOS transistors).

The input differential transconductor is based on the four matched transistors M1 to M4. Their drain currents are subtracted and transferred to the second stage through the transistors M9 to M12. The gates of the transistors M3 and M4 are biased by the two biasing circuits which are formed from M5 to M8. The two biasing circuits act to cancel the nonlinearities in the drain currents of the transistors M1 to M2.

First, expressions for the biasing voltages V_a and V_b in terms of V_1 and V_2 are obtained. Consider the biasing circuit formed from M6 to M8, the current flowing through M6 is given by

$$I_6 = \frac{K_6}{2}(V_1 - V_a - V_T)^2 \tag{4}$$

and the same current flowing through M8 is given by

$$I_8 = \frac{K_8}{2}(V_{B1} + V_{DD} - V_T)^2 \tag{5}$$

where V_{B1} is a control voltage. From (4) and (5) and by taking $K_6 = K_8$ the biasing voltage V_a is given by

$$V_a = V_1 - V_{B1} - V_{DD}$$

A similar expression for the biasing voltage V_b can be obtained and is given by

$$V_b = V_2 - V_{B1} - V_{DD} \tag{7}$$

Therefore, the currents flowing through the four matched transistors M1 to M4 can be obtained and are given by

$$I_1 = \frac{K_i}{2}(V_1 + V_{DD} - V_T)^2 \tag{8}$$

$$I_2 = \frac{K_i}{2}(V_2 + V_{DD} - V_T)^2 \tag{9}$$

$$I_3 = \frac{K_i}{2}(V_2 - V_{B1} - V_T)^2 \tag{10}$$

$$I_4 = \frac{K_i}{2}(V_1 - V_{B1} - V_T)^2 \tag{11}$$

where K_i is the transconductance parameter of each of the four matched transistors M1 to M4. The output current of the differential transconductor input stage I_d is given by

$$I_d = (I_1 + I_3) - (I_2 + I_4) \tag{12}$$

Substituting from (8) to (11) in (12), the transconductor output current I_d is given by

$$I_d = K_i(V_{B1} + V_{DD})(V_1 - V_2) \tag{13}$$

Therefore, the circuit formed from the transistors M1 to M12 simulates a linear differential transconductor stage with a transconductance controlled by the control voltage V_{B1} and is given by

$$G_i = K_i(V_{B1} + V_{DD}) \tag{14}$$

The output current of the differential transconductor input stage is the input current of the voltage controlled grounded MOS resistor formed from M13 to M17. The input current of the resistor I_d is given by

$$I_d = I_{17} - I_{16} \tag{15}$$

$$I_d = \frac{K_o}{2}\left[(V_e + V_{DD} - V_T)^2 - (V_c - V_d - V_T)^2\right] \tag{16}$$

where K_o is the transconductance parameter of each of the matched transistors M16 and M17. The circuit formed from M13 to M15 biases the gates of the MOS transistors M16 and M17 such that the circuit formed from M13 to M17 simulates a linear grounded resistor. Taking $K_{13} = K_{14} = K_{15}/4$, the biasing voltages V_c and V_e can be obtained and are given respectively by

$$V_c = 2V_{B2} - V_{DD} + V_T \tag{17}$$

$$V_e = V_d - 2V_{DD} + 2V_{B2} + V_T \tag{18}$$

By substituting from (17) and (18) in (16), the input current I_d in terms of V_d is given by

$$I_d = 2K_o(2V_{B2} - V_{DD})V_d \tag{19}$$

Therefore, the circuit formed from the transistors M13 to M17 simulates a voltage controlled grounded MOS resistor R, with magnitude given by

$$R = \frac{1}{2K_o(2V_{B2} - V_{DD})} \tag{20}$$

This MOS grounded resistor is a modified form of the voltage controlled MOS grounded resistor described by Elwan *et al.* (1995) to be threshold voltage independent.

From (13) and (19), the voltage V_d is thus given by

$$V_d = \frac{K_i(V_{B1} + V_{DD})}{2K_o(2V_{B2} - V_{DD})}(V_1 - V_2) \tag{21}$$

This voltage is then converted into two balanced output currents by the transconductor output stage formed from M18 to M23 (Arbel *et al.* 1992). Essentially, this stage is just two matched CMOS inverters biased by two current sources and operates as an analogue transconductor stage. In order to satisfy Kirchhoff's current law,

the output current from one of the inverters must equal the negative of the output current from the other inverter. This output current is given by (Arbel *et al.* 1992)

$$I_o = \tfrac{1}{2}(g_{m19} + g_{m21})V_d \tag{22}$$

where g_{m19} and g_{m21} are the p-channel and n-channel transconductances of the transistors M19 and M21. From (21) and (22), the output current of the proposed balanced output transconductor is given by

$$I_o = \frac{K_i(V_{B1} + V_{DD})(g_{m19} + g_{m21})}{4K_o(2V_{B2} - V_{DD})}(V_1 - V_2) \tag{23}$$

Therefore, the CMOS circuit in Fig. 3 operates as a balanced output transconductor with a programmable transconductance G, which is controlled by the voltages V_{B1} and V_{B2} and is given by

$$G = \frac{K_i(V_{B1} + V_{DD})(g_{m19} + g_{m21}}{4K_o(2V_{B2} - V_{DD})} \tag{24}$$

The performance of the proposed CMOS BOTA circuit was verified by PSpice simulations, with supply voltages ±5 V. The aspect ratios and the transistor's model parameters are given in Tables 1 and 2 respectively.

MOS transistor	Aspect ratio (W/L)
M1, M2, M3, M4	2/8
M5, M6, M7, M8	4/4
M9, M10	40/8
M11, M12	40/4
M13, M14	4/4
M15	16/4
M16, M17	2/6
M18, M23	200/4
M19, M20, M21, M22	40/4

Table 1. Aspect ratios.

.MODEL NMOS NMOS LEVEL= 2 LD= 0·225112U TOX= 405·000001E-10
NSUB= 2·256421E+ 15 VTO= 0·77227 KP= 4·954000E-05 GAMMA= 1·0151 PHI= 0·6
UO= 581 UEXP= 0·217142 UCRIT= 115146 DELTA= 1·360440 VMAX= 68535·3
XJ= 0·250000U NFS= 2·85E+ 12 NEFF= 1 NSS= 1·000000E+ 10 TPG= 1·000000
RSH= 27·020000 CGDO= 2·873845E-10 CGSO= 2·880845E-10 CGBO= 3·840832E-10
CJ= 4·100000E-04 MJ= 0·4650 CJSW= 4·803300E-10 MJSW= 0·351 PB= 0·800000

.MODEL PMOS PMOS LEVEL= 2 LD= 0·177432U TOX= 405·000001E-10
NSUB= 3·956006E+ 15 VTO= - 0·74048 KP= 2·526000E-05 GAMMA= 0·4251 PHI= 0·6
UO= 299·253 UEXP= 0·1933 UCRIT= 5462·67 DELTA= 0·91285 VMAX= 29720·9
XJ= 0·250000U NFS= 1·00E+ 11 NEFF= 1 NSS= 1·000000E+ 10 TPG= - 1·000000
RSH= 107·40000 CGDO= 2·262940E-10 CGSO= 2·268940E-10 CGBO= 3·471103E-10
CJ= 1·898000E= 04 MJ= 0·439556 CJSW= 2·267600E-10 MJSW= 0·207266 PB= 0·700000

Table 2. Model parameters set for 2 μm CMOS technology (obtained through MOSIS).

The output current I_o of the BOTA versus V_1 for various values of V_2 where V_1 and V_2 are scanned from - 1·5 V to 1·5 V with V_{B1} = - 3·4 V and V_{B2} = 3·9 V is shown in Fig. 4.

The output current I_o of the BOTA versus V_1 when V_2 is grounded and V_{B1} is scanned from - 3 V to - 4 V indicating the programmability of the BOTA with V_{B1} as a control parameter and taking V_{B2} = 3·7 V is shown in Fig. 5.

Also the output current I_o of the BOTA versus V_1 when V_2 is grounded and V_{B2} is scanned from 3 V to 4 V, indicating the programmability of the BOTA, with V_{B2} as a control parameter and taking V_{B1} = - 3·7 V is shown in Fig. 6.

3. Applications of the BOTA

In the following subsections, the applications of the BOTA in realizing a floating resistor, a balanced output differential integrator, a continuous-time balanced output bandpass–lowpass filter, a floating inductor and the BOTA-C active realization of RLC filters using a minimum number of the BOTAs are given. The PSpice simulation results are also given to verify the analytical results.

3.1. *The BOTA-based floating resistor*

Resistors implemented by MOS transistors find many useful applications in modern analogue VLSI signal and information processing. This is because linear passive resistors require a large area and cannot be electronically programmed to compensate for spread in their absolute values caused by random process variations

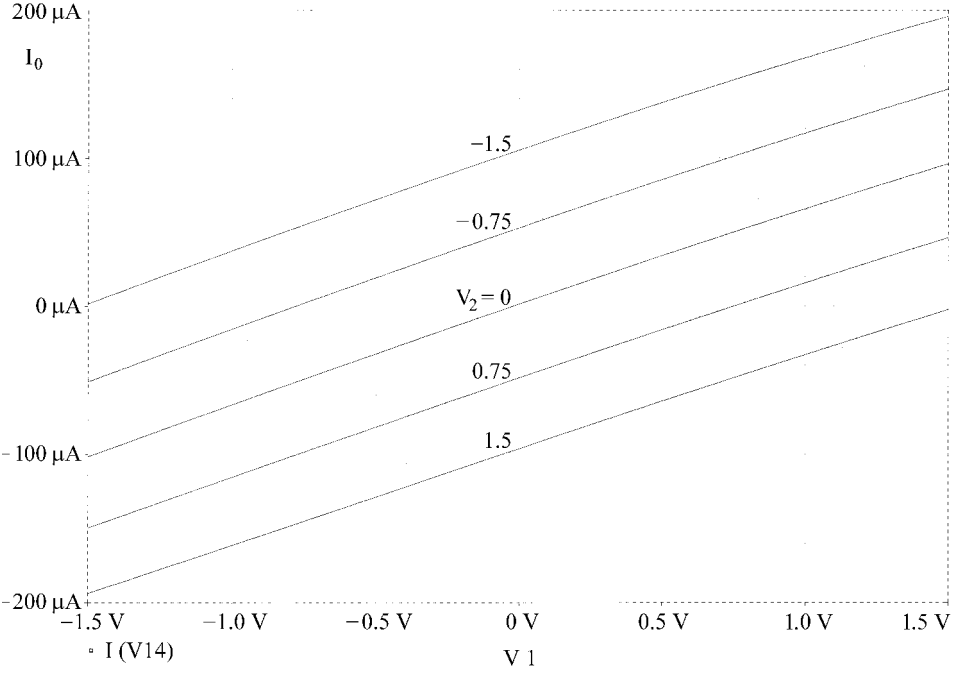

Figure 4. The output current of the BOTA.

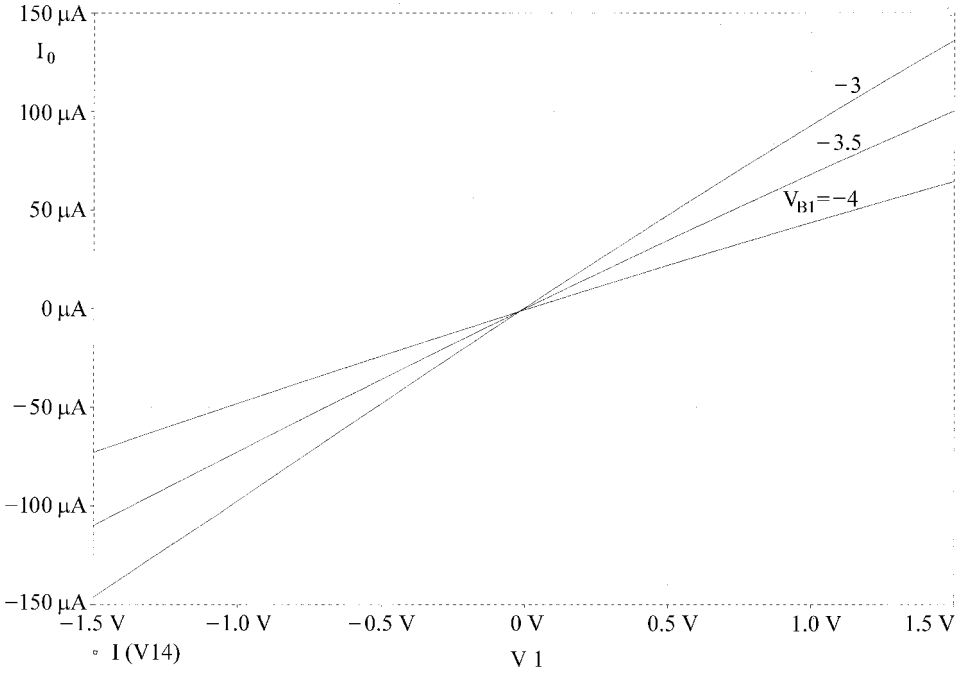

Figure 5. The output current of the BOTA with V_{B1} as a control parameter.

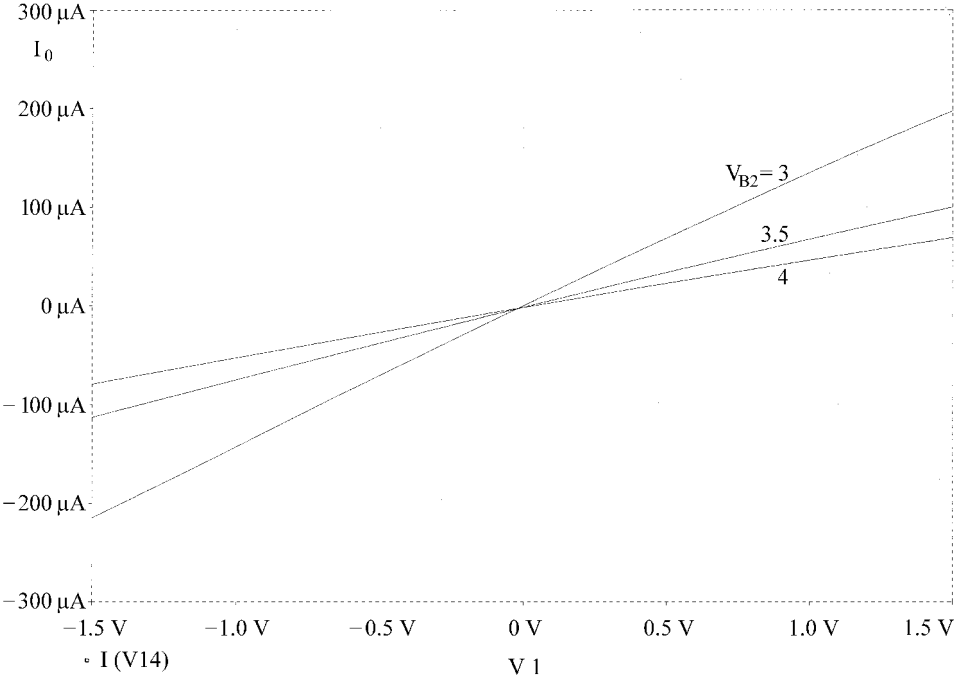

Figure 6. The output current of the BOTA with V_{B2} as a control parameter.

(Sakurai and Ismail 1992). A direct application of the BOTA is to implement a voltage controlled floating resistor as shown in Fig. 7 where the current flowing through the resistor is given by

$$I_1 = I_2 = G(V_1 - V_2) \tag{25}$$

Thus, the resistor magnitude is given by

$$R = \frac{1}{G} = \frac{4K_o(2V_{B2} - V_{DD})}{K_i(V_{B1} + V_{DD})(g_{m19} + g_{m21})} \tag{26}$$

The PSpice simulation results of the *I- V* characteristics of the floating resistor are shown in Fig. 8 where the voltages V_1 and V_2 are scanned from - 1 V to 1 V and the control voltages V_{B1} = - 3·4 V, V_{B2} = 3·9 V.

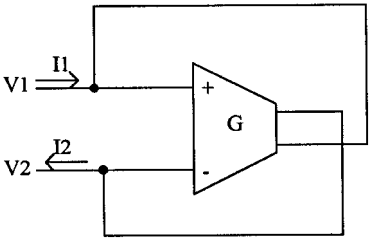

Figure 7. The BOTA-based floating resistor.

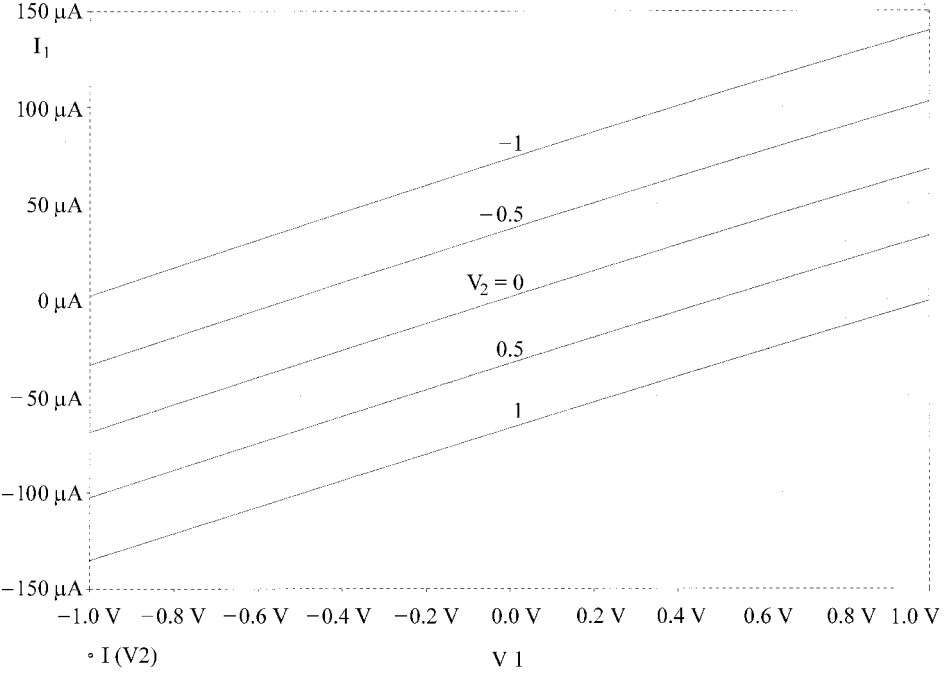

Figure 8. The *I- V* characteristics of the floating resistor.

3.2. *The BOTA-balanced output differential integrator*

Figure 9 shows the BOTA-based differential integrator. The differential integrator has a high input impedance since the inputs of the circuit are directly the inputs of the BOTA circuit (gates of MOS transistors). In addition, the differential integrator has an output in the balanced form. The output of the integrator is given by

$$V_o = \frac{G}{Sc}(V_1 - V_2) \tag{27}$$

Figure 10 shows the PSpice simulation results of the integrator outputs with a square wave input of 1 V peak-to-peak amplitude and a frequency of 5 kHz.

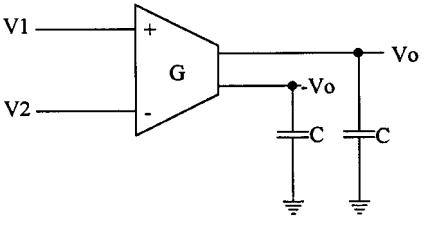

Figure 9. The BOTA-based balanced output differential integrator.

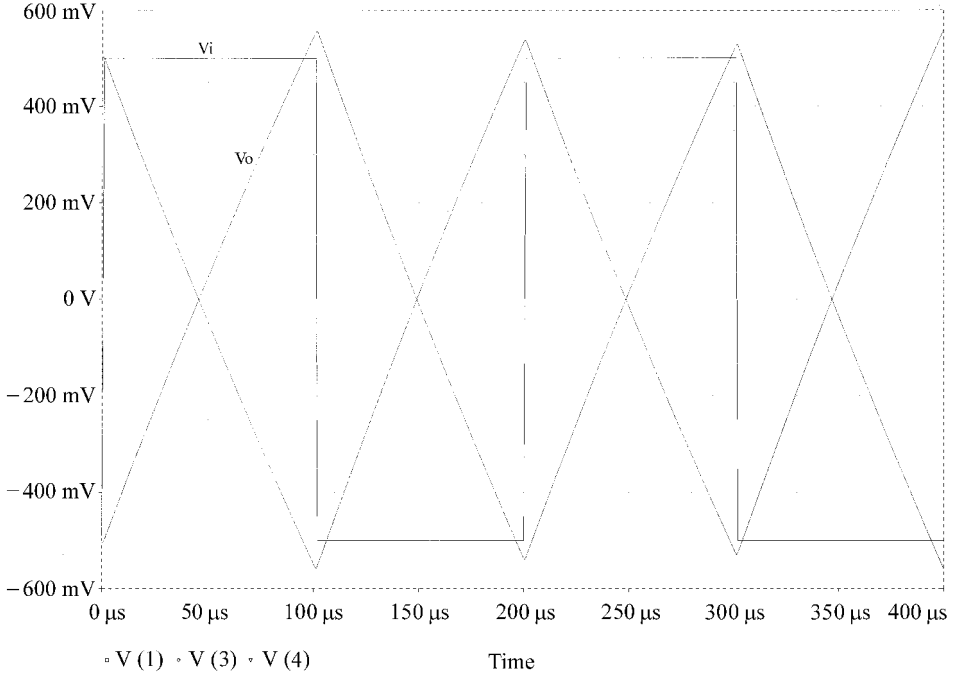

Figure 10. The input and the balanced outputs of the BOTA integrator.

3.3. *The BOTA-C balanced output bandpass–lowpass filter*

Any active filter implementation requires basic functions such as integration, lossy integration and addition (Soliman 1979). The addition–subtraction in the BOTA-C filters is achieved by simply connecting the output of the transconductors that deliver the signals to be summed. An example of the use of the BOTA integrator in the realization of an active filter is shown in Fig. 11. The filter has bandpass and lowpass outputs in a balanced form. The transfer functions of the bandpass and the lowpass outputs are given by

$$\frac{V_{BP}}{V_i} = \frac{\frac{SG_1}{C_1}}{D(S)} \tag{28}$$

$$\frac{V_{LP}}{V_i} = \frac{\frac{G_1 G_3}{C_1 C_2}}{D(S)} \tag{29}$$

where

$$D(s) = S^2 + S\frac{G_2}{C_1} + \frac{G_2 G_3}{C_1 C_2} \tag{30}$$

$$o_0 = \left(\frac{G_1 G_3}{C_1 C_2}\right)^{1/2} \text{ and } Q = \frac{\left(\frac{C_1}{C_2} G_1 G_3\right)^{1/2}}{G_2} \tag{31}$$

To simplify the design, let $G_1 = G_3 = G$ and $C_1 = C_2 = C$. As a result $o_o = G/C$ and $Q = G/G_2$. Therefore, high Q can be realized by increasing the G/G_2 ratio which can be achieved by programming both G and G_2 through the control voltages of the

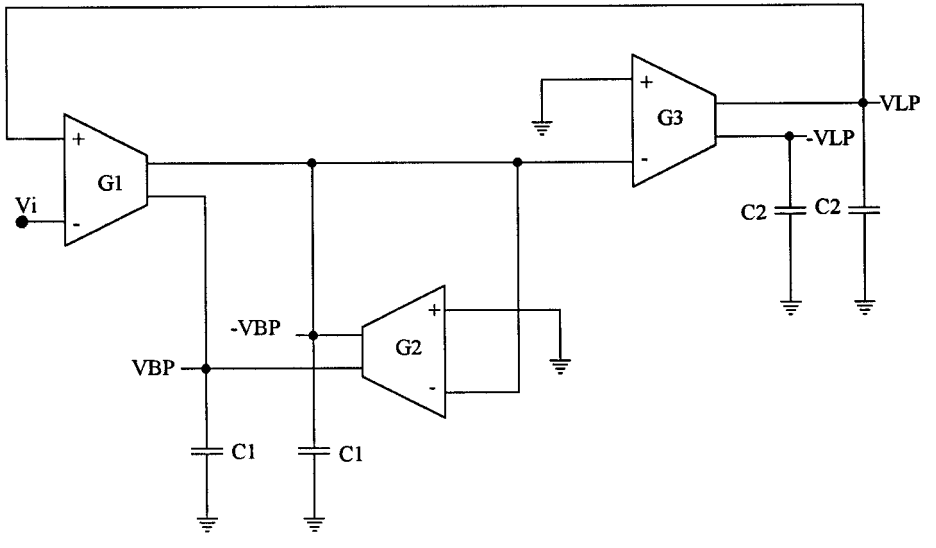

Figure 11. The BOTA-based balanced output bandpass–lowpass active filter.

BOTA circuit. The PSpice simulation results of the active filter with $G_1 = G_2 = G_3 = 65\,\mu A\,V^{-1}$ and $C_2 = 2C_1 = 0{\cdot}28\,nF$ to obtain a maximally flat magnitude characteristic of the lowpass filter are shown in Figs 12 and 13 indicating both magnitude and phase of the balanced output lowpass filter. The simulation results of the bandpass characteristics with $C_1 = C_2 = 0{\cdot}1\,nF$, $G_1 = G_3 = G = 65\,\mu A\,V^{-1}$ and $G_2 = G/4 = 16{\cdot}25\,\mu A\,V^{-1}$ to provide $Q = 4$ are shown in Figs 14 and 15 indicating the magnitude and phase of the balanced output bandpass filter.

3.4. *The BOTA-based floating inductor*

A voltage controlled floating inductor can also be realized by using the BOTA. The BOTA-based floating inductor circuit is shown in Fig. 16. The input and the output currents of the circuit are equal and are given by

$$I_1 = I_2 = \frac{G_1 G_2}{SC}(V_1 - V_2) \tag{32}$$

Therefore, the circuit realizes a floating inductor of magnitude given by

$$L = \frac{C}{G_1 G_2} \tag{33}$$

Since both G_1 and G_2 are programmable, the circuit shown in Fig. 16 provides a voltage controlled floating inductor.

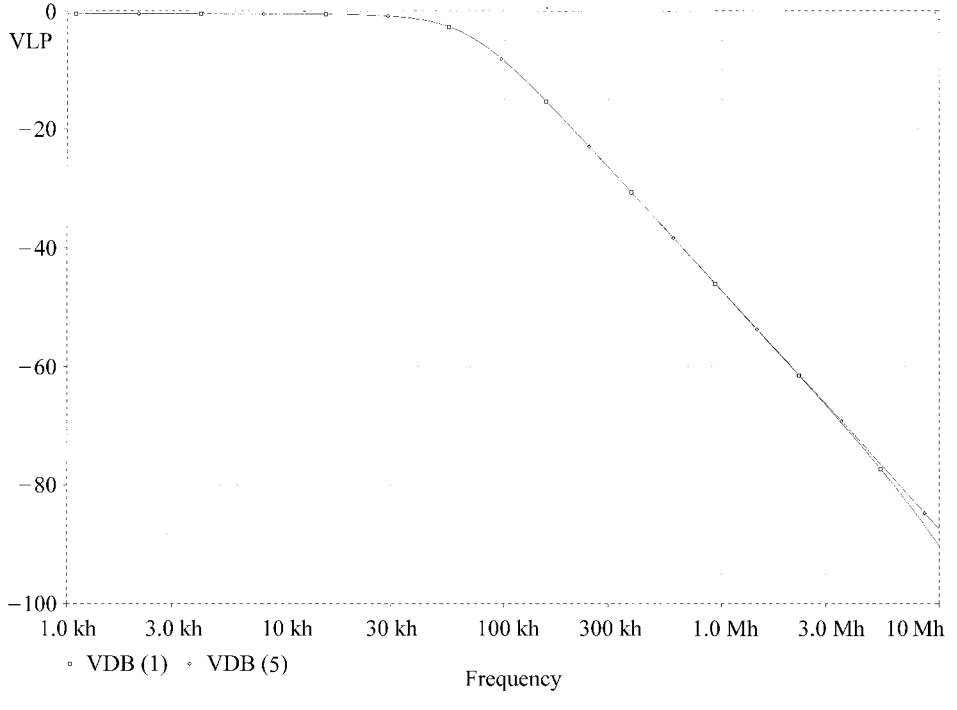

Figure 12. The magnitude response of the lowpass filter outputs.

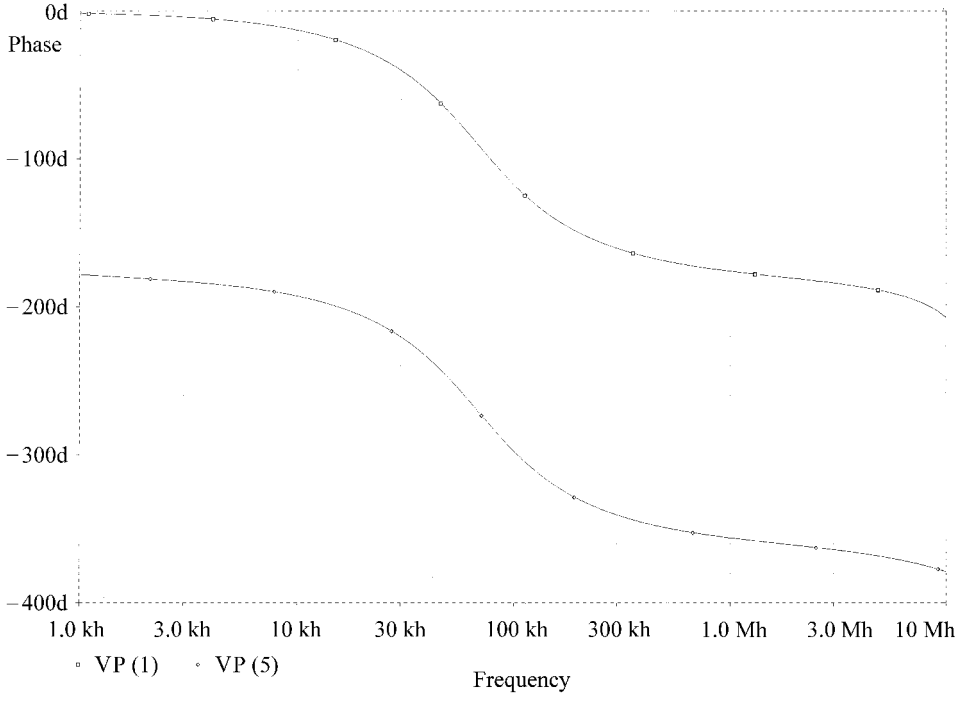

Figure 13. The phase response of the lowpass filter outputs.

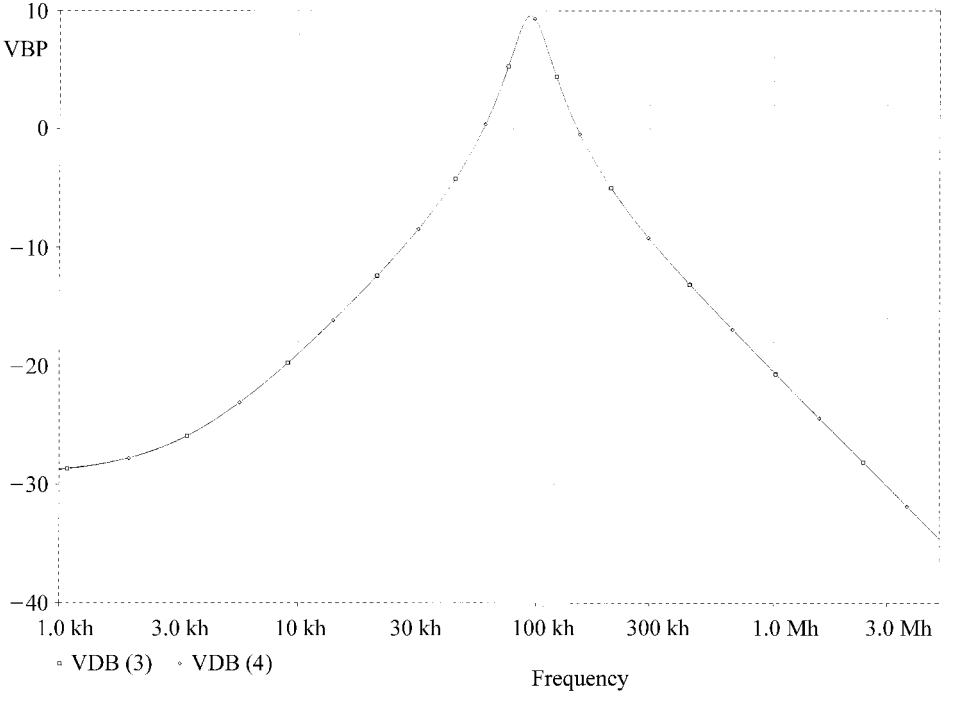

Figure 14. The magnitude response of the bandpass filter outputs.

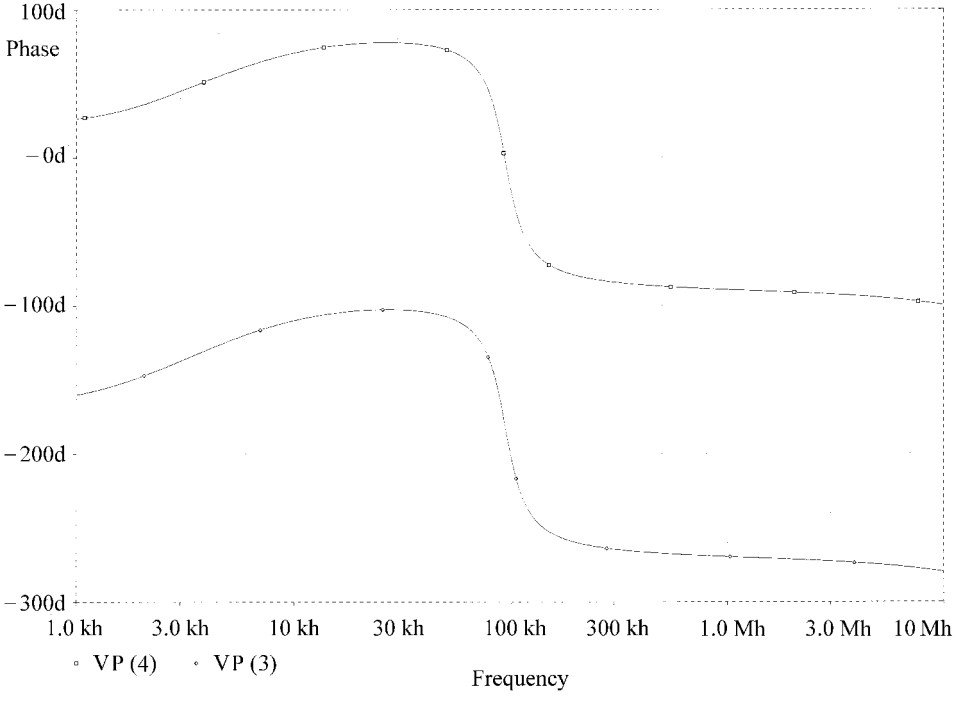

Figure 15. The phase response of the bandpass filter outputs.

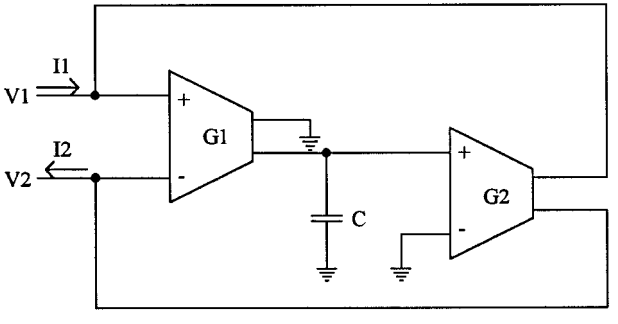

Figure 16. The BOTA-based floating inductor circuit.

3.5. *The BOTA-C active realization of the RLC filters*

The BOTA can be used to obtain active filter implementation of a passive filter using the minimum number of BOTAs. The transconductor-C synthesis given by de Queiroz *et al.* (1988), Caloba *et al.* (1989), and Hwang *et al.* (1994) for active realization of the high-order LC ladder filters are subject to complicated design procedures and need a large number of transconductors. In this section, a direct method to realize any RLC filter is introduced. The method depends on the one-to-

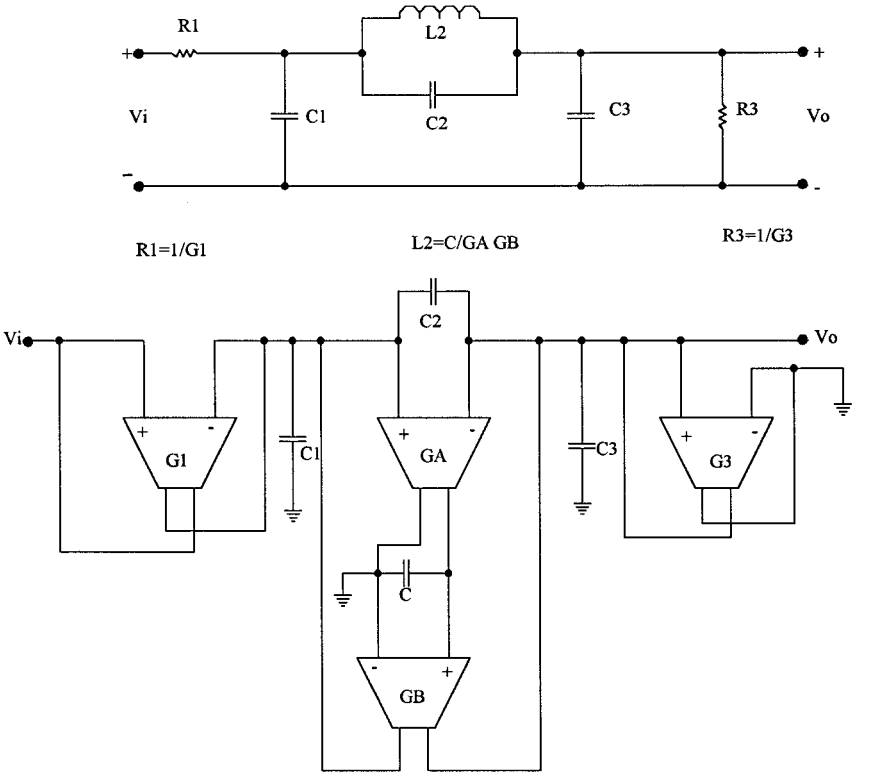

Figure 17. A third-order LCR filter and the corresponding active BOTA-C realization.

one replacement of every R and L by their equivalent active circuit. The implementations of a floating resistor and a floating inductor by using the BOTA have been discussed in previous sections. To indicate the simplicity of this method and its minimum requirements of the BOTAs, a third-order LC elliptic lowpass filter is realized. Figure 17 shows a third-order LC filter and its corresponding BOTA-C filter obtained by one-to-one replacement of the resistors and the floating inductor with the corresponding BOTA equivalent circuit. The required number of the BOTAs is only four, this comes from the ability of the BOTA block to implement a floating resistor and a floating inductor with the minimum number of the BOTAs. However, by using the single output transconductors, as given by de Queiroz *et al.* (1988), Caloba *et al.* (1989), and Hwang *et al.* (1994) a larger number of transconductors (seven to nine) is needed.

4. Conclusions

A new CMOS programmable balanced output transconductor has been proposed. The BOTA is realized using a new differential transconductor, MOS grounded resistor and a balanced output transconductor stage. Several applications of the BOTA in analogue signal processing are given. PSpice simulation results for the proposed circuit and for the proposed applications which confirm the analytical results are given.

References

Arbel, A. F., and Goldminz, L., 1992, Output stage for current-mode feedback amplifiers, theory and applications. *Analog Integrated Circuits and Signal Processing*, **2**, 243–255.

Caloba, L. P. and De Queiroz, A. C. M., 1989, OTA-C simulation of passive filters via embedding. *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1083–1086.

Caloba, L. P., De Queiroz, A. C. M., and Sanchez-Sinencio, E., 1989, Signal flow graph OTA-C band-reject integrated filters. *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1624–1627.

De Queiroz, A. C. M., Caloba, L. P., and Sanchez-Sinencio, E., 1988, Signal flow graph OTA-C integrated filters. *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2165–2168.

Elwan, H. O., Mahmoud, S. A., and Soliman, A. M., 1995, VC square-law grounded MOS resistor. *Electronic Engineering*, **67**, 34–38.

Gatti, U., Maloberti, F., Palmisano, G., and Torelli, G., 1994, CMOS triode-transistor transconductor for high-frequency continuous-time filters. *Proceedings of the Institution of Electrical Engineers: Circuits Devices System*, **141**, 462–468.

Gopinathan, V., Tsividis, Y., Tan, K., and Hester, R., 1990, Design consideration for high frequency continuous-time filters and implementation of antialiasing filter for digital video. *IEEE Journal of Solid-state Circuits*, **25**, 1368–1378.

Hwang, Y.-S., Liu, S.-I, Wu, D.-S., and Wu, Y.-P., 1994, Table-based linear transformation filters using OTA-C techniques. *Electronics Letters*, **30**, 2021–2022.

Khorramabadi, H., and Gray, P. R., 1984, High-frequency CMOS continuous-time filters. *IEEE Journal of Solid-state Circuits*, **19**, 939–948.

Krummenacher, F., and Joehl, N., 1988, A 4 MHz CMOS continuous-time filter with on chip automatic tuning. *IEEE Journal of Solid-state Circuits*, **23**, 750–758.

Nedungadi, A., and Viswanthan, T. R., 1984, Design of linear CMOS transconductor elements. *IEEE Transactions on Circuits and Systems*, **31**, 891–894.

Pennock, J. L., 1985, CMOS triode transconductor for continuous-time active integrated filters. *Electronics Letters*, **21**, 817–818.

Ramirez-Angulo, J., Robinson, M., and Sanchez-Sinencio, E., 1992, Current mode continuous-time filters: two design approaches. *IEEE Transactions on Circuits and Systems—II*, **39**, 337–341.

Sakurai, S., and Ismail, M., 1992, A CMOS Square-law programmable floating resistor independent of the threshold voltage. *IEEE Transactions on Circuits and Systems—II*, **39**, 565–574.

Seevink, E., and Wassenaar, R. F., 1987, A versatile CMOS linear transconductance/square-law function circuit. *IEEE Journal of Solid-state Circuits*, **22**, 366–377.

Silva-Martinez, J., Steyaert, M. S. J., and Sansen, W., 1991, A large signal very low-distortion transconductor for high frequency continuous-time filters. *IEEE Journal of Solid-state circuits*, **26**, 946–955.

Soliman, A. M., 1979, A new active C differential input integrator using the DVCCS/DVCVS. *International Journal of Circuit Theory and Applications*, **7**, 272–275.

Tsividis, Y., Czarnul, Z., and Fang, S. C., 1986, MOS transconductors and integrators with high linearity. *Electronics Letters*, **22**, 245–246.

Wang, S. L., 1989, Novel drain-biased transconductance building blocks for continuous-time filter applications. *Electronics Letters*, **25**, 100–101.