A Linear Transconductor / Multiplier Using a Matched Pair of MOS Transistors and a Current Conveyor

Eine lineare Transkonduktanz/Multiplizierer-Schaltung mit einem Paar von gleichen MOS-Transistoren und einem Stromwandler

By Ahmed M. Soliman*

Abstract:
A linear transconductor element is given. It is shown that full nonlinearity cancellation is achieved using only two matched MOS transistors and a single current conveyor. The proposed circuit has the attractive feature that by interchanging one MOS transistor with the current conveyor, the circuit reallizes a grounded resistor. The proposed cell is also suitable for use as a voltage multiplier with a linear output current.

Übersicht:
Ein lineares Transkonduktanzelement wird vorgestellt. Es wird gezeigt, daß in der vorgeschlagenen Schaltung bei Verwendung von nur zwei gleichen MOS-Transistoren und einem Stromwandler (Current Conveyor) vollständige Aufhebung der Nichtlinearität erreicht wird. Diese Schaltung entspricht nach Vertauschen eines MOS-Transistors mit dem Stromwandler einem geerdeten Widerstand. Sie eignet sich auch als Spannungsmultiplizierer mit linearem Ausgangsstrom.

Für die Dokumentation:
Transkonduktanz / Multiplizierer / Stromwandler (Current Conveyor) / steuerbarer Widerstand

The V-I converter which is also known as the transconductance element is a useful building block in analog circuits. A transconductance element based on using a matched pair of depletion MOS transistors and a voltage inverter was introduced in 1986 [1]. In modern MOS technology where usually depletion transistors are not available it is desirable to have linear transconductor elements using enhancement MOS transistors. The four MOS transistor circuit introduced in 1986 [2–3], and generalized in 1987 [4] was the first cell which cancels completely the nonlinearities of the MOS transistors. Very recently the same 4 MOS transistor circuit was used with the CC II [5] to realize a transconductance element [6].

The purpose of this paper is to introduce a transconductance element using only two matched MOS transistors and a current conveyor, which can be either CC I [7] or CC II. The proposed cell is also suitable for realizing a linear voltage multiplier with a current output.

The transconductor cell is shown in **Fig. 1**, which employs two matched MOS transistors operating in the nonsaturation region and a single current conveyor CC II. The current conveyor CC II will invert the drain current I2 so that the output current of the cell Io is given by

$$I_0 = I_1 - I_2. \tag{1}$$

The two currents I_1 and I_2 are [8]

$$I_1 = K\left[(V_{G1} - V_T)(V_i - V_S) + a_2\left(V_i^2 - V_S^2\right) + a_3\left(V_i^3 - V_S^3\right) + \ldots\right] \tag{2}$$

$$I_2 = K\left[(V_{G2} - V_T)(V_i - V_S) + a_2\left(V_i^2 - V_S^2\right) + a_3\left(V_i^3 - V_S^3\right) + \ldots\right] \tag{3}$$

where

$$K = \mu_n C_{OX}\left(\frac{W}{L}\right). \tag{4}$$

μ_n is the electron mobility, C_{OX} is the gate-oxide capacitance, $\frac{W}{L}$ is the transistor aspect ratio.

From (1), (2) and (3) it follows that

$$I_0 = K\left[(V_{G1} - V_{G2})(V_i - V_S)\right]. \tag{5}$$

It is seen that the output current is linearly proportional to the voltage (V_{G1}–V_{G2}) and also proportional to (V_i–V_S). With $V_S = 0$ however, (5) simplifies to

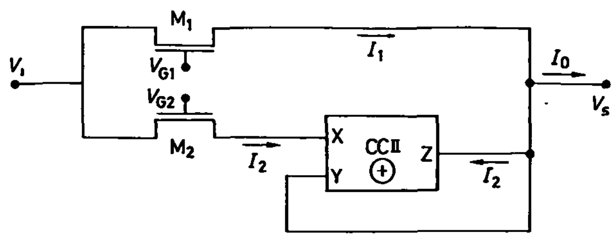

Fig. 1: Transconductance element

* Professor and Head Electronics Group, Electronics & Com. Eng. Dept. Cairo University, Egypt

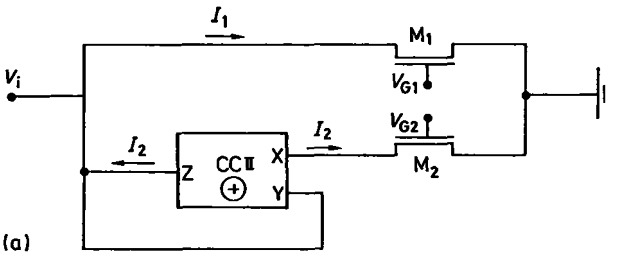

Fig. 2a: Grounded resistor

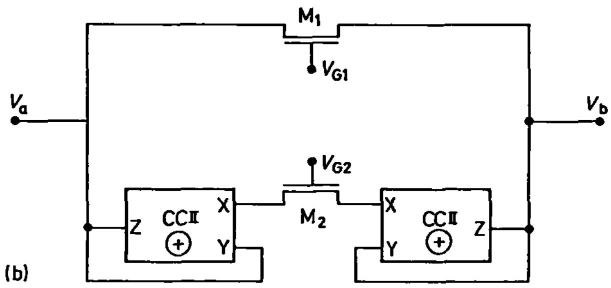

Fig. 2b: Floating resistor

$$I_0 = K[V_C][V_i] \tag{6}$$

where

$$V_C = V_{G1} - V_{G2}. \tag{7}$$

Thus the circuit converts linearly the input voltage V_i to the output current I_0 with the transconductance

$$g_m = KV_C. \tag{8}$$

It is seen that the transconductance g_m is linearly controlled by the control voltage V_C given by (7).

A necessary condition for the two MOS transistors to operate in the nonsaturation region is (assuming a positive transconductance is realized)

$$V_{G2} > V_i + V_T. \tag{9}$$

If a negative transconductance is realized however, that is if $V_{G1} < V_{G2}$, then (9) should be modified to

$$V_{G1} > V_i + V_T. \tag{10}$$

Of course with V_i and V_C as the two inputs, the cell acts as a linear multiplier with a multiplier constant K. The multiplier given in [6] employs two opposite polarity current conveyors and two MOS transistors. It should be noted that the circuit given in [1] which realizes a transconductance element can not be modified to realize a grounded resistor. The proposed circuit however has a very attractive feature that by interchanging CC II and M_2 as shown in **Fig. 2a**, the circuit realizes a grounded linear resistor with a resistance $R = 1/KV_C$ which can be either positive or negative. This is similar to the resistor reported in [9] with CC II acts as a current inversion negative impedance converter. Using both CC IIs as shown in **Fig. 2b**, a floating resistor is obtained [9].

In conclusion, it is worth noting that the first generation current conveyor CC I can replace CC II in all circuits proposed here, with proper terminal connections of CC I. It is worth noting that the full nonlinearity cancellation is achieved with two MOS transistors and a single current conveyor (CC I or CC II), but it is not possible to achieve this propery with a single output op-amp and two matched MOS transistors.

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Professor Ahmed M. Soliman
Electronics and Communication Engineering Department
Cairo University
Faculty of Engineering
GIZA-Egypt

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