A New Method for Computer Simulation of First-Order Differential Equation with Variable Coefficients

A. K. BANDYOPADHYAY, P. K. DAS, A. BAGCHI, AND D. K. BASU

The differential equation for an RC low-pass circuit is

$$RC\frac{de_0(t)}{dt} + e_0(t) = e_i(t)$$

where $e_0(t)$ and $e_i(t)$ are the output and input voltages respectively.

In systems where the resistance R is varied from an external source [1], such that its value cannot be predicted but can be known at a given instant of time, the above equation can be solved numerically by methods described in the literature [2].

This paper describes a method for the numerical solution of the above equation which requires mainly one multiplication and one evaluation of the value R for each sample. This is an advantage over other methods, which require a greater number of multiplication and evaluation.

The present method is based on the realistic assumption that the value of R remains constant between two successive samplings.

Mathematically the input signal is represented by

$$e_i(t) = \left[\sum_{n=0}^{T/\tau} e_i(n\tau)\ \{u(n\tau) - u\ [(n+1)\tau]\}\right] rep\, T$$

where T = time-period of the input signal and τ = sampling interval.

We consider the output at $t = n\tau$ to be given by

$$e_0(t) = e_0(n\tau).$$

Shifting the origin ($t' = 0$) to the sampling instant of interest ($t = n\tau$) we write

$$e_0'(t') = e_0(t) \text{ and } e_i'(t') = e_i(t) \tag{1}$$

that is

$$e_0'(0) = e_0(n\tau) \text{ and } e_i'(0) = e_i(n\tau). \tag{2}$$

The original differential equation now becomes

$$RC\frac{de_0'(t')}{dt'} + e_0'(t') = e_i'(t') \tag{3}$$

whose solution for the initial conditions (2) is given by

$$e_0'(t') = e_0'(0) + [e_i'(0) - e_0'(0)]\ (1 - e^{-t'/RC}). \tag{4}$$

At $t' = \tau$

$$e_0'(\tau) = e_0'(0) + [e_i'(0) - e_0'(0)]\ (1 - e^{-\tau/RC}).$$

Returning to the original time frame through (1) and (2) we get

$$e_0\ [(n+1)\tau] = e_0(n\tau) + [e_i(n\tau) - e_0(n\tau)] \cdot (1 - e^{-\tau/RC}).$$

The value of R is calculated at the nth sampling instant and this is used along with the voltages $e_0(n\tau)$ and $e_i(n\tau)$ to obtain the output voltage at the next sampling instant. As a result the method requires a single multiplication per sample and a substantial saving of computer time is achieved.

Acknowledgment

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A. K. Bandyopadhyay and P. K. Das are with the Computer Centre, Electronics and Telecommunication Engineering Department, Jadavpur University, Calcutta, India.

A. Bagchi is presently with the Regional Computer Centre, Calcutta, India, on leave from Tata Consultancy Services, Bombay, India.

D. K. Basu is presently with the Regional Computer Centre, Calcutta, India.

Active RC Nonminimum Phase Network Using the DVCCS/DVCVS

F. S. ATIYA, A. M. SOLIMAN, AND T. N. SAADAWI

***Abstract*—A new configuration for realizing a second-order nonminimum phase transfer function using the differential voltage controlled current source, differential voltage controlled voltage source (DVCCS/DVCVS) as the active building block is given. The special cases of a notch filter and an all-pass network are considered.**

Recently [1], the DVCCS/DVCVS [2]-[3] was used as the active building block in the realization of bandpass and lowpass filters. In this letter the synthesis of a second-order nonminimum phase transfer function using the DVCCS/DVCVS is considered.

General Configuration

Fig. 1 represents the basic structure, where N is a three-port second-order passive RC bandpass network. The device is defined by the following relations [3]:

$$I_0 = G(V_- - V_+) \tag{1}$$

$$V_0 = \alpha V_g. \tag{2}$$

By direct analysis of the network, the transfer function is

$$\frac{V_0}{V_{in}} = -\frac{1}{\left(GR_1 - \frac{1}{\alpha}\right)} \cdot \frac{1 - aGR_1T(s)}{1 - \frac{GR_1T(s)}{\left(GR_1 - \frac{1}{\alpha}\right)}} \tag{3}$$

where $T(s)$ is the open circuit voltage transfer function of N, and is given by

$$T(s) = \frac{K\omega_p s}{s^2 + \left(\frac{\omega_p}{q_p}\right)s + \omega_p^2} \tag{4}$$

where $0 < q_p < 0.5$ and $Kq_p \leq 1$.

From (4) in (3), therefore,

$$\frac{V_0}{V_{in}} = -\frac{1}{\left(GR_1 - \frac{1}{\alpha}\right)} \cdot \frac{s^2 - s\frac{\omega_p}{q_p}(aGR_1Kq_p - 1) + \omega_p^2}{s^2 + s\frac{\omega_p}{q_p}\left(1 - \frac{GR_1Kq_p}{GR_1 - \frac{1}{\alpha}}\right) + \omega_p^2} \tag{5}$$

which realises a second-order nonminimum phase transfer function having

$$\text{a gain factor} = \frac{1}{GR_1 - \frac{1}{\alpha}} \tag{6}$$

$$\omega_0 = \omega_p \tag{7}$$

$$Q_0 = \frac{q_p}{aGR_1Kq_p - 1} \tag{8}$$

$$Q_p = \frac{q_p}{1 - \left(\frac{GR_1Kq_p}{GR_1 - \frac{1}{\alpha}}\right)}. \tag{9}$$

For the absolute stability of the circuit;

$$Kq_p < 1 - \frac{1}{\alpha GR_1}. \tag{10}$$

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The authors are with the Electronics and Communication Engineering Department, Cairo University, Giza, Egypt.

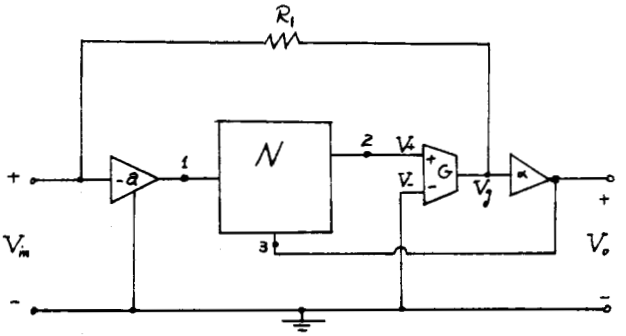

Fig. 1. The general configuration.

The VCVS a controls the position of the zeros and for a notch filter

$$a = \frac{1}{GR_1Kq_p}. \tag{11}$$

For an all-pass transfer characteristics

$$a = \frac{1}{GR_1Kq_p}\left(2 - \frac{GR_1Kq_p}{GR_1 - \frac{1}{\alpha}}\right). \tag{12}$$

Conclusions

The use of the DVCCS/DVCVS in the realization of a second-order nonminimum phase transfer function is discussed.

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Corrections to "Comments on 'A New Solution to Adaptive Control'"

C. RICHARD JOHNSON, JR., AND M. G. LARIMORE

In editing the above letter[1] several phrases were arbitrarily altered in attempting to standardize our letter to an unpublicized format for comments on published work. This change was carelessly executed, thereby obscuring the objective of the entire exchange. Furthermore, our corrections to the erroneous galley proofs were ignored. The purpose of the present letter is to alert the readership to this standardization in addition to providing specific corrections to the published comments.

By replacing our original reference to Martín-Sánchez's paper [1] with a footnote, our first sentence in [2] was standardized. This alteration required renumbering of the reference list in our manuscript. Unfortunately, we later referred to [1] in our second footnote, which was incorrectly left unaltered. In expanding this policy by removing any numbered reference by Martín-Sánchez to our comments [2], the copy editor committed a much more grievous error, obfuscating the entire purpose of the exchange. In the manuscript of his reply, which Martín-Sánchez graciously sent us, his seventh paragraph read "As remarked in [Johnson and Larimore's comment], if the plant inverse is unstable, the tracking of some kind of output trajectories may require an unbounded input signal." In the pursuit of standardization this reference was removed and the sentence was inaccurately rewritten to imply that this comment had been made originally by Martín-Sánchez in [1]. It was precisely this omission that precipitated our comments in [2]. The careless effort in consolidating the reference lists is further emphasized by the duplication of reference four as reference ten.

Upon receipt of the galley proofs we spent several hours correcting these changes while trying to obey the implicit standardization. We also corrected a technical error in the second paragraph, i.e., $\det [\Sigma_{m=1}^{r} z^{-m} B_m]^{-1} = 0$ should read $\det [\Sigma_{m=1}^{r} z^{-m} B_m] = 0$, requiring only a simple deletion. These efforts were completely overlooked despite our prompt return of the proofs within the requested 72 hour period.

References

[1] J. M. Martín-Sánchez, "A new solution to adaptive control," *Proc. IEEE*, vol. 64, no. 8, pp. 1209–1218, Aug. 1976.
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C. R. Johnson, Jr., was with the Department of Electrical Engineering, Stanford University, Stanford, CA. He is now with the Department of Electrical Engineering, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061.
M. G. Larimore was with the Department of Electrical Engineering, Stanford University, Stanford, CA. He is now with the Department of Electrical Engineering, University of Colorado, Colorado Springs, CO 80907.
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Integrable Digital Pulse Rate Doubler

K. W. CURRENT

Abstract—**A pulse rate doubling technique for periodic digital signals is described. This circuit is fully compatible with silicon bipolar integrated circuit (IC) technology; no discrete capacitors are required. The difference in storage times between an n-p-n transistor and lateral p-n-p transistor is used to generate the output pulse sequence.**

Introduction

Digital pulse rate multipliers often employ sophisticated voltage to frequency converters, error sensing circuits, counters, dividers, and phase-lock loops to develop the desired output sequence, for example [1]–[3]. In many applications such sophistication is unnecessary. In this correspondence, we present a pulse rate doubling circuit that is monolithically implementable since only silicon bipolar n-p-n and p-n-p transistors and diffusible resistors are required; no discrete capacitors are necessary. The doubled pulse rate is obtained by exploiting the inherent difference in storage times of an n-p-n transistor and lateral p-n-p transistor.

Circuit Description and Operation

The pulse rate doubling circuit is shown in Fig. 1. Input and output waveforms are shown in Fig. 2. Transistors T_1 and T_2 reproduce the digital input waveform as a pair of differential waveforms, V_{C1} and V_{C2}. The collectors of T_2 and T_1 drive identical capacitanceless monostable circuits [4], T_4, T_5, T_8, T_9 and T_6, T_7, T_{10}, T_{11}, respectively. Each monostable multivibrator section operates in the same way, so let us consider transistors T_4, T_5, T_8 and T_9. With V_{C2} in the low state T_4 will be biased off and, with the appropriate selection of resistors R_6, R_9 and R_{10}, T_5 will saturate. The voltages across R_7 and R_{10} will exceed 1 V_{BE} driving transistor T_8 and T_9 into saturation. Now the input waveform switches states causing V_{C2} to switch to the high state. The voltage V_{B4} is now sufficient to turn on and saturate T_4 which subsequently turns off T_5. In this case, V_{R7} and V_{R10} are less than 1 V_{BE} and transistors T_8 and T_9 are forced to turn off. Due to the difference in storage times in the lateral p-n-p transistor T_8 and n-p-n transistor T_9, T_9 will turn off first, leaving T_8 still conducting. Thus with T_9 off, V_{R12} now rises to nearly V_{CC} volts and then returns to zero as T_8 turns off. The resultant waveform at the collector of T_9 is then a pulse with duration dependent upon the charge stored in the base and storage time of T_9, and the resistance in the discharge path. The collector of T_9 drives transistor T_{12}. Transistor T_{12} serves as one input of a 2 input ECL "OR" gate, T_{12}, T_{13}, and

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The author is with the Department of Electrical Engineering, University of California, Davis, CA 95616.