

A New 65nm-CMOS 1V 8GS/s 9-bit Differential Voltage-Controlled Delay Unit Utilized for a Time-Based Analog-to-Digital Converter Circuit

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Abstract—A new differential Voltage-Controlled Delay Unit (VCDU) is proposed. The VCDU converts an input voltage into a pulse delay, and delivers it to a Time-to-Digital Converter (TDC) which outputs a digital word. Both circuits form a Time-Based Analog-to-Digital Converter (ADC). In scaled CMOS technology, the Time-Based ADC is a substantial block in designing Software Defined Radio (SDR) receivers, as it exhibits high speed and low power. The new manually-calibrated differential VCDU circuit operates on a high sampling frequency of 8GS/s in 65nm CMOS technology, with a supply voltage of 1V. It achieves a wide dynamic-range of 0.56V at a 3% linearity error and effective-number-of-bits (ENOB) of 8.9 bits. Additionally, it consumes an area of 742 μm^2 and a power consumption of 1.6mW. A metal-insulator-metal capacitor is used to minimize the process-voltage-temperature variations. The simulation results are compared to single-ended VCDU results and to state-of-the-art analog-part ADCs results to show the strength of the proposed design.

Keywords—Nanometer CMOS technology; voltage-controlled delay unit; time based analog-to-digital converter; software defined radio; metal-insulator-metal capacitor; effective-number-of-bits; linearity.

I. INTRODUCTION

The significance of Analog-to-Digital Converters (ADCs) becomes more crucial in emerging applications such as Software Defined Radio (SDR) receivers [1], [2] for future ultra-wide-band wireless communication services. A single Integrated Circuit (IC) of SDR receiver can acquire several chains of operating blocks of different wireless standards. It can configure and control the required chain, otherwise all chains will be switched on. This overcomes the high dissipated power and the wasted area of other receivers. This leads to exploit a new reconfigurable high-speed low-power less-area ADC. In SDR receiver, the received RF signal is applied to an ADC, followed by a digital signal processor (DSP).

The revolution of the deep sub-micron CMOS technology shows the improvement of conventional ADCs is highly challenging compared to digital systems [1]–[4]. In high frequencies, the time resolution of digital signals is so efficient. Consequently, the ADC digital part percentage will be increased in order to: (1) get the full use of the DSP, (2) reduce area

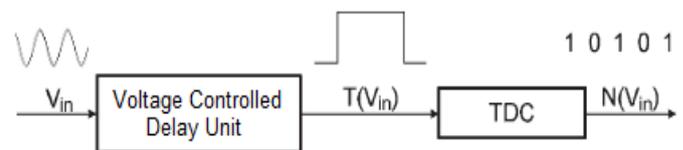


Fig. 1. Time-based ADC architecture.

and power consumption of the analog blocks and (3) speed the ADC up. In Time-Based ADC architecture, shown in Fig. 1, a Voltage-Controlled Delay Unit (VCDU) samples the signal amplitude into stream of pulses in the time-domain, then a Time-to-Digital Converter (TDC) quantizes the pulses into digital words [3].

Several VCDU circuits in CMOS 0.18 μm technology have been introduced in the literature [5]. The basic VCDU circuit controls proportionally the delay of the input clock edge with respect to a sampled input voltage. There are superb advantages in the differential design. Firstly, the even-order harmonic components caused by a single-ended VCDU non-linearity will be suppressed. Secondly, the differential input offers a doubling of the signal amplitude resulting in an improvement in the SNR. Finally, the common-mode noise will be rejected. In this paper, a new manually-calibrated differential VCDU circuit is presented and compared to its single-ended design in the CMOS 65nm technology node.

This paper presents a new VCDU circuit, in which promising results are achieved in linearity, dynamic range (DR), effective-number-of-bits (ENOB), sensitivity and Figure-of-Merit (FOM) with a higher operating sampling-rate at the expense of extra area/power overheads. A metal-insulator-metal capacitor (MIMCAP) is used to degrade the process-voltage-temperature (PVT) variations. The rest of the paper is organized as follows. Section II discusses design and analysis of the proposed circuit. Simulation results are demonstrated for the proposed design with its single-ended design and state-of-the-art analog-part ADCs in Section III. Finally, the presented work is summarized in Section IV.

II. PROPOSED DESIGN AND ANALYSIS

The new proposed VCDU architecture is based on the diff-

ifferential approach as shown in Fig. 2. The upward VCDU core converts the positive input voltage into a time-difference variable (ΔT_2) measured with respect to a reference clock event (Φ_{CLK}). The downward VCDU core converts the negative input voltage into a time-difference variable (ΔT_1) measured with respect to Φ_{CLK} . Each time-difference variable is considered the delay equation of a single-ended VCDU circuit. So, the delay equation of the proposed differential VCDU design (ΔT_0) is the time difference between ΔT_2 and ΔT_1 . Fig. 3 illustrates the timing diagram of the proposed design. Due to the fact that the VCDU circuit is considered a buffer delay circuit, the time-difference variables are measured between the rising edges of both Φ_{CLK} and their corresponding output (Φ_{O2} and Φ_{O1} respectively).

Fig. 4 portrays a single VCDU core circuit schematic. During the logic '0' of Φ_{CLK} , the capacitor (C) is reset via M6. When Φ_{CLK} raises up to logic '1', C charges by the current (I_{IN}) through the transmission gate switch formed by transistors M4 and M5. I_{IN} is generated by a Wilson current mirror [6] formed by M1-M3. M2 has a high gate voltage to decrease the high sensitivity of the current value to neglect gain-source voltage variations. The current-steering amplifier, constructed by M7-M13, senses the difference between the input voltage (V_{IN}) and the capacitor voltage (V_A) and lets the latching circuit M14-M17 make a logic decision. The output inverter M18-M19 provides a high linear output delay. Once V_A reaches the desired V_{IN} , the VCDU core output switches to logic '1'.

In fact, C is a MIMCAP which is a parasitic capacitor between the higher metal layers (i.e. Metal 7 and Metal 8). It has a higher density and linearity and smaller parasitic capacit-

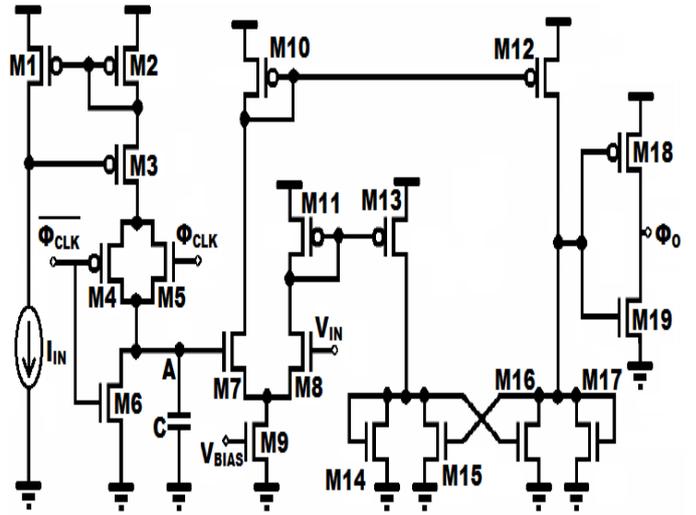


Fig. 4. The single VCDU core circuit schematic.

ances. Generally, it can highly overcome the PVT variations that happen in the drain-source voltage (V_{DS}) of a MOSFET capacitor especially at high frequencies [7]. The main disadvantage of the MIMCAP is that it consumes a larger area as the field-oxide insulator is thicker than the gate-oxide of the MOSFET capacitor. Also, there will be few process-corner variations as an expense of the insulator thickness over several wafer lots [8].

III. SIMULATION RESULTS

Design simulations were conducted on Cadence Virtuoso using industrial Taiwan Semiconductor Manufacturing Corporation (TSMC) 65nm CMOS technology. These results are tested using MATLAB. Optimal bias conditions have been selected using a manual calibration technique by which the largest linear range can be achieved. The applied DC voltage for the proposed differential design and the single-ended design is 0.5V and 0.55V, respectively. The supply voltage is 1V, while the operating clock frequency which has a 50% duty cycle is 8GHz for both designs. The capacitor's value is 167fF.

A. Linearity and Dynamic Range

The method of sweeping the input voltage in order to get a wide linear range during calibration has been discussed in [9]. Fig. 5(a) and Fig. 5(b) show the dynamic range of the proposed differential VCDU design and the single-ended VCDU design, respectively, where the linear input voltage range of the proposed design is clearly enhanced. Fig. 6(a) and Fig. 6(b) show the linearity error check for both designs, respectively.

Table I shows all specifications of both designs at an 8GHz sampling frequency (F_s). It illustrates that the proposed design has a better dynamic range, sensitivity and FOM at the expense of the area, power dissipation and the root-mean-square (RMS) noise than the single-ended design.

B. Voltage Sensitivity

Among the linear range, any two points will be chosen to evaluate the slope between the delay (y-axis) and V_{IN} (x-axis).

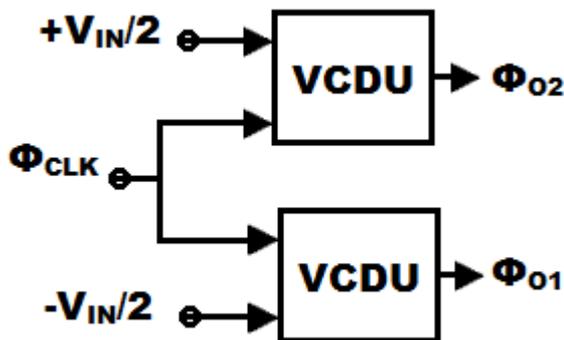


Fig. 2. The proposed differential VCDU architecture.

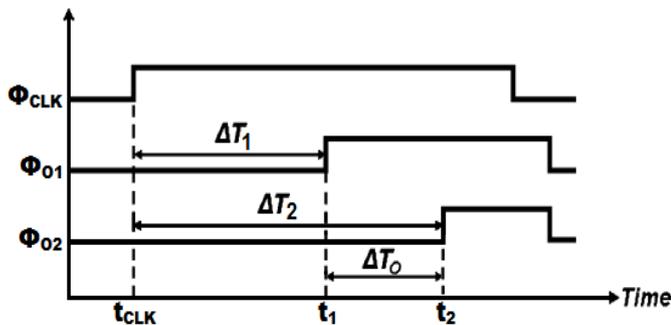


Fig. 3. The proposed design timing diagram.

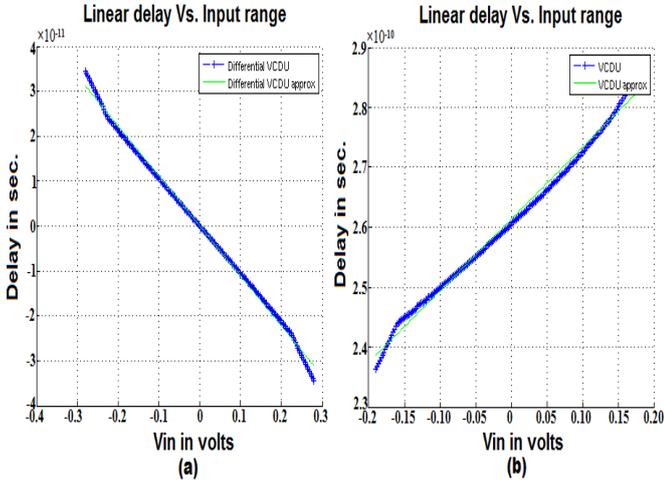


Fig. 5. Curve fitting of the linear range using MATLAB. (a) The proposed differential VCDU circuit. (b) The single-ended VCDU circuit.

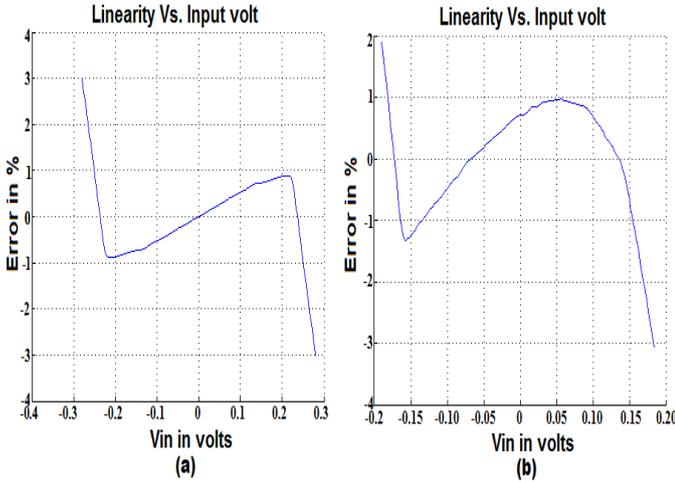


Fig. 6. Linearity error check of the linear range using MATLAB: (a) The proposed differential VCDU circuit. (b) The single-ended VCDU circuit.

The slope represents the sensitivity of a circuit. The sensitivity equals to $0.9ps/mV$ for the proposed design, while it equals to $0.3ps/mV$ for the single-ended design. The proposed design shows a higher sensitivity as the sensitivity is a function of the delay which is enhanced due to the differential approach.

C. Maximum Sampling Frequency and Power Consumption

Due to the fact that high frequencies distort the signal linearity, low-frequency applications can get higher dynamic range. In fact, high frequency applications have larger power dissipation (P_D) [3]. This power can be minimized by decreasing transistors' size. Hence, the flowing current will get higher resistance from electrons and it will be decreased.

D. Noise Simulation

Noise represents a random fluctuation in any electrical signal [10]. Thermal noise is the main dominant noise parameter of a MOSFET transistor represented in equation (1). Where V_N is the RMS voltage due to thermal noise generated in a resistance over a bandwidth in a room temperature. The

main contributing noise parameters in the proposed design are the flowing current of the steering amplifier, the output inverter and the latching circuit of each VCDU core circuit. They contribute with a percentage of 41.3%, 32.2% and 25.6% from the overall total output referred noise ($V_{N,RMS}$), respectively. $V_{N,RMS}$ is represented in Table I for an 8GHz wide frequency which is larger in case of the proposed design due to its larger number of transistors.

TABLE I: Performance summary of the proposed differential design and the single-ended design at an 8GHz F_S

Parameter	This work	The single-ended design
V_{IN} Range	-0.28V: +0.28V	-0.19V: +0.19V
Dynamic Range (V)	0.56	0.38
Input DC Bias (V)	0.5	0.55
Linearity Error (%)	3	3
Sensitivity (ps/mV)	0.9	0.3
P_D (mW)	1.6	0.8
Area (μm^2)	742	360
FOM ($\times 10^{12}$)	1.6	1.3
Noise ($nV/Hz^{1/2}$)	14.5	10.2
ENOB (bits)	8.9	5.7

The total RMS noise should be less than a single step conversion of the ADC as in equation (2). Where V_{FS} and N are the full scale voltage and the number of bits, respectively. So, this design can be part of a 9-bit ADC due to an $1.3mV$ $V_{N,RMS}$ which lets the proposed design have a good ENOB.

$$V_N = (4KTR\Delta F)^{1/2} \quad (1)$$

$$V_{N,RMS} < V_{FS} / (2^N - 1) \quad (2)$$

E. Area

The area of the proposed design, shown in Fig. 7, is $742 \mu m^2$ which is bigger than by a factor of 2X that of the single-ended design due to the circuit metal wire connections. The area of the MIMCAP is $156 \mu m^2$ which can be added on the differential VCDU layout due to its higher metal layers.

F. Effective-Number-of-Bits

ENOB is considered the main metric that tests all different types of errors (including noise and distortion errors) that a circuit practically faces. The ENOB is calculated at an input frequency of 3.5GHz in order to ensure that Nyquist conditions are achieved [4]. In equation (3), SNDR represents the signal to noise and distortion ratio. The proposed design shows a higher ENOB than the single-ended design due to the utilized differential architecture and the MIMCAP that enhanced the linearity.

$$ENOB = (SNDR - 1.76) / 6.02 \quad (3)$$

G. Figure-of-Merit

The Figure-of-Merit (FOM) approach has been discussed, in [11], as in equation (4). The FOM represents the efficiency of using the power to increase the dynamic range and/or the maximum frequency. The proposed design has a higher FOM due to the higher DR and F_S and the lower dissipated power.

$$FOM = (DR^2 \times F_S) / P \quad (4)$$

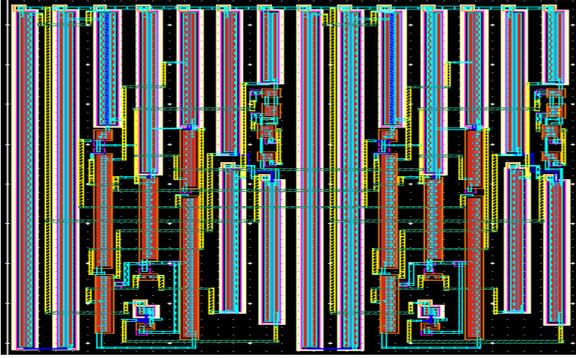


Fig. 7. The proposed design layout using Calibre

TABLE II: Comparison of 65nm CMOS state-of-the-art analog-part ADCs at a 3% acceptable error

Parameter	This	[12]	[13]	[14]	[15]
Supply Voltage (V)	1	2.5	1	1.2	1.2
Dynamic Range (V)	0.56	0.8	0.2	0.13	0.5
Sensitivity (ps/mV)	0.9	-	0.3	0.4	-
ENOB (bits)	8.9	11.2	3.5	3.7	4.9
P_D (mW)	1.6	7	4	21.4	3.7
Area (mm^2)	0.00074	0.075	0.0008	-	-
F_S (GHz)	8	2.4	5	6	2
FOM ($\times 10^{12}$)	1.6	0.2	0.1	0.01	0.1

Table II demonstrates a comparison between the proposed design and state-of-the-art analog-part ADCs [12]–[15]. According to Table II, this work provides a higher FOM, sensitivity and sampling speed that a circuit can operate on and a lower power consumption and area. Also, it provides a reasonable dynamic range and ENOB. Optimization of the proposed design is an active current research work to: combine the proposed design with a new differential TDC circuit to form a complete differential time-based ADC circuit, and add an automatic calibration circuit for the whole system to omit the PVT variations resulted from the TDC block.

IV. CONCLUSION

In this paper, a new manually-calibrated differential VCDU circuit is proposed which achieves a higher operating sampling frequency, linearity, ENOB, dynamic analog input range and sensitivity on 65nm technology. The novelty in this design is emerged from the dependency on three major factors. The first is the power of the CMOS technology which provides a high-speed, low-area and low-power design. The second is the differential architecture, in which the even order harmonics are suppressed as well as the input voltage noise. The third is depending on the MIMCAP which degrades the PVT variations.

The proposed design is compared to the single-ended VCDU circuit and state-of-the-art ADCs to show its simulation results strengths. It provides an 8GS/s sampling-speed, 0.56V dynamic range, 8.9bits ENOB, 0.9ps/mV sensitivity, 1.6mW power, 742 μm^2 area, 1.6 $\times 10^{12}$ FOM and 14.5nV/Hz^{1/2} RMS

noise. This work is a part of a differential time-based ADC and it is suitable for high-accuracy high-frequency applications especially the SDR application.

V. ACKNOWLEDGEMENT

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